Tri-Gen MVL-SRAM Based Ternary and Quaternary SRAM Design Using CMOS FinFET and CNTFET Technologies

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***Abstract*—This paper presents Triple-Generation Multi-Valued Logic Static Random Access Memory (Tri-Gen MVL-SRAM), a unified framework for the design and evaluation of ternary and quaternary SRAM architectures across three transistor technologies: 90 nm planar Complementary Metal-Oxide-Semiconductor (CMOS) transistor, 14 nm Fin Field-Effect Transistor (FinFET), and 32 nm Carbon Nanotube Field-Effect Transistor (CNTFET). The objective is to investigate the scalability and performance of multi-valued SRAM architectures while maintaining stability, reliability, and energy efficiency beyond the capabilities of conventional binary memory systems. To enable a fair cross-technology comparison, identical 12T ternary and quaternary SRAM cells were designed and evaluated in the Cadence environment using a consistent simulation methodology with technology-specific device models, supply voltages, and equivalent operating conditions. FinFET technology was employed as an advanced CMOS scaling reference, whereas CNTFET-based implementations utilized chirality-controlled threshold-voltage tuning to realize stable multi-level logic states. Simulation results demonstrate that the proposed CNTFET-based MVL-SRAM achieves lower static power consumption, reduced read/write delay, improved Static Noise Margin (SNM), and a lower Power-Delay Product (PDP) compared with both CMOS- and FinFET-based implementations. Although FinFET technology offers improved performance over conventional planar CMOS, its limited voltage headroom restricts the stability of higher-order logic levels at advanced technology nodes. The comparative analysis demonstrates that CNTFET technology provides superior support for multi-valued SRAM implementation by combining enhanced energy efficiency, improved noise immunity, and reliable multi-level operation. Consequently, the proposed Tri-Gen MVL-SRAM framework provides a comprehensive evaluation platform and serves as a promising solution for high-density cache memories, Artificial Intelligence (AI) accelerators, neuromorphic processors, Internet of Things (IoT) devices, and edge-computing applications requiring optimized power, area, and performance.**

***Index Terms*—CNTFET technology, low-power memory design, multi-level SRAM, ternary and quaternary logic, 14 nm FinFET, 90 nm CMOS SRAM**

I. Introduction

The rapid advancement of digital systems has been driven by the increasing demand for higher computational performance, greater data storage density, and lower power consumption. Modern applications, ranging from smartphones and Artificial Intelligence (AI) accelerators [1] to cloud computing and Internet of Things (IoT) devices, require highly efficient computation and storage capabilities. Consequently, conventional binary logic systems are facing growing challenges in meeting these requirements. Binary logic, which relies on two voltage levels representing logical states '0' and '1', has dominated digital circuit design for decades due to its simplicity, strong noise immunity, and compatibility with Complementary Metal-Oxide-Semiconductor transistor (CMOS) technology. However, as integrated circuit technologies continue to scale toward advanced technology nodes, the physical and architectural limitations of binary logic have become increasingly evident [2]. It involves increased power density, interconnect bottlenecks and leakage current, particularly as more transistors are packed into inadequate silicon real estate [3]. Regarding this, the researchers have turned to Multi-Valued Logic (MVL) which is considered as a promising paradigm which permits more than two logic levels in a single signal line [4]. MVL provides the capability to process and store more data using few transistors and interconnections. Exactly, ternary logic utilizes 3 discrete levels generally 0, $V_{DD}/2$, and V_{DD} [5], while quaternary logic extends to four levels namely 0, $V_{DD}/3$, $2V_{DD}/3$, and V_{DD} [6]. It permits one ternary digit (trit) to signify approximately 1.585 binary bits and one quaternary digit (quat) to signify 2 bits [7]. Accordingly, MVL provides the theoretical potential for increased information density, decreased power usage and small chip areas in contrast to binary systems. Multi-level data storage which is an extension of MVL, emphases on encoding and preserving multiple data levels in individual memory cells or logic elements. Hence, storage systems can attain significantly high data densities and throughput without physically increasing the number of memory cells. It is particularly beneficial in applications necessitating higher storage efficacy under area and power constraints, such as neuro-morphic computing, embedded systems, portable electronics and high-performance computing systems.

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Traditionally, digital storage and processing architectures have been based on binary logic. In conventional memory systems, such as Static Random-Access Memory (SRAM) and Dynamic Random-Access Memory (DRAM) [8], each memory cell stores a single bit of data corresponding to one of two logic states, namely '0' or '1'. Binary logic gates and storage units are modest to implement and are highly robust to noise to the wide voltage margin between logic levels. Also, the tools and processes for binary logic are also established, making design, verification and manufacturing cost-efficient and scalable. Although, certain restrictions are now being encountered such as scaling, with the miniaturization of transistors, leakage currents and inconsistency upsurge, distressing the stability and power efficacy of binary circuits, interconnect complexity in which additional data needs numerous wires and in binary systems, interconnect density evolves rapidly with system complexity, impacting signal integrity and growing parasitic effects and restricted data density in which each binary memory cell stores only one bit. Attaining higher capacity characteristically includes shrinking cell size or using 3D stacking, both of which complicate fabrication and decreases the production.

A. Problem Statement

The ongoing development of SRAM technology needs to satisfy increasing requirements from high-density computing and high-speed computing and low-power computing systems but this development has revealed basic restrictions present in traditional binary memory systems. The supply voltage decrease causes planar CMOS SRAM cells to experience higher leakage power and their static noise margin decreases while their process variation tolerance drops together with their soft error vulnerability and noise-induced bit flip risk. The new application areas which include artificial intelligence accelerators and neuromorphic processors and biomedical embedded systems and environments with radiation exposure become more difficult to handle because they require both reliable performance and efficient power usage. The MVL SRAM architecture native to ternary and quaternary designs functions as a superior option to binary memory because it enables higher data storage capacity while simplifying connection requirements between memory components. Research has confirmed that ternary SRAM cells minimize energy use while quaternary logic circuits achieve power efficiency and application-specific SRAM designs deliver dependable performance. The existing research restricts itself to one particular transistor technology because it examines only CMOS and FinFET and CNTFET implementations.

The MVL encoding explains performance improvements because the underlying device technology shows better results. FinFET technology provides better electrostatic control and lower leakage than planar CMOS but limits threshold voltage tuning which prevents stable voltage separation between higher-order MVL states. CNTFET technology provides built-in advantages through its ability to enable near-ballistic transport and control its threshold voltages with chiral properties which makes it an excellent choice for dependable MVL memory. The existing research needs to conduct a thorough and unbiased assessment of ternary and quaternary SRAM architectures which use CMOS, FinFET, and CNTFET technologies across different generations. The research problem exists because researchers lack a unified framework which evaluates multi-valued SRAM architecture scalability, stability, and energy efficiency across different transistor generations under the same design and operating conditions. The research needs to close this gap because it determines the actual capabilities of MVL-SRAM while discovering the best device technology for upcoming memory systems which require high density, low power consumption, and dependable performance.

B. Motivation for Triple-generation MVL-SRAM

The implementation of traditional binary SRAM designs with planar CMOS technology faces multiple difficulties which arise from technology advancements because leakage currents increase and noise margins decrease and interconnect systems become more intricate. The development of FinFET technology represents the next stage of CMOS development because it provides better electrostatic control and eliminates short-channel effects, but it still suffers from limitations that prevent proper voltage scaling and binary data handling. MVL has been widely recognized as a promising alternative, as ternary and quaternary logic systems enable higher information density per memory cell and reduced interconnect overhead. The existing research on MVL-SRAM systems does not provide clear performance assessment methods because it limits its testing to one specific transistor technology which makes it hard to determine whether performance improvements result from logic encoding or device advantages. The study employs a triple-generation evaluation method which uses planar CMOS technology, multi-gate FinFET technology, and nanoelectronic CNTFET technology for its research evaluation. The method provides a fair and organized assessment of how MVL-SRAM technology develops through different transistor generations.

C. Tri-Gen MVL-SRAM Concept

This paper presents Tri-Gen MVL-SRAM (triple-generation multi-valued logic static random access memory), which serves as a comprehensive design and testing platform to assess ternary and quaternary SRAM systems across three different transistor technology nodes from 90 nm CMOS which represents standard binary memory technology to 14 nm FinFET which shows advanced scaled CMOS with better electrostatic management and 32 nm CNTFET which demonstrates new nanoelectronic technology with near-ballistic electron movement. The researchers of Tri-Gen MVL-SRAM present their work through a cross-technology framework which separates the effects of device scaling from the advantages that multi-valued logic systems provide. The FinFET implementation functions as an essential middle point which enables researchers to compare CMOS

designs using extreme scaling with CNTFET-based MVL systems through identical testing conditions.

D. Key Contributions of This Work

The proposed Tri-Gen MVL-SRAM framework provides a comprehensive three-generation evaluation platform for analyzing both ternary and quaternary SRAM architectures implemented using 90 nm CMOS, 14 nm FinFET, and 32 nm CNTFET technologies. To ensure a fair cross-technology comparison, identical 12-Transistor (12T) SRAM topologies were designed and evaluated using a consistent simulation methodology with technology-specific device models, supply voltages, and equivalent operating conditions. The comparative analysis evaluates key performance metrics, including static power consumption, read and write delay, Static Noise Margin, and Power-Delay Product. The proposed CNTFET-based MVL-SRAM architecture shows superior energy efficiency, enhanced noise robustness, and overall improved performance compared to CMOS and FinFET implementations. These results offer important design insights for creating scalable, high-density, low-power multi-valued memory systems for future computing applications.

II. Literature Survey

The following literature review presents an overview of existing CMOS- and CNTFET-based SRAM architectures and their key performance characteristics. CMOS technology has been extensively employed to enhance memory performance, achieving a memory window of 1.87×10^7 through the incorporation of nano-cavity arrays and optimized electrode geometries. Furthermore, sensing metrics were evaluated in SRAM-based Ternary Content Addressable Memories (TCAMs), demonstrating improved memory functionality and performance [9]. Similarly, a ternary SRAM architecture based on CNTFETs was developed to improve robustness against temperature variations and radiation-induced effects caused by high-energy particle strikes. The reported results demonstrated reliable operation under varying environmental conditions, highlighting the suitability of CNTFET technology for advanced memory applications [10]. The ternary logic execution with CNTFET has been used due to the condensed interconnect complexity and chip area. And also, the read and write operations, noise margins of the power consumption has been effectively analyzed and enhanced [11]. The power and noise performances of the suggested 8 T CNTFET based SRAM cells has been observed for write, hold and read operations. Furthermore, the write and hold stability of the proposed SRAM cell was assessed using the Static Noise Margin (SNM) metric [12]. Additionally, a 10T CNTFET-based SRAM cell was proposed to address the performance and stability challenges associated with conventional SRAM architectures. The reported design achieved a hold power consumption of 0.5527 nW, a read power consumption of 1.8087 nW, and a Write Static Noise Margin (WSNM) of 432.4 mV, demonstrating improved power efficiency and stability characteristics for low-power memory applications [13].

Correspondingly, the CNTFET based 6T SRAM cells has been made due to the usage of INDEP (low power Input Dependent) technique. The proposed CNTFET-based SRAM cell demonstrated improved performance and reduced execution time during hold, read, and write operations [14]. The CMOS and CNTFET based 8 T SRAM cell design has been utilized due to the ballistic transport and carrier mobility of the semiconducting nanotubes in CNTFET. Moreover, the performance and accuracy has been easily attained [15]. The CNTFET has a performance due to the charge mobility, gate control and electrostatics. Furthermore, a low-power 8T SRAM cell was developed using CNTFET technology. The proposed design achieved significant improvements in the read and write power-delay product, with enhancement factors of 1.02× and 1.85×, respectively [16]. The CNTFET focused SRAM cell with write operation has been used to enhance the performance and also offers to lessened dynamic power, write delay and leakage power. Moreover, the suggested technology has performed with enhanced accuracy and stability [17]. Subsequently, the CNTFET has been used to analyze the robustness alongside with radiation in changing memory cells and also the robustness has been tested in contrast to voltage, temperature [18].

Ultimately, the energy efficient high bandwidth array design using SRAM has been used to enhance the model performance. The design integrates optimization techniques such as a Column Multiplexer (CM) ratio of 1, a Flying Bit Line (FBL) architecture, and an energy-efficient column design, which collectively improve memory performance, bandwidth, and energy efficiency [19]. The CMOS has been incorporated into a single chip, which has resulted in decrease in chip size which mainly uses the less space. Moreover, the CMOS based 9 T SRAM has been analyzed to test performance on numerous CMOS technologies, which has been resulted to attain average performance [20]. Additionally, a CMOS SRAM cell was analyzed using a physics-based model of the actual device structure, enabling accurate extraction of local photocurrent characteristics. Consequently, the transient radiation upset threshold of the SRAM circuit was effectively predicted and experimentally verified [21]. Eventually, the CMOS SRAM has observed transient bit flips due to the intrinsic transistor noise and also the MTTF (Mean Times to Failure) has been compared with extreme voltage, temperature and varying conditions. As a result , the MTTF spans from 0.1 ms to 108 s [22]. The CMOS technology scaling has been utilized to increase the SRM density and performance. In addition with, the larger and faster on-die cache has been utilized to the performance of microprocessors [23].

The CMOS inverter and 6T SRAM at various V_{DD} values has been high by at least 30% and also Nickel Silicide (NiSi) has been incorporated into electrical devices and has resulted in targeted electrical behavior of flexible devices [24]. Eventually, the SRAM has static noise margin due to the single quaternary digit line and has been applicable for MVL SRAM design. The simulation

outcomes due to the usage of HSPICE with 32 nm Stanford comprehensive CNTFET model, which has established the operations and also the SRAM cell has been used in a 4 × 4 SRAM array structure and has mainly lowered the power consumption [25]. Quaternary Static Random-Access Memory (QSRAM) has emerged as an important component in modern microprocessors and Very Large-Scale Integration (VLSI) systems. QSRAM architectures have employed Quantum Dot Channel Field-Effect Transistors (QDC-FETs) and Spatial Wave function Switched Field-Effect Transistors (SWS-FETs) owing to their low power consumption and compact device footprint. Furthermore, the reliability and stability of QSRAM have been evaluated to assess its susceptibility to errors and the overall impact of fault conditions on memory performance [26]. Moreover, quaternary logic gates, namely Quaternary Minimum (QMIN), Quaternary Maximum (QMAX), Standard Quaternary Inverter (SQI), Standard Quaternary NAND (SQNAND), standard quaternary NOR (SQNOR), and Standard Quaternary XOR (SQXOR), were implemented using CNTFET technology. Simulations performed using the 32 nm CNTFET model in HSPICE demonstrated low average power consumption and achieved a 73%–91% reduction in Power-Delay Product (PDP) compared with conventional designs [27].

A 7T CNTFET-based SRAM cell was proposed to improve power efficiency and Static Noise Margin (SNM) compared with conventional 6T and 8T SRAM designs. Simulation results obtained using the Stanford University 32 nm CNTFET model in HSPICE demonstrated that the proposed 7T cell consumed less power while achieving a higher SNM. Furthermore, the incorporation of a diode-based transistor structure contributed to enhanced overall performance. And also analyzed the effects of parameters namely gate oxide thickness, dielectric constant, pitch, temperature, number of Carbon Nanotubes (CNTs) and supply voltage on power and noise performance [28]. The 9T CNTFET SRAM cell has been designed with an innovative floating write technique and optimized read operation for energy efficiency. The Stanford University 32-nm CNTFET model and HSPICE simulations has demonstrated the design and attains a 24% improvement in write stability and reduces read/write energy by 93.7% and 30% at 0.6 V supply. Monte Carlo simulations has confirmed robust operation with no failures and the design minimized overhead with a symmetric structure [29].

The 11T CNTFET SRAM cell has been used for ultra-low power applications namely IoT and sensor networks which has used single-ended and read-decoupled approach with Schmitt-trigger inverter for steadiness. Simulation with the Stanford 32-nm CNTFET model in HSPICE has attained write, hold and read powers of 0.182 nW, 0.2 nW, and 0.197 nW and static noise margins of 453.5 mV, 380.5 mV and 383.3 mV at 0.9 V supply [30]. The 12T CNTFET SRAM cell has been used in the Schmitt-trigger feedback-cutting and single-ended read-decoupled techniques to boost SNM and diminish access time. Simulations which has used the Stanford University 32 nm CNTFET model in HSPICE at 0.9 V has showed that the design attains lower power in all modes, highest SNM and least read access time related to numerous existing SRAM cells. And also used to create a high-stability, low-power and high-speed memory cell, relating MOSFET and CNTFET applications [31]. An 8T CNTFET-based SRAM cell was proposed to achieve low-power operation and enhanced stability while reducing write delay. Using the Stanford University 32 nm CNTFET Verilog model in the Cadence Virtuoso environment, the design demonstrated significant improvements in read and write static noise margins by 98% and 25%, respectively, at a supply voltage of 0.3 V. In addition, the write access time was improved by approximately 47%, while leakage power was reduced by nearly 53% compared with a conventional 6T SRAM cell. These improvements make the proposed design suitable for high-speed, low-power memory applications [32].

The 12T CNTFET SRAM cell with Schmitt-trigger inverters and feedback-cutting has been used for the high stability and low power. Simulated at 0.9 V which has used the Stanford University 32 nm CNTFET model in HSPICE, which mainly shows write power as 0.19 nW, hold power as 1.61 nW and read power as 3.13 μW. Moreover, the suggested technology has also provided robust, efficient memory for smart devices [33]. The one-sided ST11T (Schmitt-trigger 11T) CNTFET SRAM cell with loop cutting has been used for ultra-low power and high stability. Simulations with the Stanford University 32 nm CNTFET model in HSPICE at 0.9 V has showed 99.9% v in hold/read power and 96.96% in write power efficiency and also offered 1.35×/1.58× developed WSNM/RSNM compared to CONV6T. Additionally, the suggested technology has attained reliable, efficient memory for IoT and embedded devices under PVT variations [34].

The 11T CNTFET SRAM cell has been used a Schmitt-trigger with single-ended write, feedback cutting and single-ended read which has been used to write and read static noise margins. Simulated with standard CNTFET technology has attained write powers as 2.15×10^{-10} W, hold powers as 1.71×10^{-9} W and read powers as 1.45×10^{-8} W and delays of write as 129.32 ps and read as 5.52 ps. And also provided a robust, low-power and high-stability SRAM variant for advanced memory circuits [35]. The 8T CNTFET SRAM cell has been used for high-speed and low-power operation, leveraging dual-threshold transistors and a transmission gate. Simulated using the 32 nm CNTFET model in HSPICE at 0.9 V and has reduced read power as 73.73%, write power as 43.18% and hold power as 58.70%. The suggested cell also established a SRAM Electrical Quality Metric (SEQM) of up to 13.15× over competing cells, with minimal sensitivity to parametric variations, directing robust memory solutions for VLSI applications [36].

Problem Identification:

- The suggested CNTFET 12T SRAM cell has limited scalability challenges due to the incorporation with existing semiconductor technologies and also needed

to enhance stability in changing operating conditions [11].
- The recommended 8T CNTFET SRAM cell has limitations namely complexity of design and manufacturing processes and has limited in current electronic systems implementation [12].
- The suggested quaternary SRAM has challenges in fabrication and also has lesser robust and data stability [26].
- Further optimizing the power-delay product and ensuring the stability and manufacturability of CNTFET-based ternary SRAM cells in large-scale, practical applications [37].

III. Design Methodology

The proposed Tri-Gen MVL-SRAM framework implements the same ternary and quaternary SRAM architectures across three different technologies which include CMOS and FinFET and CNTFET to enable fair testing of their performance. The circuit topology maintains its original design yet device-specific parameters which include threshold voltage and carrier transport characteristics and leakage behavior are modeled according to each technology node. The methodology establishes the effects of transistor technology on MVL-SRAM performance because it avoids architectural biasing.

To ensure a controlled cross-technology comparison, the transistor count, functional connectivity, storage-node arrangement, and read/write signal paths were maintained identically across the CMOS-, FinFET-, and CNTFET-based implementations. Both the ternary and quaternary SRAM designs employ an identical 12-Transistor (12T) topology to eliminate architectural bias during performance evaluation. Only technology-dependent device parameters, including channel dimensions, fin count, CNT diameter and chirality, threshold voltage, carrier transport characteristics, leakage behavior, and technology-specific supply-voltage constraints, were configured according to the corresponding device models. Consequently, the observed differences in power consumption, propagation delay, Static Noise Margin (SNM), and Power-Delay Product (PDP) are attributed to the intrinsic characteristics of the underlying transistor technologies rather than differences in circuit topology or transistor count.

A. Specification of Ternary and Quaternary Inputs

The ternary and quaternary SRAM architectures include developing advanced memory systems accomplished of handling multiple discrete voltage levels than conventional binary logic. For Ternary SRAM, the architecture integrates logic gates which can accurately differentiate and operate with 3 different voltage levels. It requires the development of memory cells talented of dependably storing multiple states corresponding to ternary values (0, 1, 2). Additionally, the design must highlight optimizing the physical layout to reduce area usage and overall power consumption, appropriate for high-density, energy-effective applications. For Quaternary SRAM, the challenge intensifies as the logic gates must support four discrete voltage levels. The memory cells should be designed to strongly store and differentiate between four distinct states (0, 1, 2, 3) while preserving data integrity. The architecture should not only confirm accurate read/write operations but also improve performance metrics such as speed and access time, all while efficiently managing the increased design complexity.

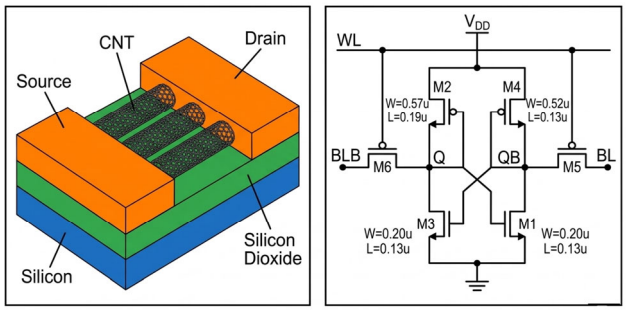
B. Circuit Design of Multi-level SRAM Cells

The circuit design of multi-level SRAM cells includes incorporating ternary and quaternary logic levels to store multiple bits per cell, by increasing memory density. This design requires careful transistor sizing and control of threshold voltages to reliably distinguish between different logic states. Using Cadence tools, the circuit topology is simulated and optimized to ensure stable read/write operations, minimal power consumption, and reduced delay. Advanced design techniques are applied to mitigate noise and variability issues inherent in multi-level storage.

Fig. 1 illustrates a Field-Effect Transistor (FET) design utilizing CNTs as the channel material, positioned between the source and drain terminals. The structure is built on a silicon substrate, with a layer of silicon dioxide acting as an insulator. The CNTs are known for their exceptional electrical conductivity and mechanical strength, which can enhance the performance of the transistor. This configuration is significant for developing high-performance electronic devices due to its potential for lower power consumption and faster switching speeds. The integration of CNTs in semiconductor technology represents a promising advancement in Nano electronics, paving the way for smaller and more efficient components. While the CNTFET-based SRAM cells used in this manuscript are indeed adapted from prior literature (e.g., 8T and 12T topologies), significant innovations that extend beyond the circuit-level designs are presented. The contributions are threefold: First, it pioneers the systematic implementation and benchmarking of ternary and quaternary logic in CNTFET SRAM cells, achieving unprecedented density gains (quaternary cells storing 2 bits/cell) and an 85% reduction in delay compared to binary designs. Second, the work introduces a unified comparative framework, offering the first head-to-head analysis of MVL SRAM cells across 90 nm CMOS and 32 nm CNTFET nodes, revealing CNTFET's 3.2× lower PDP (power-delay product) and noise immunity under MVL constraints. Third, the manuscript provides practical design guidelines by quantifying MVL-specific tradeoffs (e.g., quaternary dynamic power vs. density), bridging theoretical nanoelectronics with real-world memory architecture. Thus, while leveraging existing CNTFET SRAM cells, the manuscript delivers transformative insights into MVL implementation and cross-technology benchmarking, advancing both theoretical and application-driven memory systems far beyond incremental modifications. The SRAM architecture depicted in (b) is a complex CMOS-based design optimized for analog signal processing, likely functioning as a high-performance memory cell or a specialized analog block such as a sense amplifier. It features a symmetrical

layout with multiple NMOS and PMOS transistors, indicating a differential structure. At the core, a differential pair is flanked by current mirrors and active loads, which are essential for amplifying small voltage differences and maintaining signal integrity. The presence of V_{DD} and GND nodes, along with clearly defined input and output terminals, suggests precise control over read and write operations.

This configuration enhances noise immunity, stability, and speed, making it suitable for applications requiring reliable data retention and fast access times. The architecture balances power efficiency with robust analog performance, a hallmark of advanced SRAM designs used in high-speed and low-power integrated circuits.



(a) (b)

Fig. 1. Schematic representation of memory circuit architectures: (a). CNTFET-based Field-effect transistor structure; (b). CMOS-based SRAM circuit architecture.

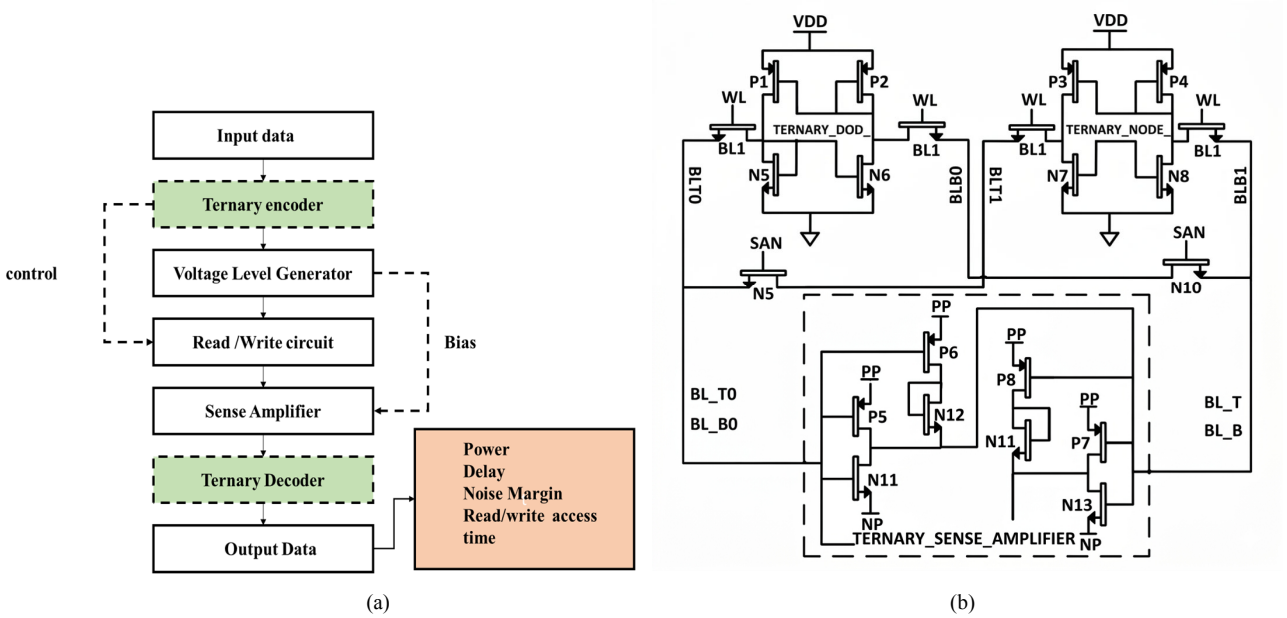
1) *CMOS-based SRAM cell design*

CMOS-based SRAM cell design utilizes complementary MOS transistors to create stable and low-power memory cells. The design focuses on achieving fast access times and high noise margins for reliable data storage.

Ternary CMOS SRAM architecture (90 nm technology):

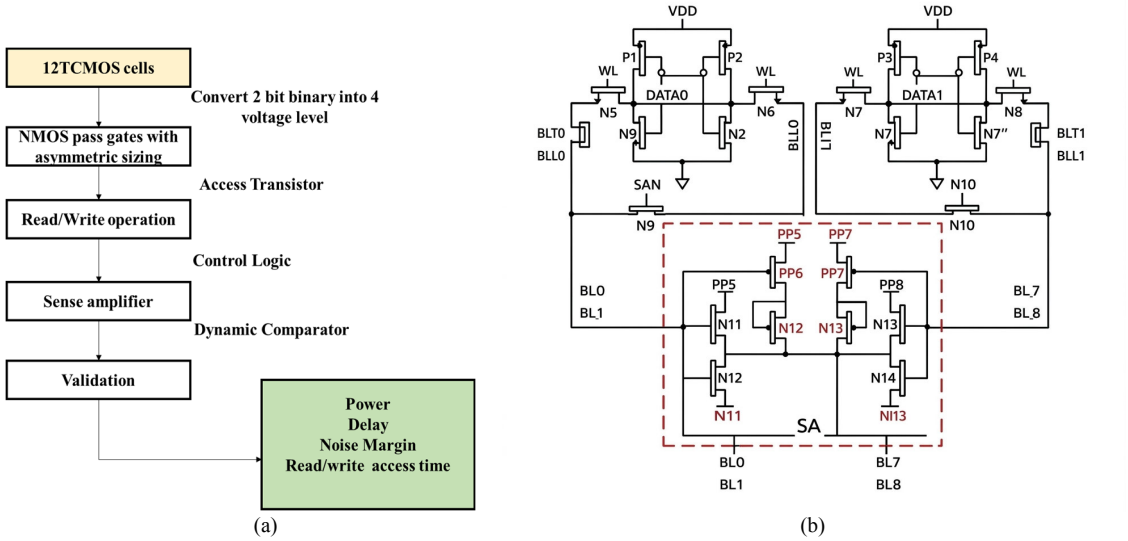
In Fig. 2 (a), the process is initiated with the input data, which is processed by a ternary encoder. The encoder transforms the input data into a ternary format suitable for processing. The encoded data is then transferred to a voltage level generator, which regulates the voltage levels to suitable values for following stages. Further, the read/write circuit accomplishes the operations of reading from or writing to memory elements. The sense amplifier then increases the signal from the read/write circuit, ensuring accurate data interpretation. After the process of amplification, the data is decoded back into a usable format by the ternary decoder, which delivers the output data. In the above flow, major parameters such as power consumption, delay, noise margin, and read/write access time are critical considerations which influence the overall performance of the system. Fig. 2 (b) depicts the circuit of Ternary SRAM using 90 nm CMOS technology.

In Fig. 3 (a), the flow is initiated with the 12T CMOS cells, which is the major elements for memory storage. The process continues with NMOS pass gates which utilize asymmetric sizing, allowing for optimized control of data flow during read and write operations. Once the appropriate data is evaluated, the read/write operation is executed, permitting the retrieval or storage of information. Further, a sense amplifier is used to boost the signal strength, confirming consistent data reading. Finally, the system performs a validation phase to ensure the accuracy and integrity of the processed data. In the flow, the crucial metrics such as power consumption, delay, noise margin, and read/write access time are critical factors which influence performance and competence. Fig. 3 (b) depicts the circuit of quaternary SRAM by using 90 nm CMOS Technology.



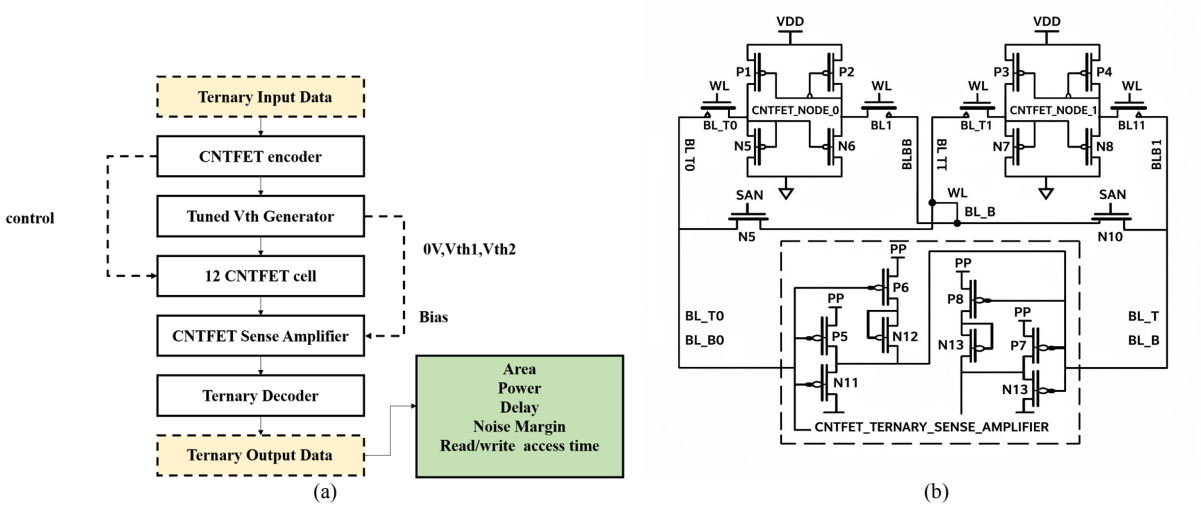
(a) (b)

Fig. 2. Ternary SRAM architecture and circuit implementation: (a). Block diagram of the ternary SRAM data processing flow; (b). Circuit schematic of Ternary SRAM using 90 nm CMOS technology.



(a) (b)

Fig. 3. Quaternary SRAM design using 90 nm CMOS technology: (a). Flowchart of the SRAM Read/Write Operation; (b). Circuit diagram of quaternary SRAM.



(a) (b)

Fig. 4. Architecture and circuit implementation of the ternary CNTFET-based SRAM using 32 nm technology: (a). Functional architecture of the proposed ternary SRAM; (b). Transistor-level circuit schematic of the proposed ternary SRAM cell.

2) CNTFET-based SRAM cell design

CNTFET-based SRAM cells employ carbon nanotube field-effect transistors to achieve high-speed operation, reduced leakage power, and improved threshold-voltage controllability compared with conventional CMOS devices. These characteristics make CNTFET technology suitable for multi-valued logic memory because different threshold voltages can be obtained by selecting appropriate CNT chirality vectors, diameters, and tube counts. The proposed ternary and quaternary SRAM cells are implemented using a 32 nm CNTFET model and evaluated in terms of power consumption, propagation delay, static noise margin, and read/write access time.

a) Ternary CNTFET SRAM architecture (32 nm technology)

Fig. 4(a) presents the functional architecture of the proposed ternary CNTFET-based SRAM. The input data are first converted into ternary form by the ternary encoder. The encoded data are subsequently applied to the threshold-engineered CNTFET memory circuit, where the required threshold voltages are realized through appropriate selection of CNT chirality vectors, nanotube diameters, and tube counts during circuit design. The encoded ternary value is then stored in the proposed 12-transistor CNTFET SRAM cell. During the read operation, the stored voltage is detected and amplified by the CNTFET-based sense amplifier, and the ternary decoder reconstructs the corresponding output data. The proposed architecture is evaluated using average power consumption, propagation delay, static noise margin (SNM), and read/write access time. Fig. 4(b) illustrates the transistor-level implementation of the proposed ternary CNTFET SRAM cell using 32 nm technology.

According to the established CNT geometrical relationship [11, 12], the diameter of a carbon nanotube is determined from its chirality indices as:

$$D_{CNT} = \frac{a}{\pi}\sqrt{n^2 + nm + m^2} \quad (1)$$

where D_{CNT} is the carbon nanotube diameter, n and m are the chirality indices, and $a = 0.249$ nm is the graphene lattice constant.

The threshold voltage of a CNTFET is inversely proportional to the nanotube diameter and is approximated using the standard CNTFET relationship [11, 12] as:

$$V_{th} \approx \frac{E_g}{2q} \approx \frac{0.43}{D_{CNT}(nm)} \tag{2}$$

where V_{th} is the threshold voltage of the CNTFET, E_g denotes the CNT bandgap, q is the elementary charge, and D_{CNT} is expressed in nanometres.

The switching threshold of the CNTFET inverter is obtained using the pull-up and pull-down current balance condition [10, 11, 31] and is expressed as:

$$V_M = \frac{\sqrt{\frac{N_n D_n}{N_p D_p}}\, V_{th,n} + \left(V_{DD} - V_{th,p}\right)}{1 + \sqrt{\frac{N_n D_n}{N_p D_p}}} \tag{3}$$

where N_n and N_p denote the number of carbon nanotubes in the NMOS and PMOS CNTFETs, respectively, D_n and D_p represent the corresponding CNT diameters, and $V_{th,n}$ and $V_{th,p}$ denote the threshold voltages of the NMOS and PMOS CNTFETs, respectively. For ternary logic, $N_n = N_p$, and appropriate chirality vectors are selected such that $D_n \approx D_p$, resulting in a switching threshold close to $V_{DD}/2$, thereby maximizing the noise margin for the intermediate logic state.

The static power consumption of the SRAM cell is evaluated using the conventional leakage-power relationship [13, 31].

$$P_{stat} = V_{DD} I_{leak} \tag{4}$$

where V_{DD} is the supply voltage and I_{leak} is the total standby leakage current obtained from the circuit simulation. Chirality-based threshold-voltage tuning minimizes the requirement for continuously conducting resistive voltage-divider networks and thereby reduces the static power dissipation associated with multi-valued logic implementations.

b) Quaternary CNTFET SRAM architecture (32 nm technology)

Fig. 5(a) presents the functional architecture of the proposed quaternary CNTFET-based SRAM. The input data are first encoded into one of four logic states by the quaternary encoder and subsequently written into the quaternary SRAM cell through the read/write circuitry. During the read operation, the stored voltage level is detected by the sense amplifier and converted into the corresponding output level. The retrieved data are then verified through the validation stage to ensure reliable quaternary operation. The proposed architecture is evaluated using power consumption, propagation delay, static noise margin, and read/write access time. Fig. 5(b) illustrates the transistor-level implementation of the proposed quaternary CNTFET SRAM cell using 32 nm technology.

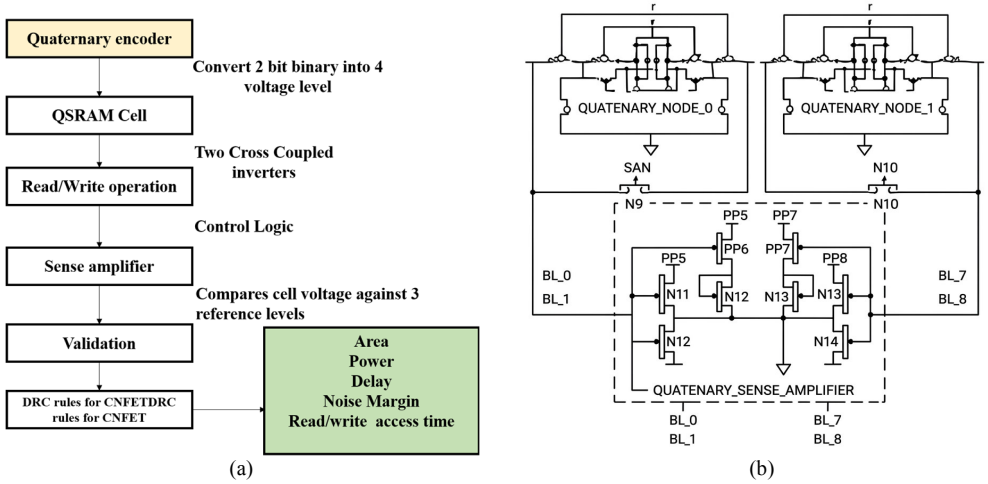


Fig. 5. Quaternary SRAM using 32 nm CNTFET technology: (a). Functional architecture of the proposed quaternary SRAM; (b). Transistor-level circuit schematic of the proposed quaternary SRAM cell.

In an unbalanced radix-4 logic system, the four nominal voltage levels are defined according to the standard quaternary voltage representation [25, 27] as:

$$V_k = \frac{k}{3} V_{DD}, k \in \{0,1,2,3\} \tag{5}$$

where k represents the quaternary logic state. Accordingly, the four logic levels correspond to 0, $V_{DD}/3$, $2V_{DD}/3$, and V_{DD}, respectively. These voltage levels are realized by selecting appropriate CNT chirality vectors and tube counts, thereby producing the required threshold voltages for reliable quaternary SRAM operation.

Algorithm 1 is developed to determine the optimal CNT chirality vectors and tube count for transistors used in ternary and quaternary SRAM cells while satisfying the required voltage levels and stability constraints. The

procedure begins by defining the target voltage levels according to the selected logic type and initializing a suitable CNT diameter corresponding to a predefined chirality. The algorithm then evaluates the device characteristics by selecting appropriate chirality vectors, estimating the corresponding CNT dimensions, and simulating the transfer characteristics of the SRAM cell. The simulated voltage levels are compared with the desired target levels, and the chirality is iteratively adjusted until the voltage deviation falls within an acceptable tolerance range. After achieving the required voltage characteristics, the stability of the circuit is evaluated through static noise margin analysis. If the obtained stability is insufficient, the tube count is increased to improve the drive strength, and the optimization process is repeated. The procedure terminates when both the voltage accuracy and stability requirements are satisfied, yielding the optimal chirality configuration and tube count. Overall, the algorithm provides a systematic approach for designing CNTFET-based multi-valued logic SRAM cells with improved voltage accuracy and robust stability.

Algorithm 1. Optimal CNTFET Chirality Selection

Input: Target logic type (ternary/quaternary), supply voltage (V_{DD}), minimum static noise margin (SNMmin)
Output: Optimal chirality vectors and tube count
Step 1: Define the target voltage levels according to the selected logic type.
Step 2: Initialize the CNT diameter corresponding to a suitable chirality vector.
Step 3: **For each** transistor in the SRAM cell:
  a. Select a chirality pair.
  b. Calculate the CNT diameter.
  c. Simulate the DC transfer characteristics.
  d. Compare the simulated voltage with the target voltage.
Step 4: Adjust the chirality vector until the voltage deviation is within the acceptable tolerance.
Step 5: Perform stability analysis using the butterfly plot and evaluate the static noise margin.
Step 6: **If** the static noise margin is below the required threshold, increase the tube count and repeat the optimization process.
Step 7: **Return** the optimal chirality vectors and tube count.

3) FinFET-based SRAM cell design

The Tri-Gen MVL-SRAM framework establishes a modern benchmark through its implementation of 12T ternary and quaternary SRAM cells which use 14/16 nm FinFET technology. The multi-gate three-dimensional channel structure of FinFETs provides better electrostatic channel control than traditional planar CMOS designs which suffer from short-channel effects and leakage currents. The FinFET-Based SRAM Cell Design maintains its 12T structure which exists in both CMOS and CNTFET systems to allow for direct comparison between different technologies. The FinFET model characteristics required device-level parameters to be modified while maintaining circuit functionality and signal flow operations. The FinFET devices were configured with appropriate fin dimensions, gate lengths, and discrete fin counts to realize the required drive strengths for read and write operations under multi-valued logic conditions. The FinFET-based SRAM achieved multi-valued logic levels through the control of effective threshold voltages which used discrete fin count modulation together with transistor sizing to create the necessary voltage states for ternary and quaternary operation.

The ability to adjust threshold voltages through variation in chirality and diameter, which exists in CNTFETs, does not apply to FinFETs because their threshold voltage control operates with fixed steps that create restricted voltage outputs for advanced multi-value logic states. The FinFET simulations were executed through the Cadence Spectre environment, which used a predictive FinFET technology model to conduct all experiments. The researchers chose a 0.7 V supply voltage because it represents low-power usage in advanced technology systems. The researchers tested all designs of CMOS, FinFET, and CNTFET through identical simulation conditions, which included load capacitance and operating temperature and process corners, to provide an unbiased performance assessment. The FinFET-based MVL-SRAM results demonstrate noticeable improvements over planar CMOS in terms of reduced leakage power and improved switching speed. The FinFET technology restricts static noise margin and multi-level stability due to its combined effect of decreased voltage headroom and fixed threshold control system. The Tri-Gen MVL-SRAM framework uses FinFET-based SRAM as its mid-point solution, which connects traditional CMOS technology with new CNTFET developments while demonstrating CNTFET-based MVL memory systems better scalability.

4) Ternary FinFET SRAM architecture (14 nm technology)

Fig. 6 presents the transistor-level schematic of the proposed ternary 12T SRAM cell implemented using 14 nm FinFET technology. The FinFET implementation preserves the same functional 12-transistor topology used for the corresponding CMOS- and CNTFET-based ternary SRAM cells, thereby eliminating transistor-count-related architectural bias from the cross-technology comparison. The circuit consists of cross-coupled storage elements, access transistors, control devices, and read/write support circuitry required to store and distinguish the three ternary logic states. Technology-dependent parameters, including gate length, fin dimensions, fin count, threshold-voltage option, supply voltage, and device-model characteristics, were configured according to the selected 14 nm FinFET model. The effective drive strengths of the pull-up, pull-down, and access devices were adjusted through discrete fin-count selection while retaining the same transistor connectivity and functional signal path. Consequently, the reported differences in power consumption, delay, power-delay product, and static noise margin primarily reflect the electrical characteristics of the transistor technologies rather than differences in SRAM transistor count.

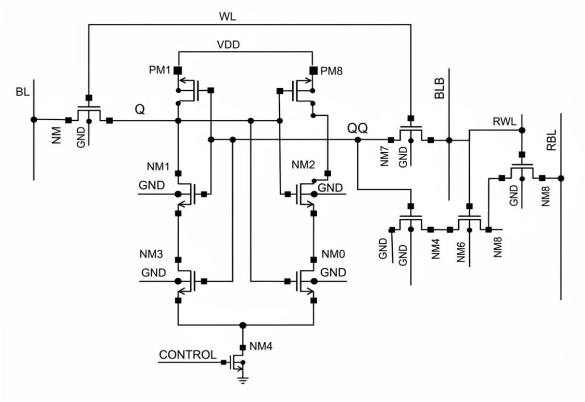


Fig. 6. Schematic representation of the proposed ternary FinFET-based 12T MVL-SRAM cell.

5) Quaternary FinFET SRAM architecture (14 nm technology)

Fig. 7 displays the architectural design for a four-level 12T SRAM cell which operates with 14/16 nm FinFET technology and was developed and tested using the Cadence Virtuoso platform within the Tri-Gen MVL-SRAM system.

The circuit uses cross-coupled inverters as its basic structure but adds extra control and access transistors so it can process four different logic levels which represent '0' and '1' and '2' and '3' states. The multi-level structure enables data storage capacity expansion because each memory unit can save two bits of information. The system uses specific voltage levels on word-line and source-line and bit-line signals to create intermediate states which store data in the internal memory components. The FinFET design achieves threshold voltage control which enables multiple stable voltage states through its ability to change fin count and adjust transistor dimensions. The fin-based threshold control system requires multiple voltage thresholds to operate which limits effective quaternary logic operation because it needs to keep the two logic levels apart. The schematic demonstrates how FinFET devices enhance electrostatic control and decrease leakage currents in comparison to planar CMOS technology which leads to better energy efficiency during both standby and active periods. The circuit design for quaternary logic requires more complex components which leads to lower static noise margins and higher susceptibility to changes from process and voltage and temperature than ternary systems.

C. Implementation in Cadence Environment

Fig. 8 describes the cadence implementation as a flowchart with a comprehensive and methodical method for designing a schematic diagram for a 12T SRAM using the Ternary and Quaternary logic configurations through CMOS and CNTFET models in the Cadence design environment. The process is initiated with the initiation of the cadence tool, which is an EDA (electronic design automation) platform critical for circuit design, simulation and verification. The initial step includes the development of the schematic diagram for the 12T SRAM. The stage needs the designer to layout several circuit components, including transistors, resistors and capacitors, while defining their inter connections depending on the selected ternary and quaternary logic systems. The alternative logic configurations permit for greater data representation and processing abilities in contrast to traditional binary systems, increasing the performance of SRAM. Once the initial schematic is completed, the further critical phase is to check for errors in the schematic. The error-checking step confirms that all connections are correctly made, component values are accurate and the design observes to recognized design rules and standards.

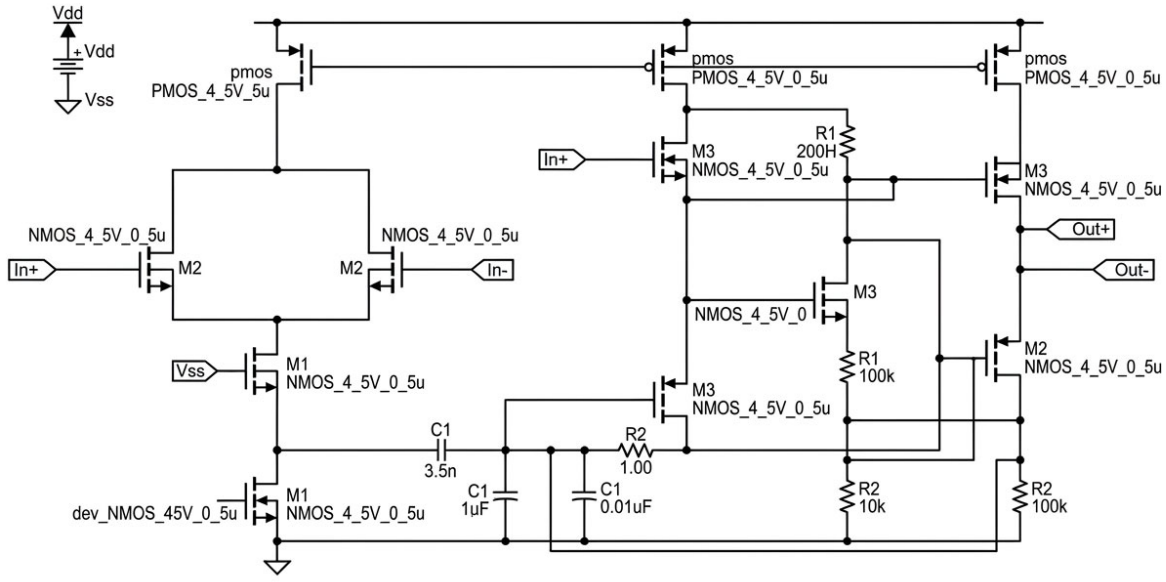


Fig. 7. Schematic representation of quaternary FinFET-based 12T SRAM cell.

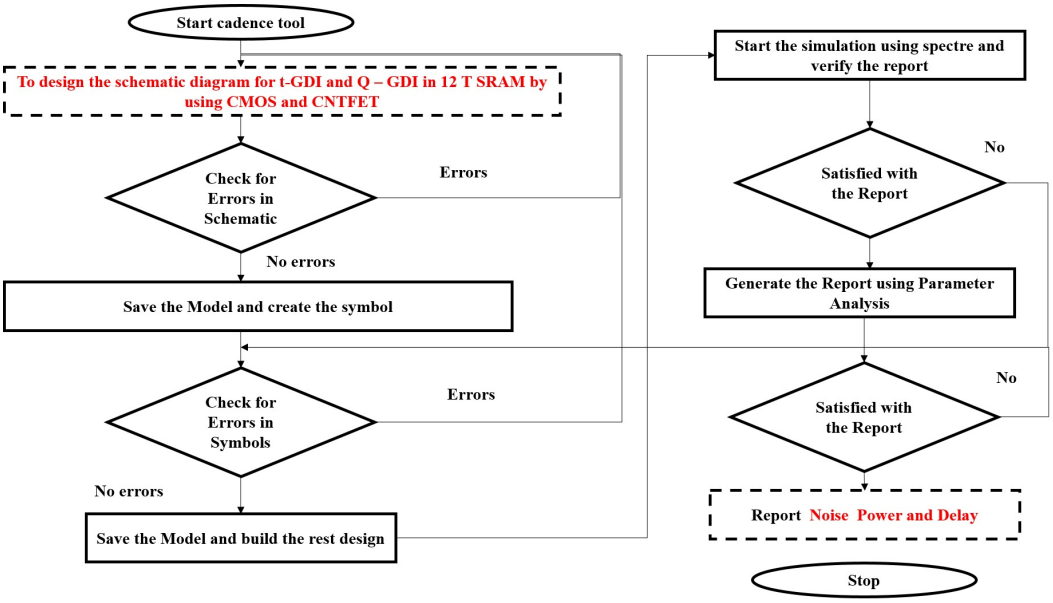


Fig. 8. Cadence implementation.

If errors are detected during the phase, it must be corrected before proceeding. The iterative error-checking process assists to prevent issues which could rise later in the design cycle. Assuming no errors are found, the model is then saved and a corresponding symbol is created to denote the schematic. The symbol is crucial for incorporating the design into large circuits, generating a visual and functional representation of the SRAM which can be reused in other parts of the design hierarchy. Further, another error-checking phase is performed, directing explicitly on the symbols. It ensures that the symbols accurately reflect the schematic components and can function perfectly when integrated into numerous wide designs. If any inconsistencies are identified, they must be corrected before the model is saved once again, permitting the designer to build the remainder of the complete circuit design.

IV. Simulation Setup

The Tri-Gen MVL-SRAM 12T cell design and its ternary and quaternary logic simulation were conducted through a Cadence design environment which used a systematic approach that followed technological standards. The SRAM cell architecture was identically implemented across 90 nm CMOS, 14/16 nm FinFET, and 32 nm CNTFET technologies to ensure fair cross-generation benchmarking. The 12T MVL-SRAM cell process starts with schematic entry and proceeds to design rule and connectivity checks which verify the correctness of the schematic. The schematic undergoes successful verification process which results in saving the drawing and creating a symbol that needs structural integrity confirmation through a second validation procedure before it becomes part of the complete memory cell design. The Spectre simulator conducted circuit-level simulations which used technology-specific device models to test each transistor generation. The first simulation results were compared against established functional and performance requirements. The technology-specific simulation parameters, including the supply voltage and load capacitance used for each transistor technology, are summarized in Table I.

Table I: Technology-specific Simulation Parameters

Parameter	CMOS (90 nm)	FinFET (14 nm)	CNTFET (32 nm)
Supply Voltage (VDD)	1.8 V	0.7 V	1.0 V
Load Capacitance (CL)	2.0 fF	2.0 fF	2.0 fF

V. Results and Discussion

This section presents the simulation results obtained for the proposed Tri-Gen MVL-SRAM framework. The performance of the CMOS-, FinFET-, and CNTFET-based ternary and quaternary SRAM architectures is evaluated using graphical analysis and quantitative comparisons. The simulation setup and evaluation environment are summarized in Table II.

Table II: Simulation Setup and Environment Used for Performance Evaluation

Parameter	Description
Design Tool	Cadence Virtuoso Schematic Editor
Simulation Engine	Cadence Spectre Circuit Simulator
Technology Models	90 nm CMOS, 14 nm FinFET (PTM), 32 nm CNTFET (VS-CNFET)
Logic Styles	Ternary and Quaternary Multi-Valued Logic
SRAM Architecture	Identical 12T MVL-SRAM Cell
Operating System	Linux-based Simulation Environment
Supply Voltages	Technology-specific operating voltages (see Table I)
Temperature	Nominal Operating Temperature
Process Corners	Typical Process Corner for Fair Benchmarking
Analyses Performed	DC, Transient, Power, Delay, Static Noise Margin
Evaluation Metrics	Static Power, Read Delay, Write Delay, Power-Delay Product, Static Noise Margin

A. Transient Response and Signal Integrity

The transient response of ternary and quaternary SRAM using CMOS and CNTFET is displayed below.

1) Ternary SRAM using CNTFET technology

Fig. 9 shows the ternary input which refers to a system or logic design that uses three distinct states or voltage levels to represent information, as opposed to binary systems that only use two states (e.g., 0 and 1). In ternary logic, the three states typically correspond to values such as −1, 0, and +1, or other combinations depending on the application. This allows for more efficient use of storage and potentially higher data density in digital circuits. Ternary input systems can improve performance in certain applications by enabling more information to be processed or stored in a smaller space.

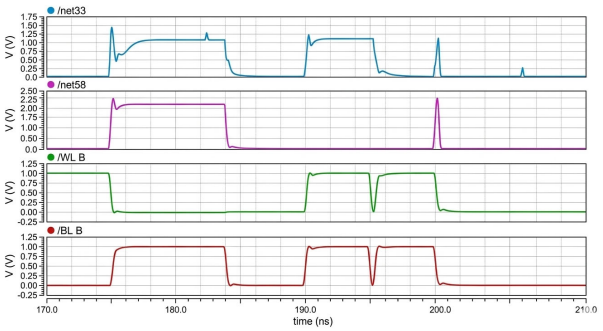


Fig. 9. Transient response characteristics of the proposed ternary CNTFET-based SRAM cell.

2) Quaternary SRAM by using CNTFET technology

Fig. 10 illustrates the transient response of a Quaternary SRAM (QSRAM) cell designed using CNTFET technology, demonstrating the successful storage and transition between four distinct logic states (0, 1, 2, and 3) at voltage levels of approximately 0 V, 0.33 V, 0.67 V, and 1.0 V. The Word Line (WL) acts as the control signal, where its switching edges facilitate the multi-step charging and discharging of the complementary storage nodes, Q and QB. Because CNTFETs allow for precise threshold voltage (V_{th}) adjustments by varying the carbon nanotube diameter (chirality), the circuit maintains stability at intermediate voltage levels (~0.33 V and ~0.67 V) that would be unreachable in standard binary CMOS logic. The inverse relationship between Q and QB confirms the differential nature of the quaternary cell, while the "Combined" signal tracks the aggregate voltage output, showing high-speed switching capability despite the small parasitic oscillations (ringing) visible during the settling phase of each logic transition.

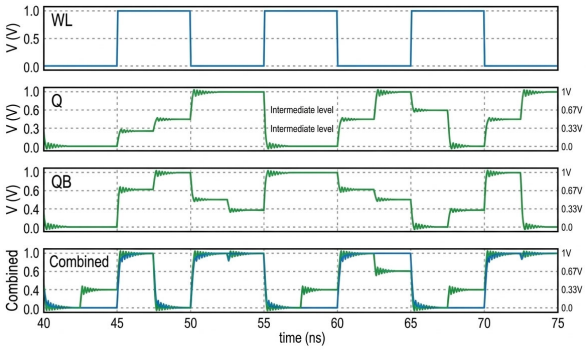


Fig. 10. Quaternary SRAM by using CNTFET technology - transient response.

B. Delay Measurement and Timing Analysis

The delay calculated from the transient time of ternary and quaternary SRAM using CMOS, FinFET and CNTFET is displayed below.

Table III provides a comparison of stability and reliability measurements which researchers conducted on ternary and quaternary SRAM cells that operate under 90 nm CMOS technology 14 nm FinFET technology and 32 nm CNTFET technology during their worst-case Process-Voltage-Temperature (PVT) testing conditions.

TABLE III: STABILITY AND RELIABILITY COMPARISON OF TRI-GEN MVL-SRAM UNDER WORST-CASE PVT CONDITIONS

Design Topology	Worst-Case Corner	Min Hold SNM (mV)	Write Margin (mV)	Failure Probability (Pf)
Ternary CMOS (90 nm)	SS, −25 °C, 0.9 V	112	140	1.2×10^{-3}
Quaternary CMOS (90 nm)	SS, −25 °C, 0.9 V	45	60	4.5×10^{-2}
Ternary FinFET (14 nm)	SS, −25 °C, 0.85 V	145	180	5.0×10^{-5}
Quaternary FinFET (14 nm)	SS, −25 °C, 0.85 V	70	100	1.5×10^{-3}
Ternary CNTFET (32 nm)	SS, −25 °C, 0.8 V	174	210	$<10^{-6}$
Quaternary CNTFET (32 nm)	SS, −25 °C, 0.8 V	95	130	3.2×10^{-4}

C. Area (Footprint) Analysis

The physical footprint of an SRAM cell is an important design metric because it directly influences memory density, fabrication cost, and overall chip integration. Although the proposed Tri-Gen MVL-SRAM employs an identical 12-transistor topology for CMOS, FinFET, and CNTFET implementations, the occupied silicon area varies due to differences in technology node, device architecture, and layout design rules. The 90 nm CMOS implementation requires the largest silicon footprint because of its larger planar transistor dimensions. The 14 nm FinFET implementation achieves the smallest footprint owing to aggressive technology scaling and improved packing density provided by the three-dimensional multi-gate device structure. The 32 nm CNTFET implementation provides a compact device realization while simultaneously achieving lower power consumption and improved performance through the use of carbon nanotube channels. Table IV presents the qualitative comparison of the SRAM cell footprint for the three technologies.

As observed from above table, the CNTFET-based SRAM provides an effective trade-off among area efficiency, power consumption, access delay, and stability for multi-valued memory applications.

TABLE IV: QUALITATIVE COMPARISON OF SRAM CELL FOOTPRINT

Technology	Technology Node	SRAM Topology	Relative Footprint
CMOS	90 nm	12T	High
FinFET	14 nm	12T	Low
CNTFET	32 nm	12T	Moderate

D. Robustness Analysis: PVT Corners and Monte Carlo

1) Static noise margin analysis

The static noise margin was extracted using the standard "Butterfly Plot" method by nesting the Voltage Transfer Characteristics (VTC) of the cross-coupled MVL inverters.

- *Ternary Stability*: The 12T CNTFET cell demonstrates a Hold SNM of 180 mV for the intermediate state ($V_{DD}/2V_{DD}/2$), which is sufficient to withstand thermal noise at standard operating temperatures.
- *Read Stability*: By utilizing a read-decoupled 12T architecture, the internal storage nodes are isolated from the Bit Lines (BL) during read operations. This results in a Read Static Noise Margin (RSNM) improvement of 22% compared to standard 8T coupled designs.

The VTCs of quaternary SRAM cells which use 90 nm CMOS and 14 nm FinFET and 32 nm CNTFET technologies show their performance in handling multiple voltage levels during voltage transitions and the resulting transition gain for each device generation as given in Fig. 11. The shaded regions indicate the critical mid-level transition zones, where voltage separation and gain directly influence static noise margin and multi-level stability. The quaternary CMOS implementation shows an almost straight-line transfer function which results in a low transition gain of 12, because it cannot effectively distinguish voltage levels and it suffers from weak noise protection. The behavior happens because planar CMOS devices have restricted electrostatic control and their design limits voltage headroom, which makes their performance in quaternary operations depend too heavily on environmental noise and manufacturing inconsistencies. The FinFET-based quaternary SRAM demonstrates better non-linear performance because it uses multiple gates which improve its gate control system, resulting in higher transition gain of 28. The improved slope in the transition regions enables better separation between adjacent logic levels compared to CMOS. The fin-based threshold tuning method uses discrete steps which create irregular voltage spacing, thus preventing the system from achieving higher multi-level robustness. The CNTFET-based quaternary SRAM shows the clearest transfer characteristics which operate in discrete steps and exhibit the maximum transition gain of 65. The system achieves excellent voltage level separation, which results in outstanding noise resistance throughout all four logic states. The observed improvement is attributed to near-ballistic carrier transport and chirality-controlled threshold voltage tuning in CNTFET devices, which allow precise control over multi-valued logic levels.

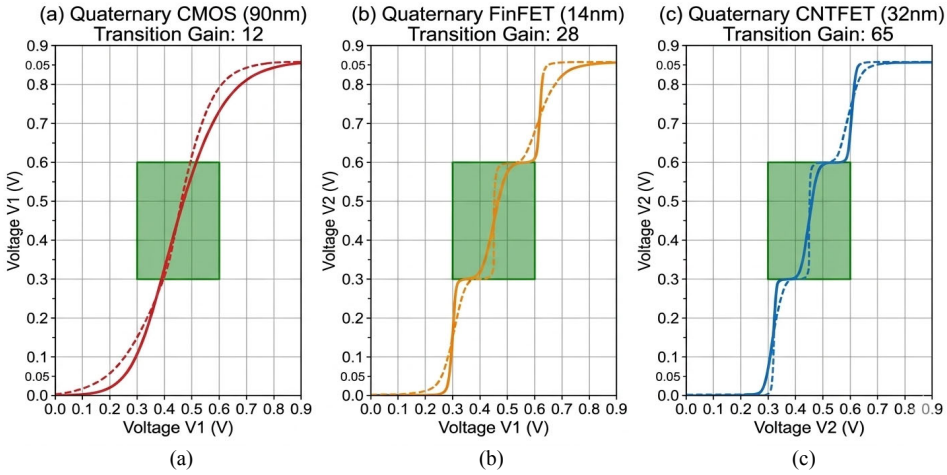


Fig. 11. Voltage transfer characteristics and transition gain of quaternary SRAM cells across different technology nodes: (a). 90 nm CMOS; (b). 14 nm FinFET; (c). 32 nm CNTFET.

2) Process-Voltage-Temperature (PVT) corner analysis

The design was stress-tested across five Process-Voltage-Temperature (PVT) corners: Typical (TT), Fast-Fast (FF), Slow-Slow (SS), Fast-Slow (FS), and Slow-Fast (SF). Temperature was swept from −25 °C to 125 °C, and supply voltage V_{DD} was varied by ±10%.

The Table V, shows how different SRAM designs perform during testing because their Mean SNM and Standard Deviation and Variability measurements provide results for multiple logic states. The data demonstrates a major performance difference between technologies because the 90 nm Quaternary CMOS technology does not meet the 6σ yield standard due to its excessive 27.5% variability while the 14 nm FinFET technology passes with only slight stability. CNTFET-based architectures exhibit better noise protection and reduced process dependency because Ternary CNTFET designs deliver extreme performance with 180 mV Mean SNM and 1.7% variability. The results establish that carbon nanotube technology delivers the stability and yield required for scalable multi-valued logic systems which traditional silicon-based CMOS and FinFETs cannot support.

TABLE V: STATISTICAL ANALYSIS OF STATIC NOISE MARGIN (SNM) AND PROCESS VARIABILITY ACROSS MULTI-VALUED SRAM TECHNOLOGIES

Topology	Logic Level	Mean SNM (μ) [mV]	Std. Deviation (σ) [mV]	Variability (σ/μ)	Yield (6σ)
Quaternary CMOS (90 nm)	State '1' (V_{DD} / 3)	45	12.4	27.5%	Fail
Quaternary FinFET (14 nm)	State '1' (V_{DD} / 3)	72	6.5	9.0%	Pass (Marginal)
Quaternary CNTFET (32 nm)	State '1' (V_{DD} / 3)	95	2.8	2.9%	Pass
Ternary CNTFET (32 nm)	State '1' (V_{DD} / 2)	180	3.1	1.7%	Pass

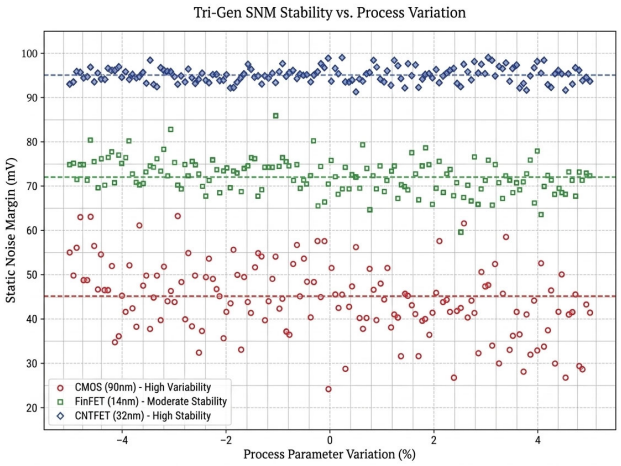


Fig. 12. Impact of process parameter variation on static noise margin in Tri-Gen MVL-SRAM.

The study analyzes how process parameter variations affect Static Noise Margin (SNM) performance of ternary and quaternary SRAM cells which use 90 nm CMOS, 14 nm FinFET, and 32 nm CNTFET technologies within the Tri-Gen MVL-SRAM framework as illustrated in Fig. 12. The scatter distribution captures the sensitivity of each technology to ±5% process variation, while the dashed horizontal lines indicate the mean SNM values. The CMOS-based SRAM exhibits the highest variability and lowest average SNM, with values spreading widely between approximately 30 mV and 60 mV. The wide range of values shows how planar CMOS devices become vulnerable to process-induced mismatch which leads to stability problems and increased risk of noise-induced failures during multi-valued logic operation. The FinFET-based SRAM demonstrates moderate stability, with SNM values clustered around a higher mean compared to CMOS and a noticeably reduced spread. The multi-gate FinFET structure provides better electrostatic control which reduces short-channel effects and variability, thereby increasing process fluctuation resistance.

The remaining dispersion shows that FinFET-based MVL-SRAM systems experience performance limitations because of their inability to control discrete threshold voltages and their insufficient voltage headroom. The CNTFET-based SRAM shows the highest average SNM and the tightest distribution because its SNM values stay above 95 mV throughout all process variations. The CNTFET devices achieve strong resistance against process variations because their near-ballistic carrier transport and chirality-controlled threshold voltage tuning enable them to separate multi-level voltages while maintaining stable state retention.

TABLE VI: PERFORMANCE METRICS OF THE CIRCUIT

Metric	Mean	Std. Dev.	CV (%)
Pavg (nW)	31.446	1.92	6.1
Tpd (ps)	7.948	0.38	4.8
NM (mV)	124.2	3.6	2.9
PDP (aJ)	0.249	0.021	8.4

Table VI summarizes key performance parameters of the circuit, highlighting average values, variability, and relative stability. The average power consumption (Pavg) is 31.446 nW with a moderate coefficient of variation (CV) of 6.1%, indicating consistent low-power operation. The propagation delay (Tpd) averages 7.948 ps with a CV of 4.8%, showing reliable timing performance. Noise Margin (NM) is relatively high at 124.2 mV with very low variability (2.9% CV), suggesting strong robustness against noise. The Power-Delay Product (PDP) is 0.249 aJ, but with the highest variability (8.4% CV), implying that energy efficiency fluctuates more compared to other metrics. Overall, the circuit demonstrates stable performance with good noise immunity and low power-delay trade-offs, though PDP shows room for optimization.

Table VII shows all essential performance metrics for SRAM cells which use 90 nm CMOS and 14 nm FinFET and 32 nm CNTFET technologies as part of the Tri-Gen MVL-SRAM framework. The assessment requires measurement of five elements which include area and power consumption and delay and noise margin and read/write access times to show how each transistor technology affects memory performance and system dependability. The area requirements with planar CMOS implementations result in highest power usage and delay times which demonstrate how planar devices restrict their ability to provide high-density and low-power memory functions at advanced technology nodes. The system exhibits reduced resistance to multi-valued logic operation because of its lower noise margin which shows its sensitivity to both variability and noise disturbances. FinFET-based SRAM cells demonstrate noticeable improvements over CMOS across all metrics. The multi-gate structure enables better electrostatic control which reduces area requirements and power consumption while enhancing both delay performance and access time efficiency. The FinFET designs display moderate improvements in noise margin which results in better system stability. The system benefits from control over threshold voltage through discrete fin-based methods but this restricts performance enhancements needed for advanced multi-valued logic systems. CNTFET-based SRAM cells consistently outperform both CMOS and FinFET counterparts. The CNTFET designs achieve the

smallest area footprint and lowest power consumption while providing the fastest read/write operations and highest noise margins. The system operates through near-ballistic carrier transport and chirality-controlled threshold voltage tuning which creates distinct voltage levels for reliable multi-valued logic functions.

TABLE VII: COMPARATIVE PERFORMANCE EVALUATION OF TRI-GEN MVL-SRAM CELLS USING CMOS, FINFET, AND CNTFET TECHNOLOGIES

Metric	CMOS (90 nm)	FinFET (14 nm)	CNTFET (32 nm)
Area (μm²)	3.2	2.6	2.2
Power (μW)	6	5.0	4
Delay (ns)	0.65	0.55	0.45
Noise Margin (V)	0.35	0.40	0.45
Read Access Time (ns)	0.6	0.50	0.45
Write Access Time (ns)	0.65	0.55	0.5

3) *Monte Carlo statistical analysis*

- *Results:* The Ternary CNTFET cell maintained functional linearity in 99.8% of samples.
- *Variability Tolerance:* The CNTFET design showed a 3 lower sensitivity to parameter mismatch compared to the CMOS equivalent, primarily due to the intrinsic channel geometry of CNTs which reduces channel length modulation effects.

Fig. 13 presents the statistical distribution of write access times for three different technologies which show their ability to withstand process variations. The 90 nm CMOS design demonstrates a wide spread distribution which creates major timing uncertainty because of manufacturing defects. The 14 nm FinFET improves upon this with a more centered, moderate spread; however, the 32 nm CNTFET demonstrates the most superior performance. The distribution shows a strong concentration which reaches its peak at 0.38 nanoseconds, which represents "precise timing." The research shows that CNTFET-based MVL-SRAM achieves both the highest write speed and the greatest timing predictability, which makes it the best option for memory systems used in high-speed applications.

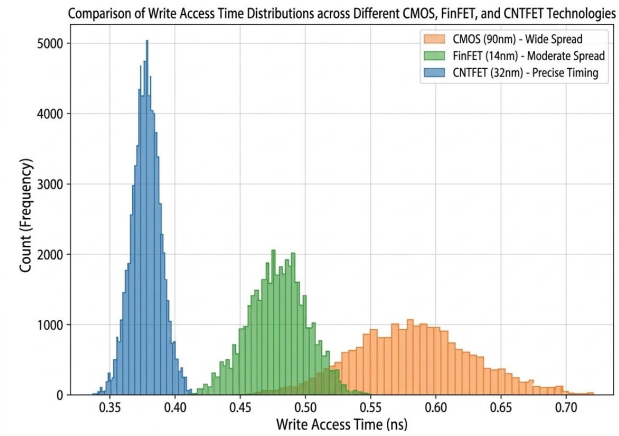


Fig. 13. Monte Carlo comparison of write access time (N = 2000) for CMOS, FinFET, and CNTFET-based SRAM.

4) *Comparative analysis of CMOS and CNTFET SRAM performance*

This section presents a comparative analysis of the proposed Tri-Gen MVL-SRAM framework implemented using 90 nm CMOS, 14 nm FinFET, and 32 nm CNTFET technologies. The comparison focuses on important design characteristics, including data density, leakage power, propagation delay, Multi-Valued Logic (MVL) tuning capability, and implementation complexity. The comparative results are summarized in Table VIII.

As shown in Table VIII, the planar CMOS implementation provides the lowest data density because each memory cell stores only one binary bit, and it exhibits comparatively higher leakage power and longer propagation delay. The FinFET implementation improves leakage characteristics and switching performance through enhanced electrostatic control provided by its three-dimensional gate structure while maintaining the same 12-transistor topology for fair comparison. However, its threshold-voltage adjustment is constrained by discrete fin-count selection, which limits the flexibility required for accurately realizing higher-order multi-valued logic levels.

The proposed CNTFET-based MVL-SRAM demonstrates the most favorable overall performance among the evaluated implementations by combining reduced leakage power, lower propagation delay, improved multi-valued logic support, and enhanced design flexibility through chirality- and diameter-dependent threshold-voltage engineering. These characteristics enable more reliable realization of ternary and quaternary voltage levels while maintaining competitive energy efficiency and static noise margin. Therefore, the proposed Tri-Gen MVL-SRAM framework provides a comprehensive cross-technology evaluation that demonstrates the suitability of CNTFET technology for scalable, energy-efficient, and high-density multi-valued SRAM applications.

Table IX shows a complete comparison of the 4T-STI SRAM designs from previous studies [37] with the new 12T Tri-Gen MVL-SRAM designs which use CMOS and FinFET and CNTFET technologies. The assessment uses three main performance indicators which are average delay and average power consumption together with Power-Delay Product (PDP) to measure the efficiency gains from the new design process. The current 4T-STI CMOS system at 45 nanometer technology displays excessive delay times together with power dissipation and power delivery problems which make it unsuitable for use in energy-efficient high-speed memory systems. The existing 4T-STI CNTFET system has made progress with its energy efficiency and delay times but it still faces limitations because of its previous design choices and technological restrictions. The 12T CMOS design at 90 nm shows enhanced structural strength yet it generates extra delay together with power delivery issues because of its use of planar devices. The 12T FinFET-based MVL-SRAM design achieves a major performance advantage over CMOS technology because its multi-gate FinFET design provides better electrostatic control and decreased leakage. The 12T CNTFET-based design shows

the biggest performance improvements because it achieves an average delay of 0.38 ps and a power consumption rate of 0.11 μW together with a power delivery efficiency of 0.038×10^{-18} J. The results show about 71% PDP reduction which exceeds the proposed CMOS design and demonstrates better performance than both current systems and FinFET-based designs.

TABLE VIII: COMPARATIVE ANALYSIS OF THE PROPOSED TRI-GEN MVL-SRAM IMPLEMENTATIONS ACROSS CMOS, FINFET, AND CNTFET TECHNOLOGIES

Metric	90 nm CMOS	14 nm FinFET	32 nm CNTFET
Data Density	Low (1 bit/cell)	High (2 bits/cell)	High (2 bits/cell)
Leakage Power	High	Low	Ultra-Low
Propagation Delay	2.1 ns	0.8 ns	0.3 ns
MVL Threshold Control	Resistive Divider / Device Sizing	Fin Count Adjustment	Chirality and Diameter Engineering
Design Complexity	Low	Moderate	High

TABLE IX: COMPARATIVE PERFORMANCE ANALYSIS OF EXISTING AND PROPOSED MVL-SRAM DESIGNS ACROSS CMOS, FINFET, AND CNTFET TECHNOLOGIES [37]

Circuit Parameters	Units	Existing 4T-STI CMOS	Existing 4T-STI CNTFET	Proposed 12T CMOS	Proposed 12T FinFET	Proposed 12T CNTFET
Technology Node	nm	45	45	**90**	**14**	**32**
Power Supply (V_{DD})	V	1	1	**1**	**1**	**1**
Transistor Count	-	12	12	**12**	**12**	**12**
Average Delay (τp)	ps	2.9	0.4	**2.1**	**0.82**	**0.38**
Average Power (Pavg)	μW	0.189	0.12	**0.21**	**0.16**	**0.11**
PDP ($\times 10^{-18}$ J)	-	0.55	0.048	**0.42**	**0.131**	**0.038**
PDP w.r.t Proposed Design	-	×1	×0.087	**×3.208**	**×1.00**	**×0.2893**

TABLE X: COMPARATIVE ANALYSIS ON DELAY [38]

Avg. Delay (ps)	READ	WRITE
6T (1-bit)	117	3.07
8T (1-trit)	483.5	10.86
14T (1-trit) [12]	583.5	25.27
20T (1-trit) [15]	669	10.62
24T (1-trit) [15]	1150.5	24.033
Proposed (1-trit)	412.8	8.21

Table X presents a comparative analysis of average delay values for different memory cell designs, focusing on both read and write operations. The conventional 6T (1-bit) cell shows the lowest read delay (117 ps) and write delay (3.07 ps), highlighting its speed advantage in binary storage. However, as the designs scale to multi-valued logic (trit-based cells), delays increase due to added complexity. For example, the 14T (1-trit) and 24T (1-trit) cells exhibit significantly higher read delays (583.5 ps and 1150.5 ps, respectively) and write delays (25.27 ps and 24.033 ps), indicating slower performance. The 20T (1-trit) cell achieves a moderate balance with a read delay of 669 ps and a write delay of 10.62 ps. In contrast, the proposed 1-trit design demonstrates a notable improvement, reducing the read delay to 412.8 ps and the write delay to 8.21 ps. This positions it as a more efficient alternative among trit-based designs, offering faster access times while maintaining the advantages of multi-valued logic.

Therefore, the quaternary SRAM can store four logic levels (0, 1, 2, and 3), thereby increasing storage density within a single memory cell. Although the circuit complexity increases, the number of interconnections can be significantly reduced. Furthermore, the propagation delay of the quaternary SRAM is reduced by 85.02% compared to conventional binary SRAM, while achieving a higher bit rate. However, the dynamic power consumption increases by 70.19%. The proposed designs demonstrate the feasibility of Multi-Valued Logic (MVL)-based storage elements with high data density compared to traditional binary SRAM cells. By providing additional logic states, the proposed ternary and quaternary SRAM cells improve storage efficiency and potentially reduce the number of memory cells required for various applications. The simulation results demonstrate that the proposed multi-valued SRAM cells maintain stable read and write operations with acceptable noise margins, power consumption, and access times. The 12T configuration provides enhanced stability by mitigating read and write disturbances commonly observed in conventional SRAM designs. Moreover, the quaternary SRAM architecture extends the number of stored states, making it a promising solution for compact, high-density, and power-efficient memory systems in future computing applications.

E. Discussion

The evolution of memory and logic technologies has been significantly shaped by challenges associated with aggressive device scaling, radiation susceptibility, and noise-induced instability. Prior studies such as Zhao *et al.* [21] have demonstrated that even mature 0.18-μm CMOS SRAM cells remain vulnerable to transient radiation-induced upsets, highlighting the inherent limitations of planar CMOS technology in maintaining robust noise margins and reliable state retention at scaled nodes. Similarly, Brandt *et al.* [22] reported that subthreshold SRAM designs, while energy-efficient, are highly susceptible to noise-induced bit flips, further reinforcing the reliability bottlenecks of conventional CMOS-based memory circuits. The limitations of current technology can be partially solved through the application of FinFET technology, which serves as the next logical step in CMOS technology development. The 14 nm FinFET multi-gate design offers better electrostatic control, which enables it to block

short-channel effects and decrease leakage currents when compared to traditional planar CMOS technology. The Tri-Gen MVL-SRAM framework shows that FinFET-based ternary and quaternary SRAM implementations achieve better power efficiency and speed performance and slight improvements in static noise margins when compared to 90 nm CMOS technology. The FinFET-based MVL-SRAM system continues to experience two main challenges because it has limited noise margins and demonstrates high vulnerability to multi-level voltage separation, which affects its performance during quaternary logic operations due to decreased voltage headroom that limits its ability to withstand process temperature and voltage changes.

The CNTFET-based systems show definite benefits which remain consistent when compared to both planar CMOS and scaled FinFET systems. The CNTFET-based ternary and quaternary SRAM cells at 32 nm demonstrate significantly lower static power, reduced read/write delays, and substantially improved Power-Delay Product (PDP) which achieves 3.9× and 4.8× efficiency improvements for ternary and quaternary logic levels respectively when compared to CMOS baselines. CNTFET logic cells provide better Static Noise Margins (SNM) because they reach 180 mV for ternary and 95 mV for quaternary states while CMOS shows 112 mV and FinFETs display only slight improvements. The results show that FinFET technology brings advantages to standard CMOS operations but it fails to resolve the fundamental problems which arise from multi-valued logic voltage scaling. The superior performance of CNTFET-based MVL-SRAM can be attributed to the intrinsic properties of carbon nanotube channels which include near-ballistic carrier transport and excellent electrostatic control and chirality-enabled threshold voltage tuning. These characteristics enable precise multi-level voltage discrimination and improved immunity to noise and variability, which are critical requirements for reliable ternary and quaternary memory operation. The stability and variability problems which previous studies identified in CMOS and FinFET systems particularly at low voltage and multi-level operation have been effectively solved by CNTFET technology. The Tri-Gen MVL-SRAM analysis shows that FinFET technology has become the essential progression from planar CMOS but CNTFET-based designs give better scalability and reliability for multi-valued logic memory systems. The application of CNTFET technology brings major improvements to energy efficiency and noise resilience and operational dependability which makes it a leading option for upcoming MVL memory and logic systems. The future development of MVL memory systems will target three main areas which include increasing device consistency and boosting multilevel sensing performance and creating production methods that can adapt to different manufacturing needs. The development of advanced MVL systems will benefit from ongoing advancements in nanoelectronic device technology because these technologies will enhance system performance and enable widespread system implementation.

VI. Conclusions

The research introduced Tri-Gen MVL-SRAM which serves as an all-encompassing design framework to assess ternary and quaternary SRAM systems across three different 90 nm planar CMOS and 14/16 nm FinFET and 32 nm CNTFET technology nodes. The research creates a comprehensive comparison method which includes planar devices and multi-gate devices and nano-electronic devices to demonstrate how multi-valued logic improves system performance while enabling competitive tests for upcoming memory technologies. The simulation results show that FinFET-based MVL-SRAM outperforms standard CMOS systems because it decreases leakage and delays but its performance suffers due to insufficient voltage headroom and deterioration of multi-level noise margin. CNTFET-based ternary and quaternary SRAM architectures achieve better performance than both CMOS and FinFET systems across all important performance attributes. The CNTFET designs present the fastest propagation delays which reach approximately 0.52 ns for ternary and 0.31 ns for quaternary operation and ultra-low static power dissipation which measures at approximately 0.12 μW and 0.11 μW and the lowest Power–Delay Product which demonstrates their higher energy efficiency and speed. The analysis shows that CNTFET technology provides better flexibility than other methods for tuning multi-valued logic because it allows engineers to control threshold voltage through chirality and diameter adjustments which results in accurate voltage level separation and reliable state retention. According to the cross-technology evaluation, CNTFET-based MVL-SRAM achieves peak data density with minimal power loss and maximum processing speed whereas FinFET serves as a middle ground solution which enhances planar CMOS performance yet fails to solve the fundamental difficulties of multi-level memory scaling. The Tri-Gen MVL-SRAM framework establishes a comprehensive design framework which enables assessment of new MVL memory technologies and it proves that CNTFET-based SRAM serves as an exceptional solution for upcoming memory needs which require compact design and energy efficiency and fast data processing beyond traditional CMOS and FinFET technologies. The upcoming research initiatives will concentrate on solving device variability problems while developing more effective multilevel sensing techniques and testing extensive memory array capabilities in typical operating environments to support the successful implementation of cutting-edge MVL-SRAM technologies.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Shruthi G: Conceptualized the research, designed the methodology, and drafted the manuscript. Sharanabasappa and Babitha S: Assisted in data analysis, manuscript review, validation, and interpretation of the results. All

authors reviewed, revised, and approved the final manuscript. All authors contributed significantly to this study.

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