

Design and Optimization of OTA for Biomedical Applications Using EAVOA Bio-Inspired Algorithms

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Abstract—The paper presents an efficient design method for the sizing of an advanced analog circuit. Numerous researchers have been attracted to the field of biomedical devices, specifically the design of cochlear implants. The use of a cochlear implant enables individuals with hearing loss to receive stimulation of the cochlear nerve. A cochlear implant plays a crucial role in processing incoming signals. The low power consumption and efficient processing of biological signals by an Operational Transconductance Amplifier (OTA) make it ideal for biomedical applications. This paper presents a comparative analysis of two OTA designs optimized for biomedical applications using bio-inspired algorithms. The first case study explores a Split-Folded Cascode (SFC) amplifier for cochlear implants, while the second examines a preamplifier circuit for neurological signal processing. Various state-of-the-art bio-inspired algorithms, including the enhanced version of the African Vulture Optimization Algorithm (EAVOA), Hybrid Whale Particle Swarm Optimization (HWPSO), and other algorithms, are employed to optimize performance metrics such as gain, input noise, power, and area minimization for both case studies. Simulation results demonstrate that EAVOA outperforms other algorithms by achieving high gain, low noise, and reduced power dissipation, which have been validated through Cadence Virtuoso simulations.

Index Terms—Cochlear implants, Enhanced African Vultures Optimization Algorithm (EAVOA), global optimization, Split Folded Cascode (SFC), two-stage OTA

I. INTRODUCTION

The development of high-performance front-end circuits for biomedical applications presents unique challenges, particularly in intensifying weak bio-signals with amplitudes in the microvolt (μV) range and operating frequencies below 20 kHz [1]. One of the widely popular biomedical circuits is the cochlear implant, a wonderful medical technological advancement that helps people with acute hearing problems by applying direct stimulation at the acoustic neuroma. The most important component of these devices is the amplifier, which processes incoming sound waves and amplifies them before transferring them to the auditory nerve. A

sound processor and an electrode array are additional crucial components. The cochlear implant amplifier's overall efficacy and functioning are mostly determined by its design [2].

The block diagram of a biomedical amplifier is given in Fig. 1. In Fig. 1, the transconductance G_m signifies the operational transconductance amplifier (OTA), while C_{in} and C_f are input DC-blocking capacitors and feedback capacitors, respectively. M_{f1} and M_{f2} are used as pseudo-resistors.

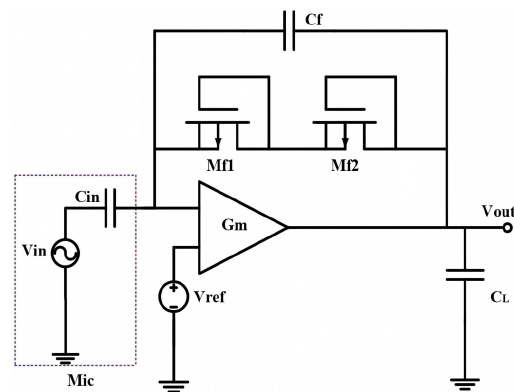


Fig. 1. Block diagram of a biomedical closed-loop amplifier [2].

As critical components of biomedical systems such as cochlear implants and neurological amplifiers, OTAs must simultaneously meet stringent requirements: high gain, ultra-low noise, and minimal power consumption, while maintaining compact physical dimensions suitable for implantable devices [3, 4]. The obligation to minimize circuit area stems not only from spatial constraints in medical implants but also from manufacturing cost considerations. However, indiscriminate transistor scaling risks degrading essential performance measures such as gain, bandwidth, and noise etc. [5], creating a complex optimization challenge. Manually sizing transistors has traditionally been the go-to method in analog circuit design, but it often turns out to be both time-consuming

and inefficient—especially when dealing with the complex trade-offs involved in balancing multiple performance targets [6]. However, advancements in the realm of bio-inspired and evolutionary computing have opened up new avenues for improving the design of these amplifiers.

Because bio-inspired algorithms imitate the flexible and efficient behaviors found in natural systems, they provide a novel solution to challenging optimization problems [7, 8]. These algorithms have demonstrated striking efficacy in handling a wide variety of engineering problems, including pattern recognition, control systems design, and optimization. They take inspiration from biological phenomena such as genetic evolution, neural networks, and swarm intelligence [9]. Bio-inspired algorithms present a possible opportunity to leverage the principles underlying biological hearing systems to enhance the efficacy and efficiency of the amplification process while constructing cochlear implant amplifiers [10, 11]. Bio-inspired algorithms application in related fields, including auditory signal processing and brain prosthetics, to learn more about their applicability and effectiveness for improving cochlear implant amplifiers [12]. By comparing several bio-inspired optimization algorithms, the aim is to ascertain the most effective approaches for addressing the unique requirements and constraints of cochlear implant amplifier design.

Over the years, various optimization approaches, such as Particle Swarm Optimization (PSO) [13], and various other variants like Differential Evolution Particle Swarm Optimization (DEPSO) [14], human behavior-based particle swarm optimization (HBPSO) [15], Differential Evolution (DE) [16], hybrid whale particle swarm optimization (HWPSO) [17], Dragonfly Algorithm (DA) [18], whale optimization algorithm (WOA) [19], Salp Swarm Algorithm (SSA) [12], League Championship Algorithm (LCA) [20], African Vultures Optimization Algorithm (AVOA) [21], have been applied to amplifier design with some success. However, these methods tend to struggle with certain issues: they converge slowly, can easily get stuck in local optima, and often are not very effective when it comes to managing multiple design goals at once [12–28]. While a lot of existing research has tackled optimization for high-frequency applications [29–31] there's been surprisingly little attention given to the unique needs of low-frequency biomedical systems such as neural amplifiers [32–42]. In particular, one of the most important challenges in this area, minimizing circuit area, hasn't been explored as thoroughly as it should be. In the design of cochlear implant amplifiers, there has also been no reported work on the use of bio-inspired algorithms. Although there have been quite a few state-of-the-art works in the conventional design of cochlear implants. Some of the reported works include those by Ryoo *et al.* [43], Devi *et al.* [44], Oh *et al.* [45], and Croce *et al.* [46]. However, the major limitation in these works is the noise-power trade-off in the design. One of the recently reported works is by Nath *et al.* [2], wherein they reported a cochlear implant amplifier using Split

Folded Cascode (SFC) topology. However, the main limitation of their work is that the reported area is higher, and because of manual computation, it is a time-consuming process. The purpose of this paper is to study and analyze the use of bio-inspired algorithms to minimize the area in biomedical amplifier design, considering two case studies: firstly, a cochlear implant design using the split-folded cascode topology, and secondly a neurological amplifier design using two-stage OTA topology [47, 48]. The objective function has been formulated as the summation of the width and length of all the transistors in the circuit, and the constraints are defined by modelling both circuits so as to formulate the dependency of every design specification on a particular width and length. Simulations have been performed using various state-of-the-art bio-inspired algorithms, and a comparative analysis among them is performed [12–25, 49–53] based on simulations and validation. The results demonstrate that the enhanced African vulture optimization algorithm (EAVOA) outperforms most state-of-the-art algorithms when it comes to achieving a minimum area by delivering optimal design specifications for both circuits. The study utilized the 180-nanometer process technology for the validation of the design aspects of the Cadence Virtuoso simulation software tool for circuit design. The results indicate that the approach employed is effective, and it is in very close agreement with algorithmic suggestions.

The remaining paper is organized as follows: Section II of the paper discusses the problem formulation of Case Study 1 and Case Study 2. In Section III, we explain bio-inspired optimization algorithms. In Section IV, highlight the analysis of the detailed results. Finally, in Section V, the conclusion has been presented.

II. PROBLEM FORMULATION

In this section, the problem formulation or design procedure of the proposed approach for both case studies is presented in detail. These design procedures define the various constraints, the optimum design specifications imposed on the transistor dimensions, and have to be met accordingly while minimizing the desired cost function for optimal performance.

A. Case Study: 1 Split-Folded Cascode (SFC)-based Cochlear Implant Amplifier

The Split Folded Cascode (SFC) amplifier [2] is selected for cochlear implant applications due to its high gain and bandwidth. This topology incorporates split input transistors and cascoded current mirrors to achieve superior transconductance. Using the folded cascode OTA architecture, which self-compensates and permits reduced supply margins, the first stage of the proposed preamplifier was designed. The device uses the conventional folded cascode design, which consists of a split input transistor and a folded transistor with the same aspect ratio [2]. By doing this, the amplifier's total transconductance will increase, and the current will be divided into two branches. This arrangement makes using

low-bias current to obtain adequate gain easier, which lowers power consumption. The split folded cascode is shown in Fig. 2. The split input transistors M_{1a} , M_{1b} , M_{2a} , and M_{2b} show that two transistors are coupled rather than one. Two folded transistors, designated as M_{5a} , M_{5b} , M_{6a} , and M_{6b} , are also connected to balance the splitting. Reducing the size, capacitance, and parasitic resistance in the backend architecture while maintaining the same performance is achieved by splitting at a lower aspect ratio. Connected to scale the current are resistances R_2 , R_3 , R_4 , and R_5 . With less current flowing through them, their design results in reduced noise levels. Here, the normal current mirror is substituted with the cascode current mirror load in order to boost the gain. To give a high output swing, a folded cascode requires an extra transistor, the M_{13} , because its output swing is moderate.

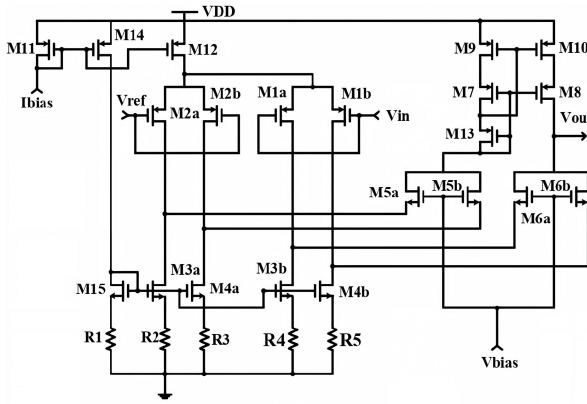


Fig. 2. Split folded cascode amplifier [2].

The area of the Cochlear Implants amplifier can be computed by taking into account the multiplication of the dimensions {width (W_k) and Length (L_k)} of all the transistors. The SFC OTA area minimization problem statement has been defined below. The Cost Function (CF) for area minimization is defined by Eq. (1). The design constraints formulated by Eq. (2) to Eq. (18) must be satisfied while ensuring that the area is optimized. The minimum desired specifications of the circuit are affected by these constraints and have been formulated by various modelling and analysis of the circuit, such as small-signal, large-signal, frequency, noise analysis, etc. (W/L), and I_D refers to the aspect ratio and drain current of the corresponding transistors.

Cost function (CF)

$$CF = \text{Area} = \sum_{k=1}^{15} W_k L_k \quad (1)$$

Slew rate (SR)

$$I_{D12} = SR \times C_L \quad (2)$$

where C_L is the load capacitor. Eq. (2) represents the single-ended slewing condition. For a fully differential folded cascode OTA, the effective Slew Rate is given by $SR = 2I_{bias}/C_L$, since both output branches contribute to charging and discharging the load capacitance. This distinction is important to avoid confusion when comparing single-ended and differential implementations.

$$\left(\frac{W}{L}\right)_{4a} = \frac{2I_{D4a}}{K_n V_{DS4a}^2} = \left(\frac{W}{L}\right)_{3a} \quad (3)$$

where K_n is the transconductance parameter of NMOS, and V_{DS} is the drain-to-source voltage.

$$\left(\frac{W}{L}\right)_{4b} = \frac{2I_{D4b}}{K_n V_{DS4b}^2} = \left(\frac{W}{L}\right)_{3b} \quad (4)$$

$$\left(\frac{W}{L}\right)_{6a} = \frac{2I_{D6a}}{K_n V_{DS6a}^2} = \left(\frac{W}{L}\right)_{5a} \quad (5)$$

$$\left(\frac{W}{L}\right)_{6b} = \frac{2I_{D6b}}{K_n V_{DS6b}^2} = \left(\frac{W}{L}\right)_{5b} \quad (6)$$

$$V_{DS4a}(\text{sat}) = V_{DS6a}(\text{sat}) = \frac{V_{out}(\text{min}) - |V_{SS}|}{2} \quad (7)$$

where $V_{DS}(\text{sat})$ is the drain-source voltage at saturation, $V_{out}(\text{min})$ is the minimum output voltage, and V_{SS} is the negative supply voltage.

$$V_{DS4b}(\text{sat}) = V_{DS6b}(\text{sat}) = \frac{V_{out}(\text{min}) - |V_{SS}|}{2} \quad (8)$$

$$\left(\frac{W}{L}\right)_{10} = \frac{2I_{D10}}{K_n V_{DS10}^2(\text{sat})} \quad (9)$$

$$\left(\frac{W}{L}\right)_8 = \frac{2I_{D8}}{K_n V_{DS8}^2(\text{sat})} \quad (10)$$

$$V_{DS8}(\text{sat}) = V_{DS10}(\text{sat}) = \frac{V_{DD} - V_{out}(\text{max})}{2} \quad (11)$$

where V_{DD} is the positive supply voltage, and $V_{out}(\text{max})$ is the maximum output voltage.

$$\left(\frac{W}{L}\right)_{1a} = \left(\frac{W}{L}\right)_{2a} = \frac{g_{m1a}^2 (K+1)}{K_p 2I_{D3a}} \quad (12)$$

where K_p is the transconductance parameter of PMOS, g_m is the transconductance of the corresponding transistors, and K is the current gain factor.

$$\left(\frac{W}{L}\right)_{1b} = \left(\frac{W}{L}\right)_{2b} = \frac{g_{m1b}^2 (K+1)}{K_p 2I_{D3b}} \quad (13)$$

$$\left(\frac{W}{L}\right)_{12} = \frac{2I_{D12}}{K_p \left[V_{DD} - V_{CM}(\text{max}) - \sqrt{\frac{2I_{D3}}{K_p (W/L)_{1a}}} - V_{tp} \right]^2} \quad (14)$$

where $V_{CM}(\text{max})$ is the maximum common-mode input voltage, and V_{tp} is the threshold voltage of PMOS.

$$\left(\frac{W}{L}\right)_{4a} = \left(\frac{W}{L}\right)_{3a} = \frac{2I_{D4a}}{K_n \left[V_{CM}(\text{min}) - |V_{SS}| + V_{tp} \right]^2} \quad (15)$$

where $V_{CM}(\text{min})$ is the minimum common-mode input voltage. Overall gain of the split-folded cascode amplifier.

$$A_v = g_{m1a} g_{m1b} g_{m6a} g_{m6b} r_{o6a} r_{o6b} \left(r_{o1} \parallel r_{o1b} \parallel r_{o5} \parallel R_4 \right) \parallel (g_{m8} r_{o8} r_{o10}) \quad (16)$$

where r_o is the output impedance, and R_4 is the resistance. Input-referred thermal noise spectral density, $S_n(f)$:

$$S_n(f) = \frac{8KT}{g_{m1a}^2} \left(\frac{g_{m1a}}{3} + \frac{1}{R_1} + \frac{2g_{m9}}{3} + \frac{2g_{m13}}{3} \right) \quad (17)$$

where K and T are the Boltzmann constant and absolute temperature, respectively.

Power dissipation

$$P = (V_{DD} + \|V_{SS}\|)(I_{D12} + I_{D9} + I_{D10}) \quad (18)$$

B. Case Study 2: Two-Stage OTA-based Neurological Amplifier Design

Fig. 3 indicates the schematic for a two-stage OTA [54]. This circuit consists of a first-stage differential pair and a current mirror load. This configuration can help minimize common-mode noise. The following arrangement provides a common-source gain stage capable of producing an overall high gain. In this circuit, the current mirror load is composed of M_3 and M_4 , while the input differential pair for the circuit is composed of M_1 and M_2 . The common source driver and load are labeled as M_6 and M_7 . The 1st and 2nd stages are connected to a Miller compensation capacitor (C_c). This helps in improving the stability and Phase Margin of the OTA [55]. The Phase Margin (PM) greater than 60 degree criterion is utilized in selecting the appropriate Miller compensation capacitor (C_c), to determine the load capacitor C_L defined in Eq. (19).

$$C_c > 0.22C_L \quad (19)$$

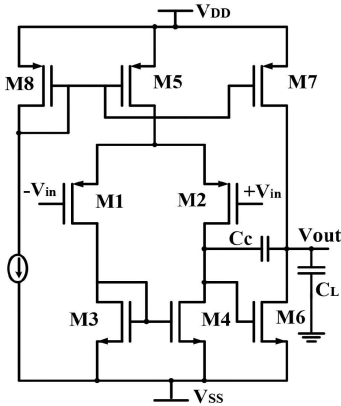


Fig. 3. Two-Stage OTA [54].

This choice of compensation capacitor C_c doesn't consider the inherent power and noise tradeoffs in the circuit design, which is a vital design norm of biomedical amplifier design [1]. The choice of the compensation capacitor C_c plays a significant role in determining the power and noise of the OTA. A reduction in noise with a high C_c will lead to higher power dissipation. That's why the best C_c is required to be selected for optimal performance. In response to this requirement, Mahatanakul & Chutichatuporn [56] proposed a two-step OTA design modelling that is regarded as a constraint while also maximizing value of both the intentional cost functions outlined in Laskar *et al.* [17].

As mentioned earlier, the problem formulation statement provided an outline for the area minimization

of the Two-Stage OTA, which is given below. The cost function for area minimization is defined in Eq. (20), while design constraints for minimizing the area are formulated in Eqs. (21) to (35).

$$\text{Minimize CF} = \sum_{k=1}^8 W_k L_k \quad (20)$$

Input-referred thermal noise spectral density $S_n(f)$:

$$S_n(f) = \frac{16KT}{3\omega_u C_c} \left[1 + \frac{\text{SR}}{\omega_u (V_{\text{HR}}^{\text{CM}} - V_{\text{tn}} + V_{\text{tp}})} \right] \quad (21)$$

where ω_u is the unity-gain frequency, and $V_{\text{HR}}^{\text{CM}}$ is the headroom voltage for ICMR (input common-mode range) of the op-amp. The second term assumes that the input-referred noise is limited primarily by dynamic current starvation, while flicker noise contributions are negligible under the chosen biasing conditions.

$$I_{D7} = \text{SR} (C_c + C_L) \quad (22)$$

$$L_6 = \sqrt{\frac{3\mu_n V_{\text{HR}}^{\text{out}} C_c}{2\omega_u (C_c + C_L) \tan(\phi_M)}} \quad (23)$$

where $V_{\text{HR}}^{\text{out}}$ is the headroom output voltage for the output swing of the op-amp, μ_n is the mobility for NMOS, and ϕ_M is the phase margin.

$$W_6 = \frac{2 \times \text{SR} \times (C_c + C_L) L_6}{\mu_n C_{\text{ox}} (V_{\text{HR}}^{\text{out}})^2} \quad (24)$$

where C_{ox} is the gate-oxide capacitance per unit area.

$$I_{D5} = \text{SR} \times C_c \quad (25)$$

$$\left(\frac{W}{L} \right)_{1,2} = \frac{\omega_u^2 C_c}{\mu_p C_{\text{ox}} \times \text{SR}} \quad (26)$$

where μ_p is the mobility for PMOS.

$$\left(\frac{W}{L} \right)_{5,8} = \frac{2 \times \text{SR} \times C_c}{\mu_p C_{\text{ox}} \left(V_{\text{HR}}^{\text{CM}} - V_{\text{tp}} - \frac{\text{SR}}{\omega_u} \right)^2} \quad (27)$$

$$\left(\frac{W}{L} \right)_7 = \left(\frac{C_c + C_L}{C_L} \right) \left(\frac{W}{L} \right)_{5,8} \quad (28)$$

$$\left(\frac{W}{L} \right)_{3,4} = \frac{\left(\frac{W}{L} \right)_6 \left(\frac{W}{L} \right)_{5,8}}{2 \left(\frac{W}{L} \right)_7} \quad (29)$$

Power dissipation

$$P = \text{SR} \times (3C_c + C_L) (V_{DD} - |V_{SS}|) \quad (30)$$

Overall gain of two-stage OTA

$$A_v = \frac{2g_{m1}g_{m6}}{I_{D5}I_{D6}(\lambda_n + \lambda_p)^2} \quad (31)$$

where the channel length modulation parameters for NMOS and PMOS are λ_n and λ_p , respectively.

$$V_{HR}^{CM+} = V_{DD} - V_{CM}(\max) \quad (32)$$

$$V_{HR}^{CM-} = V_{CM}(\min) - |V_{SS}| \quad (33)$$

$$V_{HR}^{out+} = V_{DD} - V_{out}(\max) \quad (34)$$

$$V_{HR}^{out-} = V_{out}(\min) - |V_{SS}| \quad (35)$$

III. BIO-INSPIRED OPTIMIZATION ALGORITHMS

Bio-inspired algorithms are algorithms [12–21] that use biological systems and processes as a source of inspiration to solve difficult optimization and search problems. To solve a variety of issues across several fields, these algorithms imitate the behavior of natural systems like swarm intelligence, evolution, or neural networks. These days, bio-inspired algorithms address application problems from several scientific and technical domains, such as information processing, optimization, and decision-making [12]. It is projected that several approaches and fields will create intelligent optimization algorithms in the next few years that will be more adept at managing diverse difficulties for anomaly and failure detection domains. Optimization is essential when applying deterministic or stochastic methods to tackle more single- or multi-objective issues. Extensions and improvements to meta-heuristic optimization techniques are the goal of NP-hard problem-based algorithms, both deterministic and stochastic. Bio-inspired algorithms are more enhanced, flexible, intelligent, and easy to test than traditional techniques.

Bio-inspired algorithms are being used these days to solve issues quickly in various areas, such as robotics, computer networks, image processing, electrical and mechanical challenges, electronics, management, planetary science, and production engineering. Because bio-inspired algorithms are a novel topic, the authors hope to explore the debate surrounding and potential applications of these algorithms. One of the newer techniques (AVOA) [21] is based on how vultures behave in the wild when searching for food. It works decently in many scenarios, but it's not without issues—it can be slow to find good solutions, sometimes gets stuck too early in local optima, and struggles more with complicated or high-dimensional problems. The enhanced AVOA algorithm would seek to enhance the exploitation and exploration balance [57, 58]. Some traditional AVOA, such as classical AVOA [59, 60], multi-strategy AVOA [61], multi-objective AVOA [62], and recent advancements [63, 64], are based on AVOA.

To improve on this, an enhanced version, called enhanced AVOA (EAVOA), was introduced [65]. This version adds a few new ideas to make it work better. First, we have the Representative Vulture Selection Strategy (RVSS), which picks the most promising search agents smartly so that the algorithm can explore and exploit them efficiently. Then there's the Rotating Flight Strategy (RFS), which adds variety to the search by mimicking how vultures fly in circles—this helps the algorithm avoid getting stuck in the same place. Thirdly,

the Selecting Accumulation Mechanism (SAM) is used to make use of good solutions found earlier, so the process becomes faster and more focused as it proceeds further.

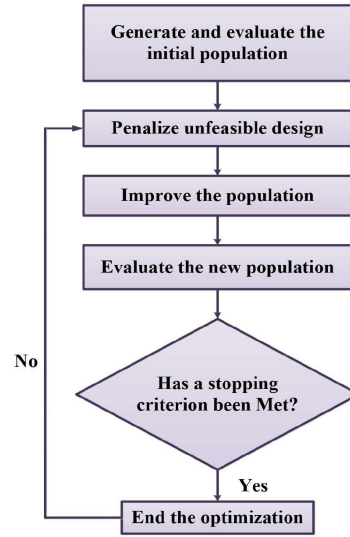


Fig. 4. Flowchart of bio-inspired algorithms search mechanism.

Various algorithms have a theme derived from bio-inspired algorithms: Particle Swarm Optimization (PSO), Dragonfly Algorithm (DA), hybrid whale PSO, salp swarm algorithm, Artificial Bee Colony Algorithm (ABC), etc., amongst others, are employed along with EAVOA to optimize both the circuits. The generalized flowchart of the search mechanism of bio-inspired algorithms is shown in Fig. 4.

IV. RESULTS AND ANALYSIS

Various Bio-inspired Algorithms are utilized in the optimization of the area of OTA for biomedical amplifiers, considering two studies. Firstly, an SFC OTA is considered for cochlear implants, and simulations are performed in MATLAB, and a comparative analysis between the state-of-the-art algorithms has been done based on their performance for 20 independent runs with the same population size and design constraints. Finally, validation of the algorithmic results is done by redesigning the SFC OTA using the transistor dimensions and other design parameters corresponding to the minimum area, i.e. the best value in Cadence Virtuoso, and performing necessary analysis. After that, similar approaches have been repeated for Case Study 2, which is an optimal two-stage OTA design for a neurological amplifier.

A. Case Study 1

Various bio-inspired algorithms are then utilized to determine the optimal area for a particular circuit by taking into account the constraints specified in Eqs. (2) to (18), and the cost function minimization formula is defined in Eq. (1). The constraints for the OTA are based on the required specifications for the cochlear implant application. Table I shows the optimal design specifications of amplifiers for various biomedical applications such as Cochlear Implants and Neural

Recording applications, and the optimal values of the design variables are then determined by considering these boundaries. Additionally, the optimal value of $1 \leq W_k/L_k \leq 100$ for each MOS transistor is also required. A population matrix of 50×10 is then created to solve the problem, while the population size of 50 is considered.

The study consists of 100 iterations at maximum, and over 20 independent runs were then performed on the algorithm to evaluate its various features. The results of the study revealed the worst, best, mean, and standard deviations of the algorithms. As a result, around 2,500 function evaluations were made for the algorithm before it was analyzed for its optimal results. The evaluation of state-of-the-art algorithms was carried out according to the parameters, and the results of the comparison are illustrated in Table II and Table III.

From Table II, it can be clearly seen that the DA Algorithm outperforms the other algorithm employed by obtaining a low area with high gain and high slew rate,

however, with a tradeoff in power dissipation. However, the power dissipation is still lower than that of other algorithms, such as WOA and HWPSO, which achieve a higher area and lower gain. In view of the above discussion, it can be inferred that DA is best suited for this case study, considering the objective function of minimization of area such that other design specifications are optimized within the bounds.

Note: CMRR and PSRR constraints were enforced during optimization as per Table I, and all algorithms satisfied these bounds. Hence, they are not repeated in Table II.

The validation of the algorithm results was performed by redesigning the SFC OTA. The minimum area of the integrated circuit was achieved by using Cadence Virtuoso simulator 180nm process technology. The pre- and post-layout analysis and simulation of the Cadence Virtuoso were carried out using the 180nm process technology.

TABLE I: OPTIMAL DESIGN SPECIFICATIONS FOR OTA'S FOR VARIOUS BIOMEDICAL APPLICATIONS

Design Criteria	Specifications (Neural)	Specifications (Cochlear)
Minimum output voltage, $V_{out(min)}$ (V)	> -1.2	> -1.2
Input noise, $S_n(f)$ (V/ $\sqrt{\text{Hz}}$)	$< 500\text{n}$	$< 2\mu$
Maximum output voltage, $V_{out(max)}$ (V)	≤ 1.2	≤ 1.2
CMRR(dB)	> 70	> 60
PSRR(dB)	> 60	> 50
Minimum ICMR, $V_{CM(min)}$ (V)	≥ -1.6	≥ -1.5
Maximum ICMR, $V_{CM(max)}$ (V)	< 1.6	< 1.5
Power dissipation, $P(\mu\text{W})$	< 7	< 7
Slew rate, SR(V/ μs)	≥ 10	≥ 10
Cut-off frequency-3dB(KHz)	≤ 15	≤ 20
Gain, A_v (dB)	> 40	> 30

TABLE II: COMPARISON OF OPTIMAL DESIGN SPECIFICATIONS DETERMINED BY BIO-INSPIRED ALGORITHMS AFTER 20 RUNS (CASE STUDY-1)

Specification	HWPSO	HBPSO	WOA	DA	BASICPSO	SSA
Slew rate (V/ μs)	14.256	10.000	14.256	14.256	10.000	14.2559
UGB (MHz)	3	3	3	3	2.5	3
Gain (dB)	41.51	42.17	40.6	46.02	43.17	44.79
$V_{IC(min)}$ (V)	-0.705	-0.010	-0.186	-0.1880	-0.265	-0.453
$V_{IC(max)}$ (V)	1.2	1.16	1.2	1.2	1.18	1.2
Power dissipation (μW)	5.12	4	5.53	4.62	4.016	4.106
Area (μm^2)	240	238.52	257.59	234.284	267.04	289.59

TABLE III: COMPARISON OF OPTIMAL DESIGN PARAMETERS DETERMINED BY BIO-INSPIRED ALGORITHMS AFTER 20 RUNS (CASE STUDY-1)

Design parameters	HWPSO	HBPSO	WOA	DA	BASICPSO	SSA
W1A/L1	25/1	25/1	25/1	25/1	25/1	25/1
W1B/L1	25/1	25/1	25/1	25/1	25/1	25/1
W2A/L2	0.045/1	0.0645/1	0.0451/1	7.142/1	0.0452/1	0.0451/1
W2B/L2	0.045/1	0.0645/1	0.0451/1	7.142/1	0.0452/1	0.0451/1
W3A/L3	1/1	1/1	1/1	10/1	1/1	1/1
W3B/L3	1/1	1/1	1/1	10/1	1/1	1/1
W4A/L4	1/1	1/1	1/1	10/1	5.91/1	1/1
W4B/L4	1/1	1/1	1/1	10/1	5.91/1	1/1
W5A/L5	10/1	10/1	10/1	10/1	10/1	10/1
W5B/L5	10/1	10/1	10/1	10/1	10/1	10/1
W6A/L6	10/1	10/1	10/1	10/1	10/1	10/1
W6B/L6	10/1	10/1	10/1	10/1	10/1	10/1
W7/L7	10/1	10/1	10/1	10/1	10/1	10/1
W8/L8	10/1	10/1	10/1	10/1	10/1	10/1
W9/L9	10/1	10/1	10/1	10/1	10/1	10/1
W10/L10	10/1	10/1	10/1	10/1	10/1	10/1
W11/L11	10/1	10/1	10/1	10/1	10/1	10/1
W12/L12	1.25/1	1.25/1	1.25/1	10/1	1.25/1	1.25/1
W13/L13	10/1	10/1	10/1	10/1	10/1	10/1
W14/L14	1.25/1	1.25/1	1.25/1	10/1	1.25/1	1.25/1
W15/L15	1/1	1/1	1/1	10/1	1/1	1/1

TABLE IV: COMPARISON WITH THE STATE-OF-THE-ART COCHLEAR IMPLANTS

Work	Gain (dB)	BW (Hz)	Noise (V/ $\sqrt{\text{Hz}}$)	Area	Power (W)
Ryoo <i>et al.</i> (2016) [43]	33	400–8 k	331n	0.282mm ²	167.7 μ
Oh <i>et al.</i> (2017) [45]	9.6	20–20 k	7.3 μ	0.07mm ²	NA
Nath <i>et al.</i> (2021) [2]	43.7	18.7–20.6 k	473.47n	46101.377 μ m ²	4.6 μ
This work	46	20–20 k	2.2 μ	234.28 μ m ²	11.6 μ

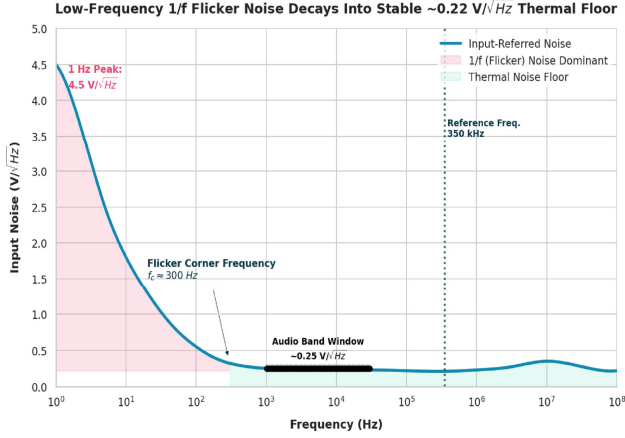


Fig. 5. Input noise plot for SFC OTA in Cadence Virtuoso.

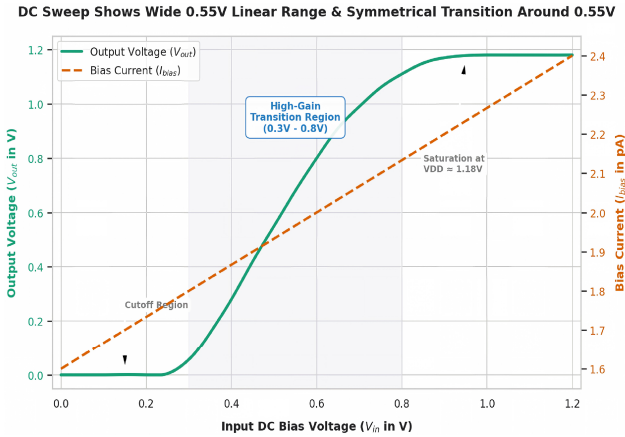


Fig. 6. ICMR plot for SFC OTA in Cadence Virtuoso.

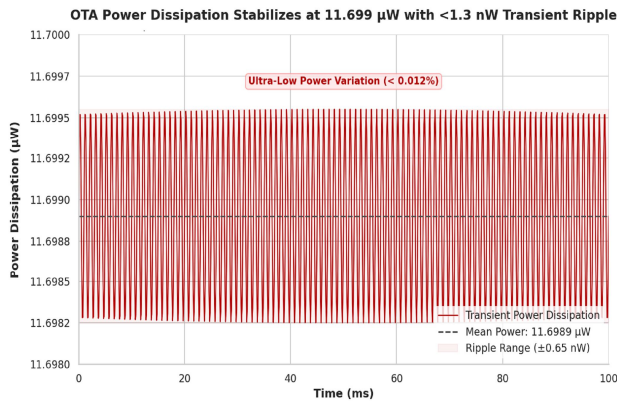


Fig. 7. Power dissipation plot for SFC OTA in Cadence Virtuoso.

The results of the analysis are shown in Fig. 5 to Fig. 8, which show proximity with algorithm-based results, with minimal deviation, and a split folded cascode (SFC) amplifier layout shown in Fig. 9. A comparison of optimized SFC OTA for Cochlear Implants with existing Cochlear Implants is presented in Table IV.

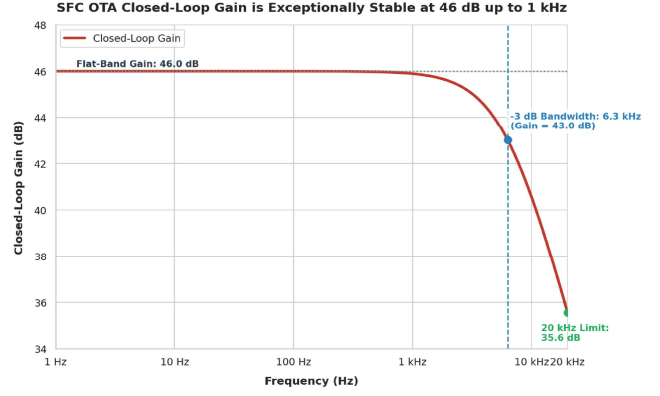


Fig. 8. Gain plot for SFC OTA in Cadence Virtuoso.

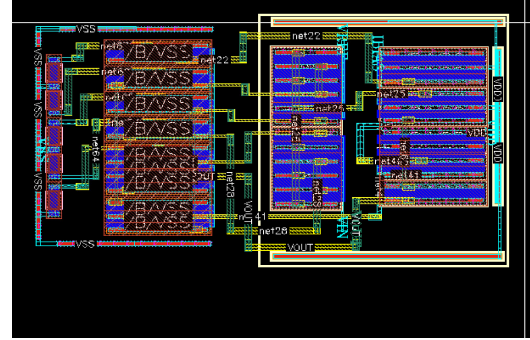


Fig. 9. Split folded cascode amplifier layout.

B. Case Study 2

Analogous to Case Study 1, the bio-inspired algorithms were utilized to determine the optimal area for the Two-Stage OTA for the neurological amplifier. The cost function minimization is defined in Eq. (20) and is subjected to the constraints specified in Eq. (21) to Eq. (35). These constraints are based on specific requirements for OTA to be utilized in the cochlear implant application. Table I presents the specifications and the optimal design variables values. These values can be determined by considering the boundaries. Additionally, the optimal value of $1 \leq W_k/L_k \leq 100$ for each MOS transistor is also required. A population matrix of 50×10 is then created to solve the problem while considering the overall population size of 50.

As before 100 iterations was chosen as maximum, and more than 20 independent runs were then done on the algorithm to evaluate its various features. These included recording the worst, best, mean, and standard deviation of the algorithms. As a result, around 2,500 function evaluations have been made for the algorithm before it is analyzed for its optimal results. The evaluation of state-of-the-art algorithms was conducted according to the specified parameters, and the results of the comparison are presented in Tables V and VI. A comparison of the optimized Two-Stage OTA-based Neurological Amplifier

Design with other reported work is presented in Table VII below.

From the results achieved, it can be noted that the EAVOA outperforms other state-of-the-art algorithms by attaining a minimum area of $450\mu\text{m}^2$, with low noise and better stability at a trade-off in gain, which is also

sufficient for amplification of biomedical signals. Table VII further validates the discussion by designing the neural amplifier using an EAVOA optimized two-stage OTA, which gives a higher mid-band gain with lower power dissipation than other reported works, but with a trade-off in power dissipation.

TABLE V: COMPARISON OF THE BEST RESULTS EVALUATED USING LCA AND OTHER ALGORITHMS AFTER 20 INDEPENDENT RUNS (CASE STUDY-2)

Specifications	PSO [34]	DE [34]	SSA	DEPSO [34]	HBPSO	DA	WOA [34]	HWPSO [34]	LCA	EAVOA
Slew rate, SR (V/ μs)	20	20	20	20	20	20	20	20	15.25	15
Unity gain frequency, f_u (MHz)	3.4	3.4	3.4	3.56	2.45	2.45	2.45	2.88	7.79	7.5
Compensation Capacitance, C_c (pF)	4	4	4	4	4	4	4	4	4.7	4
Load Capacitance, C_L (pF)	11.87	11.87	11.87	11.87	11.87	11.87	11.87	11.87	13.7	11.4
$V_{CM}(\text{min})$ (V)	-1	-1	-1	-512.92m	-543.186m	-543.186m	-543.186m	-1.12	-1.12	-1.1
$V_{CM}(\text{max})$ (V)	1.64	1.64	1.64	1.39	1.52	1.52	1.52	1.39	1.32	1.3
$V_{out}(\text{max})$ (V)	1.78	1.35	1.35	1.79	1.79	1.792	1.792	1.791	1.55	1.5
$V_{out}(\text{min})$ (V)	-1.74	-1.74	-1.74	-1.71	-1.68	-1.69	-1.69	-1.67	-1.353	-1.3
Phase Margin, ϕ_M (degrees)	49.73	49.73	49.73	45.15	44.9	45.1	45.1	77	78.53	75
Gain, A_v (dB)	60.78	60.78	60.78	46.08	69.59	69.59	69.59	65.82	34.38	33
Power dissipation (W)	1.5 μ	1.5 μ	1.5 μ	1.5 μ	1.5 μ	1.6 μ	1.6 μ	1.5 μ	3.1 μ	3.0 μ
Cut-off frequency, f_{-3dB} (KHz)	3.3	3.3	3.3	23.4	1.2	1.2	1.2	1.65	5.2	5
Input noise, $S_n(f)$ (V/ $\sqrt{\text{Hz}}$)	0.37 μ	0.37 μ	0.37 μ	0.35 μ	0.125 μ	0.125 μ	0.125 μ	0.126 μ	10.7	10.0
Optimum area, CF (m^2)	7.97e-10	7.97e-10	7.97e-10	7.52e-10	7.21e-10	7.20e-10	7.20e-10	5.23e-10	4.961e-10	4.5e-10

TABLE VI: COMPARISON OF OPTIMAL DESIGN PARAMETERS CORRESPONDING TO BEST RESULT OBTAINED USING LCA AND OTHER ALGORITHMS (CASE STUDY-2)

Design Parameters	PSO [34]	DE [34]	SSA	DEPSO	HBPSO	DA	WOA [34]	LCA	EAVOA
W1(m)	4.172e-05	4.172e-05	4.172e-05	3.45e-05	3.61e-05	3.48e-05	3.48e-05	2.1645e-05	2.175e-05
W2(m)	4.172e-05	4.172e-05	4.172e-05	3.45e-05	3.61e-05	3.48e-05	3.48e-05	2.1645e-05	2.175e-05
W3(m)	3.56e-06	3.56e-06	3.56e-06	3.54e-06	3.43e-06	3.31e-06	3.31e-06	2.6754e-06	2.19e-06
W4(m)	3.56e-06	3.56e-06	3.56e-06	3.54e-06	3.43e-06	3.31e-06	3.31e-06	2.6754e-06	2.19e-06
W5(m)	7.127e-06	7.127e-06	7.127e-06	6.69e-06	6.86e-06	6.62e-06	7.13e-06	4.8760e-06	4.32e-06
W6(m)	4.56e-05	4.56e-05	4.56e-05	5.47e-05	4.59e-05	5.11e-05	5.32e-05	4.4798e-05	3.76e-5
W7(m)	2.74e-05	2.74e-05	2.74e-05	2.58e-05	2.64e-06	2.55e-05	2.55e-05	1.8735e-05	1.534e-05
W8(m)	7.127e-06	7.127e-06	7.127e-06	6.69e-06	6.86e-06	6.62e-06	7.13e-06	5.8573e-06	5.31e-06
L1(m)	3.56e-06	3.56e-06	3.56e-06	3.34e-06	3.43e-06	3.31e-06	3.31e-06	2.3131e-06	2.1105e-06
L2(m)	3.56e-06	3.56e-06	3.56e-06	3.34e-06	3.43e-06	3.31e-06	3.31e-06	2.3131e-06	2.1105e-06
L3(m)	3.56e-06	3.56e-06	3.56e-06	3.34e-06	3.43e-06	3.31e-06	3.31e-06	2.3131e-06	2.1105e-06
L4(m)	3.56e-06	3.56e-06	3.56e-06	3.34e-06	3.43e-06	3.31e-06	3.31e-06	2.3131e-06	2.1105e-06
L5(m)	3.56e-06	3.56e-06	3.56e-06	3.34e-06	3.43e-06	3.31e-06	3.31e-06	2.3131e-06	2.1105e-06
L6(m)	7.12e-06	7.12e-06	7.12e-06	6.69e-06	6.86e-06	6.62e-06	7.13e-06	4.6263e-06	3.8432e-06
L7(m)	3.56e-06	3.56e-06	3.56e-06	3.34e-06	3.43e-06	3.31e-06	3.31e-06	2.3131e-06	2.1105e-06
L8(m)	3.56e-06	3.56e-06	3.56e-06	3.34e-06	3.43e-06	3.31e-06	3.31e-06	2.7199e-06	2.1105e-06
ID5(μA)	80	80	80	80	80	80	80	66	55

TABLE VII: RESULTS COMPARISON WITH OTHER REPORTED WORKS

Works	Gain (dB)	Bandwidth (Hz)	Input noise ($\mu\text{V}/\sqrt{\text{Hz}}$)	Power
[66]	20	NA	0.057	33.3 μW
[67]	13.81–60.15	NA	2.62	27.4 μW
[68]	30	0.3–2K	38.5	NA
This work	33	5K	10	3.0 μW

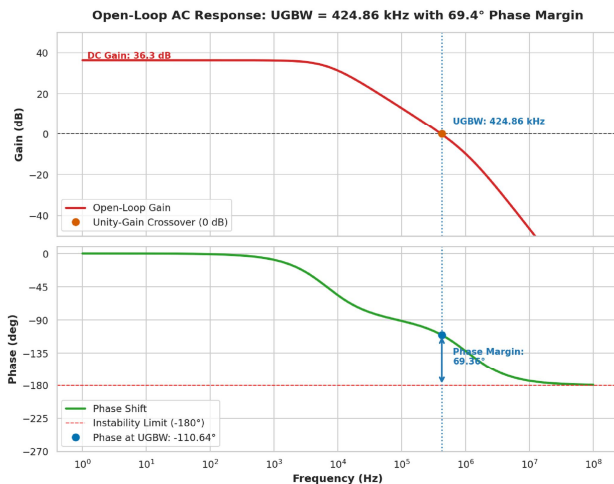


Fig. 10. Plot for gain and phase validation in Virtuoso.

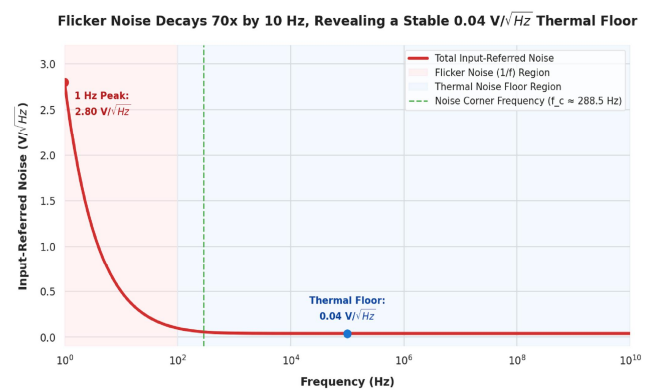


Fig. 11. Plot for validation of input referred noise in Virtuoso.

Furthermore, validation of the algorithm results has been performed. In order to reduce the design area of the

circuit, a two-stage OTA is redesigned using 180 nm technology in Cadence's Virtuoso platform, performing pre- and post-layout simulations and analysis. The results of the analysis are shown in Fig. 10 to Fig. 12, which show near proximity with algorithm based results, with minimal deviation. The two-stage OTA layout is also shown in Fig. 13.

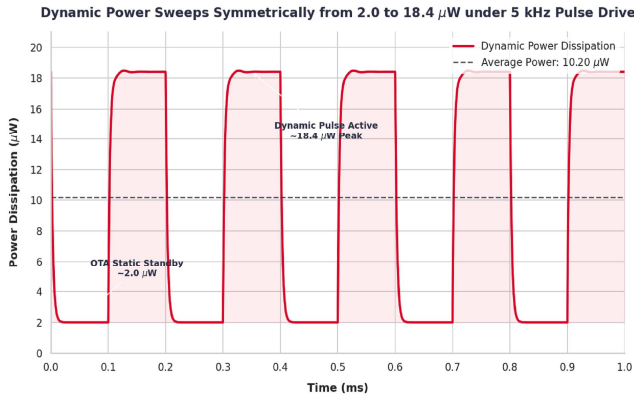


Fig. 12. Plot for validation of dynamic power dissipation in Virtuoso.

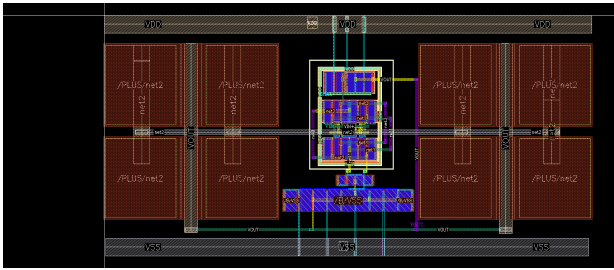


Fig. 13. Two-stage OTA layout.

V. CONCLUSION

The proposed work demonstrates the applications of bio-inspired algorithms in optimizing the design of a biomedical amplifier using a state-of-the-art bio-inspired algorithm. Among the various algorithms employed, the Enhanced AVOA (EAVOA) emerged as the most effective approach for transistor sizing, thereby optimizing the area to meet design specifications. Two case studies were performed: (i) Split Folded Cascode (SFC) OTA for cochlear implants, and (ii) Two-stage OTA for neurological amplifiers. In Case Study-1, the DA algorithm outperformed other bio-inspired algorithms, achieving a better area with optimized design specifications, which were further validated by Cadence Virtuoso-based simulations in 180 nm technology. For Case Study-2, EAVOA consistently demonstrated superior performance in area minimization with improved noise performance and more gain compared to other bio-inspired algorithms and reported works. Future works will include applying more hybrid algorithms in optimization of the circuits, and also a multi-objective optimization problem can be formulated and solved for achieving a Pareto-optimal solution.

The optimized result of SFC OTA for Cochlear Implants (case study 1) parameter using EAVOA when simulated on MATLAB environment is found to be gain 46dB, BW 20kHz, input noise $2.2\mu\text{V}/\sqrt{\text{Hz}}$, area

$234.28\mu\text{m}^2$, power $11.6\mu\text{W}$, and the results obtained in this case study from EAVOA are compared with HWPSO (Hybrid Whale Particle Swarm Optimization), HBPSO (Human behavior based Particle Swarm Optimization), WOA, DA, BASICPSO, and SSA (Salp Swarm Algorithm) algorithms. The optimized result of Two Stage OTA-based Neurological Amplifier (case study 2) parameter using EAVOA when simulated on MATLAB environment is found to be a gain of 33dB, input noise of $10\mu\text{V}/\sqrt{\text{Hz}}$, power of $3.0\mu\text{W}$, and frequency bandwidth of 5KHz. Results obtained in case study 2 from EAVOA are also compared with PSO, DE, SSA, DEPSO, HBPSO, DA, WOA, and LCA. The results of the analysis depict the better performance of the EAVOA over the PSO, DE, SSA, DEPSO, HBPSO, DA, WOA, and LCA algorithms.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Kumari Archana conducted Problem Formulation, Simulation and Data Analysis, and Writing the Original Draft. Ram Kumar conducted Supervision, Reviewing, and Editing. Naushad Manzoor Laskar conducted Supervision, Editing, Reviewing, and Data Analysis. All authors approved the final version.

REFERENCES

- [1] N. M. Laskar, K. Guha, S. Nath, S. Chanda *et al.*, "Design of high gain, high bandwidth neural amplifier IC considering noise-power trade-off," *Microsyst. Technol.*, vol. 27, pp. 585–599, 2021. doi: 10.1007/s00542-018-4142-5
- [2] S. Nath, N. M. Laskar, S. Devi, K. Guha, K. L. Baishnab, and J. Iannacci, "Design of low power preamplifier IC for cochlear implant using split folded cascode technique," *Microsyst. Technol.*, vol. 27, no. 9, pp. 3483–3491, 2021.
- [3] V. Chaturvedi and B. Amrutur, "An area-efficient noise-adaptive neural amplifier in 130 nm CMOS technology," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 1, no. 4, pp. 536–545, 2011.
- [4] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, 2007. doi: 10.1109/TBCAS.2007.907071
- [5] M. Habibollahi, D. Jiang, H. T. Lancashire, and A. Demosthenous, "Active neural interface circuits and systems for selective control of peripheral nerves: A review," *IEEE Trans. Biomed. Circuits Syst.*, 2024. doi: 10.1109/TBCAS.2024.3430038
- [6] K. L. Baishnab, K. Guha, S. Chanda, N. M. Laskar, and D. Biswas, "A low power, low noise amplifier for neural signal amplification in SCL 180nm," in *Proc. 2017 Int. Conf. on Electron Devices and Solid-State Circuits (EDSSC)*, 2017, pp. 1–2. doi: 10.1109/EDSSC.2017.8333234
- [7] H. Ali, T. J. Ahmad, A. Ajaz, and S. A. Khan, "Laboratory prototype of cochlear implant: Design and techniques," in *Proc. 2009 Annual Int. Conf. of the IEEE Engineering in Medicine and Biology Society*, 2009, pp. 803–806.
- [8] D. Joshi, S. Dash, S. Reddy, R. Manigilla, and G. Trivedi, "Multi-objective hybrid particle swarm optimization and its application to analog and RF circuit optimization," *Circuits, Syst. Signal Process.*, vol. 42, no. 8, pp. 4443–4469, 2023.
- [9] H. A. Yiğit, H. Uluşan, M. Koç, M. B. Yüksel, S. Chamanian, and H. Külah, "Single supply PWM fully implantable cochlear implant interface circuit with active charge balancing," *IEEE Access*, vol. 9, pp. 52642–52653, 2021.

- [10] Z. Jakšić, S. Devi, O. Jakšić, and K. Guha, "A comprehensive review of bio-inspired optimization algorithms including applications in microelectronics and nanophotonics," *Biomimetics*, vol. 8, no. 3, 278, 2023.
- [11] N. Kumar, K. L. Baishnab, S. Nath, K. Guha, and K. S. Rao, "Design of low power, low noise with high output swing preamplifier of cochlear implants," in *Proc. 2023 IEEE Devices for Integrated Circuit*, 2023, pp. 511–515. doi: 10.1109/DevIC57758.2023.10134815
- [12] A. Ahmed, M. F. Nadeem, I. A. Sajjad, R. Bo, and I. A. Khan, "Optimal allocation of wind DG with time varying voltage dependent loads using bio-inspired: Salp swarm algorithm," in *Proc. 2020 3rd Int. Conf. on Computing, Mathematics and Engineering Technologies (iCoMET)*, 2020, pp. 1–7. doi: 10.1109/iCoMET48670.2020.9074118
- [13] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proc. ICNN'95 - Int. Conf. Neural Networks*, vol. 4, pp. 1942–1948. doi: 10.1109/ICNN.1995.488968
- [14] W.-J. Zhang and X.-F. Xie, "DEPSO: hybrid particle swarm with differential evolution operator," in *Proc. 2003 IEEE Int. Conf. on Systems, Man and Cybernetics. Conf. Theme-System Security and Assurance*, 2003, vol. 4, pp. 3816–3821.
- [15] R. W. Kadhim, "Optimizing learning object sequencing in E-learning systems using human behaviour-based particle swarm optimization," *J. La Multiapp*, vol. 6, no. 3, pp. 457–469, 2025.
- [16] A. P. Piotrowski, J. J. Napiorkowski, and A. E. Piotrowska, "Particle swarm optimization or differential evolution—A comparison," *Eng. Appl. Artif. Intell.*, vol. 121, 106008, 2023.
- [17] N. M. Laskar, K. Guha, K. L. Baishnab, P. K. Paul, and K. Srinivasa Rao, "Optimizing the random offset voltage in two stage amplifier considering noise-power trade-off using HWPSO algorithm," in *Proc. ESDA 2019*, pp. 349–359, 2020.
- [18] C. M. Rahman, T. A. Rashid, A. Alsadoon, N. Bacanin, P. Fattah, and S. Mirjalili, "A survey on dragonfly algorithm and its applications in engineering," *Evol. Intell.*, vol. 16, no. 1, pp. 1–21.
- [19] M. H. Nadimi-Shahraki, H. Zamani, Z. Asghari Varzaneh, and S. Mirjalili, "A systematic review of the whale optimization algorithm: Theoretical foundation, improvements, and hybridizations," *Arch. Comput. Methods Eng.*, vol. 30, no. 7, pp. 4113–4159, 2023.
- [20] A. H. Kashan, "League championship algorithm (LCA): An algorithm for global optimization inspired by sport championships," *Appl. Soft Comput.*, vol. 16, pp. 171–200, 2014. doi: 10.1016/j.asoc.2013.12.005
- [21] B. Abdollahzadeh, F. S. Gharehchopogh, and S. Mirjalili, "African vultures optimization algorithm: A new nature-inspired metaheuristic algorithm for global optimization problems," *Comput. Ind. Eng.*, vol. 158, art. no. 107408, 2021.
- [22] S. Mirjalili, "Dragonfly algorithm: A new meta-heuristic optimization technique for solving single-objective, discrete, and multi-objective problems," *Neural Comput. Appl.*, vol. 27, no. 4, pp. 1053–1073, 2016. doi: 10.1007/s00521-015-1920-1
- [23] H. Liu, G. Xu, G. Ding, and Y. Sun, "Human behavior-based particle swarm optimization," *Sci. World J.*, vol. 2014, 2014. doi: 10.1155/2014/194706
- [24] M. Pant, H. Zaheer, L. Garcia-Hernandez, and A. Abraham, "Differential evolution: A review of more than two decades of research," *Eng. Appl. Artif. Intell.*, vol. 90, art. no. 103479, 2020.
- [25] S. Mirjalili and A. Lewis, "The whale optimization algorithm," *Adv. Eng. Softw.*, vol. 95, pp. 51–67, 2016. doi: 10.1016/j.advengsoft.2016.01.008
- [26] Z. Meng and Y. Chen, "Differential evolution with exponential crossover can be also competitive on numerical optimization," *Appl. Soft Comput.*, vol. 146, 110750, 2023.
- [27] R. Das, B. P. De, S. Ghosh, R. Kar, D. Mandal, and B. Appasani, "Optimal CMOS analog amplifier circuit design using a modified PSO for consumer electronic applications," *J. Electr. Comput. Eng.*, vol. 2024, no. 1, 2004118, 2024.
- [28] S. K. Dash, B. P. De, P. K. Samanta, B. Appasani *et al.*, "Optimal design of voltage reference circuit and ring oscillator circuit using multiobjective differential evolution algorithm," *J. Electr. Comput. Eng.*, vol. 2023, no. 1, 7621594, 2023.
- [29] H. Bouali, B. Benhala, and M. Guerbaoui, "Multi-objective optimization of CMOS low noise amplifier through nature-inspired swarm intelligence," *Bull. Electr. Eng. Informatics*, vol. 12, no. 5, pp. 2824–2836, 2023.
- [30] P. K. Paul, N. M. Laskar, S. Nath, and K. L. Baishnab, "Performance analysis of new swarm intelligence based algorithms in optimizing the design of CMOS folded cascode OPAMP and comparator circuits," *Int. J. Appl. Eng. Res.*, vol. 10, no. 22, pp. 973–4562, 2015.
- [31] S. K. Dash, B. P. De, B. Appasani, N. K. Rout, and A. Srinivasulu, "Design of a optimized CMOS differential amplifier using Crazyness-based PSO," *J. VLSI Circuits Syst.*, vol. 7, no. 1, pp. 26–31, 2025.
- [32] N. M. Laskar, K. Guha, S. Nath, K. L. Baishnab, and P. K. Paul, "Optimal sizing of recycling folded cascode amplifier for low-frequency applications using new hybrid swarm intelligence-based technique," *Appl. Artif. Intell.*, vol. 34, no. 12, pp. 880–897, 2020.
- [33] N. M. Laskar, K. Guha, P. K. Paul, and K. L. Baishnab, "Random offset minimization in low frequency front-end amplifiers using swarm intelligence based techniques," *Evol. Intell.*, vol. 14, pp. 1317–1335, 2021. doi: 10.1007/s12065-020-00495-5
- [34] R. Das, K. N. Das, S. Mallik, S. Das, N. M. Laskar, and S. Nath, "A novel self-adaptive multi-population quadratic approximation guided jaya for solving real-parameter constrained optimization problems," *Expert Syst. Appl.*, vol. 238, 121898, 2024.
- [35] N. M. Laskar, S. Devi, S. Kumaravel, M. N. Hasan, S. Choudhury, and A. Pandey, "Optimal design of a biomedical amplifier for minimum offset using a modified ABC algorithm," *Solving with Bees: Transformative Applications of Artificial Bee Colony Algorithm*, Springer, pp. 117–132, 2024.
- [36] M. Mneimneh, N. Quadir, and L. Albasha, "Advancements in neural recording circuits: Review of nerve biopotentials, and neural recording circuit architectures," *IEEE Access*, 2024. doi: 10.1109/ACCESS.2024.3441840
- [37] S. Nath, K. Guha, and K. L. Baishnab, "A review on neural amplifier design," *Micro Nanoelectron. Devices, Circuits Syst. Sel. Proc. MNDCS 2023*, 2023, vol. 1067, 355.
- [38] U. Kumari and R. Yadav, "A review about analysis and design methodology of two-stage operational transconductance amplifier (OTA)," in *Proc. Int. Conf. on Data Science and Applications: ICDSA 2022*, 2023, pp. 849–860.
- [39] S. Nath, S. Devi, N. M. Laskar, K. Guha, and K. L. Baishnab, "Design of a noise efficient bio-amplifier using CCFVF OTA for neurological signal acquisition," *Microsyst. Technol.*, vol. 31, no. 12, pp. 1–13, 2025. doi: 10.1007/s00542-025-05932-y
- [40] S. Nath, L. Kundu, S. Devi, K. Guha, and K. L. Baishnab, "Analysis of a low-power OTA-based neural amplifier design for EEG signal acquisition," *J. Circuits, Syst. Comput.*, vol. 33, no. 10, 2450174, 2024.
- [41] S. Nath, N. Kumar, K. Guha, K. L. Baishnab, and K. S. Rao, "Novel design of a low power neural amplifier using split push pull balanced high swing OTA for brain machine interface," *Microsyst. Technol.*, vol. 30, no. 2, pp. 197–207, 2024.
- [42] S. Nath, K. Guha, and K. L. Baishnab, "A review on neural amplifier design for brain-machine interface," in *Proc. Int. Conf. on Micro/Nanoelectronics Devices, Circuits and Systems*, 2023, pp. 355–374.
- [43] K. Ryoo, M. Chilukuri, and S. Jung, "A low power and low noise preamplifier circuit for hearing aid devices," in *Proc. 2016 IEEE Dallas Circuits and Systems Conf. (DCAS)*, 2016, pp. 1–4. doi: 10.1109/DCAS.2016.7791128
- [44] S. Devi, K. Guha, and K. L. Baishnab, "Swarm intelligence-based mono and multi-objective methods for sizing preamplifier circuits for biomedical applications," *Int. J. Nanoparticles*, vol. 14, no. 2–4, pp. 159–180, 2022.
- [45] S. Oh, T. Jang, K. D. Choo, D. Blaauw, and D. Sylvester, "A 4.7 μ W switched-bias MEMS microphone preamplifier for ultra-low-power voice interfaces," in *Proc. 2017 Symposium on VLSI Circuits*, 2017. doi: 10.23919/VLSIC.2017.8008522
- [46] M. Croce, C. De Berti, L. Crespi, P. Malcovati, and A. Baschiroto, "Cap-less audio preamplifiers for silicon microphones," in *Proc. 2016 IEEE SENSORS*, 2016. doi: 10.1109/ICSENS.2016.7808720
- [47] S. Nath, L. Kundu, K. Guha, and K. L. Baishnab, "Design and analysis of cross-coupled source degenerated balanced OTA for biomedical application," in *Proc. 2024 28th Int. Symp. on VLSI Design and Test*, 2024. doi: 10.1109/VDAT63601.2024.10705720
- [48] J. B. Yogeshwar, N. M. Laskar, A. Samuel, A. Solomon, and V. Vijayvargiya, "Design and analysis of low noise, low power OTA considering design trade-offs for biomedical applications," *Results Eng.*, 105103, 2025.

- [49] R. Mendes, J. Kennedy, and J. Neves, "The fully informed particle swarm: simpler, maybe better," *IEEE Trans. Evol. Comput.*, vol. 8, no. 3, pp. 204–210, 2004.
- [50] I. Fister Jr, X.-S. Yang, I. Fister, J. Brest, and D. Fister, "A brief review of nature-inspired algorithms for optimization," *arXiv*, arXiv:1307.4186, 2013.
- [51] S. Mirjalili and S. Z. M. Hashim, "A new hybrid PSOGSA algorithm for function optimization," in *Proc. 2010 Int. Conf. on Computer and Information Application*, 2010, pp. 374–377.
- [52] D. Pal, P. Verma, D. Gautam, and P. Indait, "Improved optimization technique using hybrid ACO-PSO," in *Proc. 2016 2nd Int. Conf. on Next Generation Computing Technologies (NGCT)*, 2016, pp. 277–282.
- [53] S. Mirjalili, A. H. Gandomi, S. Z. Mirjalili, S. Saremi, H. Faris, and S. M. Mirjalili, "Salp swarm algorithm: A bio-inspired optimizer for engineering design problems," *Adv. Eng. Softw.*, vol. 114, pp. 163–191, Dec. 2017.
- [54] B. P. De, R. Kar, D. Mandal, and S. P. Ghoshal, "Optimal analog active filter design using craziness-based particle swarm optimization algorithm," *Int. J. Numer. Model. Electron. Networks, Devices Fields*, vol. 28, no. 5, pp. 593–609, 2015.
- [55] P. E. Allen, R. Dobkin, and D. R. Holberg, *CMOS Analog Circuit Design*. Elsevier, 2011.
- [56] J. Mahattanakul and J. Chutichatuporn, "Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 52, no. 8, pp. 1508–1514, 2005.
- [57] W. Cao, X. Chen, Z. Cao, and B. Badami, "An improved African vulture optimization for bidding strategy of two-settlement market in China," *J. Electr. Eng. Technol.*, vol. 18, no. 2, pp. 751–764, 2023.
- [58] A. G. Hussien, F. S. Gharehchopogh, A. Bouaouda, S. Kumar, and G. Hu, "Recent applications and advances of African vultures optimization algorithm," *Artif. Intell. Rev.*, vol. 57, no. 12, 335, 2024.
- [59] G. A. Ghazi, H. M. Hasanien, E. A. Al-Ammar, R. A. Turkey, W. Ko, S. Park, and H.-J. Choi, "African vulture optimization algorithm-based PI controllers for performance enhancement of hybrid renewable-energy systems," *Sustainability*, vol. 14, no. 13, 8172, 2022, doi: 10.3390/su14138172
- [60] F. S. Gharehchopogh and T. Ibricki, "An improved African vultures optimization algorithm using different fitness functions for multi-level thresholding image segmentation," *Multimed. Tools Appl.*, vol. 83, no. 6, pp. 16929–16975, 2024.
- [61] D. Ke and C. Yu, "Multi-strategy improved African vulture optimization algorithm," in *Proc. 2023 4th Int. Seminar on Artificial Intelligence, Networking and Information Technology (AINIT)*, 2023, pp. 524–528.
- [62] H. Askr, M. A. Farag, A. E. Hassanien, V. Snášel, and T. A. Farrag, "Many-objective African vulture optimization algorithm: A novel approach for many-objective problems," *PLoS One*, vol. 18, no. 5, e0284110, 2023.
- [63] K. Jayasree and M. K. Hota, "Optimized convolutional neural network using African vulture optimization algorithm for the detection of exons," *Sci. Rep.*, vol. 15, no. 1, 3810, 2025.
- [64] H. Blankson, V. Chandran, H. Lala, and P. Mohapatra, "An enhanced opposition-based African vulture optimizer for solving engineering design problems and global optimization," *Sci. Rep.*, vol. 15, no. 1, 33078, 2025.
- [65] R. Zheng, A. G. Hussien, R. Qaddoura, H. Jia *et al.*, "A multi-strategy enhanced African vultures optimization algorithm for global optimization problems," *J. Comput. Des. Eng.*, vol. 10, no. 1, pp. 329–356, 2023.
- [66] R. F. Yazicioglu, "A 60µW 60 nV/√Hz readout front-end for portable biopotential acquisition systems," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1100–1110, 2006. doi: 10.1109/JSSC.2007.894804
- [67] S. A. Mahmoud and A. A. Alhammedi, "A CMOS digitally programmable OTA based instrumentation amplifier for EEG detection system," in *Proc. 2015 IEEE Int. Conf. on Electronics, Circuits, and Systems (ICECS)*, 2015, pp. 543–546.

- [68] L. Gupta and A. Kumar, "An efficient approach to design of EEG preamplifier using conventional transconductance amplifiers," in *Proc. 2021 Int. Conf. on Advances in Electrical, Computing, Communication and Sustainable Technologies (ICAECT)*, 2021. doi: 10.1109/ICAECT49130.2021.9392473

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