Timer-Based Capacitance-to-Voltage Converter

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***Abstract*—This article presents the design and analysis of a capacitance-to-voltage converter based on 555-timer Integrated Circuits (ICs) as the core design element. The circuit structure consists of two primary active components: two 555-timer ICs connected in conjunction with a low-pass filter circuit. The first 555-timer IC operates in astable mode to generate a signal that controls the timing of the second IC. The target capacitor or capacitive sensor to be measured is connected to the second 555-timer IC, which operates in monostable mode. The output signal from the second 555-timer IC is then converted into a DC voltage output using a low-pass filter circuit. The circuit was tested using laboratory capacitors in the range of 52.72 pF to 807.61 pF, and the data were analyzed using Microsoft Excel. The results showed excellent agreement with the measurements obtained from the GW INSTEK LCR-819. The maximum uncalibrated error was found to be −3.32% of full scale. After applying linear curve fitting in Excel, the maximum error was reduced to 0.92% of full scale, confirming the effectiveness of the calibration approach. Furthermore, the circuit was applied to measure the moisture content of paddy rice using a cylindrical capacitive sensor within the moisture range of 12.1% to 23.2%. The experimental data were fitted to a derived equation, which was then used to predict rice moisture content, producing results that corresponded closely with those obtained from the KETT PM-450 grain moisture meter.**

***Index Terms*—Capacitance-to-Voltage Converter (CVC), 555-timer, capacitive sensor, capacitive readout circuit**

I. Introduction

The Capacitance-to-Voltage Converter (CVC) is a type of circuit block specifically designed to measure capacitance in capacitors and capacitive sensors. Over the years, its designs and applications have been diversified and improved. The classification of CVCs can vary depending on the context or the criteria adopted for grouping. In this study, the CVCs of interest are categorized as shown in Fig. 1 and explained as follows. The first group relies on an AC sine wave voltage generator to produce an excitation signal (V_{ex}) for the target capacitor (C_x) to be measured [1–4]. This signal is processed through Voltage-to-Current (VIC) and Current-to-Voltage Conversion (IVC) circuits, typically based on active components such as operational amplifiers (op-amps). The amplitude of the resulting voltage signal corresponds to the capacitance value of C_x. An amplitude detector circuit is then used to convert the amplitude into a DC voltage output (V_{out}). Common approaches for amplitude detection include combining a rectifier circuit with a low-pass filter [2] or using a signal multiplier circuit with a low-pass filter [3, 4]. This method is highly effective for measuring small capacitance values but poses challenges in maintaining precise control of the V_{ex} signal amplitude, as it directly influences the V_{out} signal magnitude.

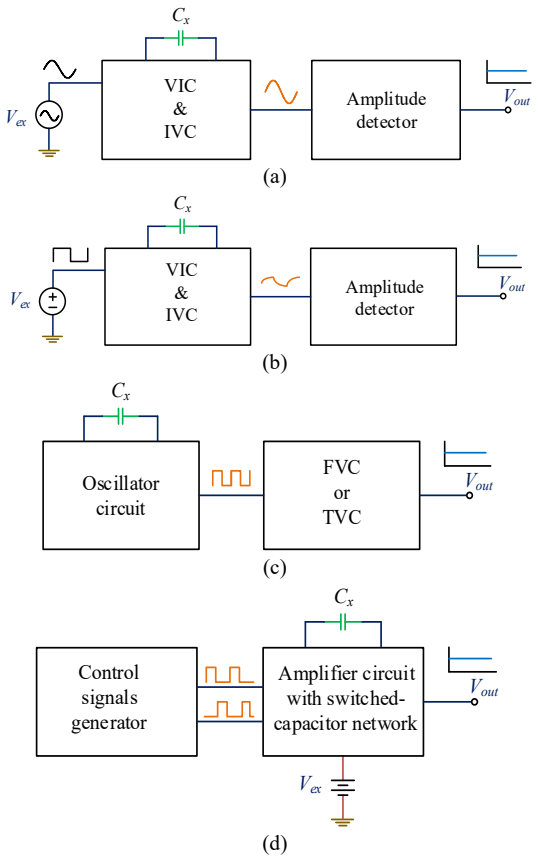

Fig. 1. Various configurations of CVCs previously proposed: (a) Utilizing a sine wave voltage signal as the excitation signal, (b) Utilizing a square wave voltage signal as the excitation signal, (c) Integrating the target capacitor as part of an oscillator circuit, and (d) Employing the characteristics of a switched-capacitor circuit.

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The second group, as reported in earlier studies, has a circuit design similar to the first group but differs in key aspects. A square wave voltage signal is used as the excitation signal (V_{ex}) for the target capacitor (C_x) instead of a sine wave. The VIC and IVC are implemented through a simple RC circuit, where the overall impedance converts voltage to current, and the capacitor impedance converts current back to voltage. Amplitude detection is performed using a basic rectifier circuit combined with a low-pass filter [5, 6]. This approach simplifies signal generation and amplitude control, as square wave signals are easier to handle compared to sine wave signals. Consequently, the sub-circuits are less complex than those in the first group. However, the use of a simple rectifier circuit (without an op-amps) can result in interference from thermal voltage and the diode's built-in potential barrier, which can adversely impact the detection of small signal amplitudes.

The third group utilizes a method where the target capacitor (C_x) to be measured is integrated as a component of an oscillator circuit. This circuit generates a square wave signal whose frequency (or period) is determined by the capacitance value of C_x. The frequency is then converted into a voltage signal using a Frequency-to-Voltage Converter (FVC) [7, 8]. The advantage of this approach is its self-excitation capability, eliminating the need for an external signal generator, which results in a relatively simple circuit structure. Nevertheless, numerous studies [9, 10] have indicated that the frequency of the excitation signal can significantly affect the dielectric constant or the capacitance of the sensor being measured. This means that measurements conducted at different excitation frequencies may produce inconsistent capacitance values. As such, employing a fixed excitation frequency provides more reliable measurements and allows for confident comparisons with other measurement instruments.

The fourth group involves designing a circuit using a switched capacitor network integrated as part of an amplifier circuit, commonly referred to as a switched capacitor circuit [11–14]. This design leverages the charge transfer properties of capacitors, where the circuit behaves as an equivalent resistance that depends on the capacitance value and the frequency of the control signal. The CVC circuit proposed in this paper shares similarities and differences with the principles mentioned earlier. The circuit design is based on the widely available 555 timer IC, utilizing a fixed-frequency square wave signal to control the operation of a monostable circuit. The square wave voltage output from the monostable circuit contains a DC component that is directly proportional to the capacitance of the measured capacitor. A simple low-pass filter is then employed to smooth the signal, eliminating the need for additional components such as signal multipliers or rectifier circuits. A principal advantage of the circuit proposed in this paper lies in the stability of both the amplitude and frequency of the excitation signal applied to the sensor or target capacitor—attributes that can be more readily controlled than those of the first group of CVC circuits previously described. Moreover, the proposed circuit exhibits a broader linear operating range than that of the second group of CVC circuits, while maintaining a substantially lower level of circuit complexity compared to the third and fourth groups. These combined merits enable the circuit to be implemented efficiently as a discrete-type integrated configuration, thereby supporting practical realization with minimal design overhead.

The structure of the content in this paper is organized as follows: Section II presents the proposed CVC circuit, which discusses the operating principles, analytical modeling, and key limitations of the circuit. Section III describes materials and methods. Section IV outlines the experimental results and discussion, where the experiments are divided into two main parts: 1) circuit testing using laboratory capacitors and 2) testing with a cylindrical sensor designed for measuring the moisture content of paddy rice. Finally, Section V concludes the paper.

II. Proposed Capacitance-to-Voltage Converter

The proposed CVC is based on the 555-timer ICs, as shown in Fig. 2, C_x represents the target capacitor to be measured or converted into a DC voltage output signal. Fig. 2 (c) illustrates a timing diagram sketch, showing the waveform of voltage signals at critical points in the circuit. The operation of the circuit can be explained as follows: The 555-timer$_1$ is configured in an astable mode to generate the voltage signal V_{o1}, which is used to control the timing operation of the 555-timer$_2$. The voltage signal V_{o1} has time durations for its logic 0 and logic 1 states, denoted as T_1 and T_2, respectively, and can be expressed as follows:

$$T_1 = R_b C_0 \ln(2) \tag{1}$$

$$T_2 = (R_a + R_b) C_0 \ln(2) \tag{2}$$

The period T, duty cycle D_c, and frequency f of the voltage signal V_{o1} can be determined as follows:

$$T = T_1 + T_2 = (R_a + 2R_b) C_0 \ln(2) \tag{3}$$

$$D_c = \frac{T_2}{T} = \frac{(R_a + R_b)}{(R_a + 2R_b)} \tag{4}$$

$$f = \frac{1}{T} = \frac{1}{(R_a + 2R_b) C_0 \ln(2)} \tag{5}$$

From Eq. (1) to Eq. (5), to ensure sufficient time for the monostable circuit to charge C_x, this work employs a technique where $R_a > R_b$. This approach differs from the typical design of the astable circuits for reading capacitive sensors [15], where D_c is often designed to be close to 0.5 ($T \approx 2T_2$).

Consider the monostable circuit operation. When the voltage signal V_{o1} transitions from logic 1 to logic 0, the voltage signal V_{o2} transitions from logic 0 to logic 1. During this time, the capacitor C_x is charged, causing the voltage V_c to rise from 0 V to approximately $(2/3)V_{cc}$, where V_{cc} is the supply voltage. After reaching this value, the capacitor C_x discharges instantaneously, resulting in V_c returning to 0 V, and the voltage signal V_{o2} transitions from logic "1" to logic "0". The time duration (t_c) for which V_{o2} remains at logic "1"

can be expressed as follows:

$$t_c = [R_1 \ln(3)]C_x \quad (6)$$

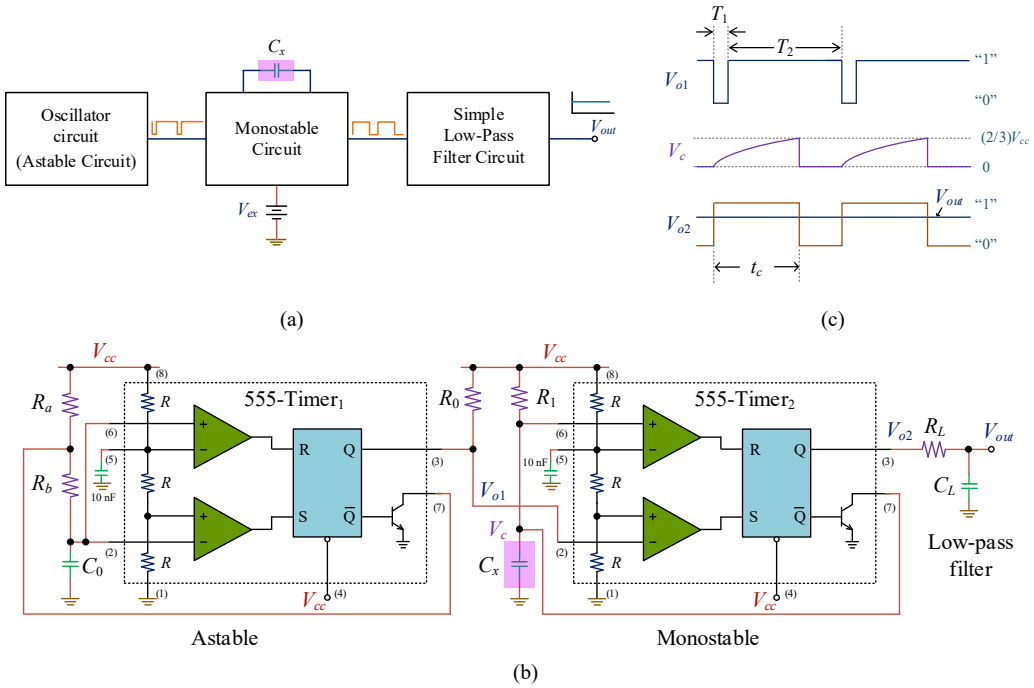


Fig. 2. The proposed CVC: (a) Block diagram, (b) circuit structure and (c) timing diagram.

When analyzing the DC component of the voltage signal V_{o2}, the result is given as follows:

$$V_{o2(\mathrm{dc})} = \frac{t_c}{T} V_{o2(\max)} = \frac{R_1 \ln(3) V_{o2(\max)}}{(R_a+2R_b)C_0 \ln(2)} C_x \quad (7)$$

where $V_{o2(\mathrm{dc})}$ denotes the DC component of the voltage signal V_{o2}, and $V_{o2(\max)}$ represents the magnitude of V_{o2} when in the logic "1" state. The voltage signal V_{o2} is subsequently converted into a smooth output voltage signal V_{out} using a simple low-pass filter. The resulting expression is as follows:

$$V_{\mathrm{out}} = V_{o2(\mathrm{dc})} = HC_x = \frac{R_1 \ln(3) V_{o2(\max)}}{(R_a+2R_b)C_0 \ln(2)} C_x \quad (8)$$

$$H = \frac{R_1 \ln(3) V_{\mathrm{cc}}}{(R_a+2R_b)C_0 \ln(2)} \quad (9)$$

where H represents the transfer rate between V_{out} and C_x. From Eq. (8) to Eq. (9), it is evident that the output voltage V_{out} exhibits a linear relationship with the capacitance C_x. The circuit can be utilized for capacitance measurement by employing Excel to perform linear regression fitting based on a linear model for calibration of the measurement results.

The analysis of the limitations of the proposed circuit can be considered as follows. The first condition requires that t_c must be greater than or equal to T_1 ($t_c \geq T_1$). This implies that in the circuit design, T_1 should be minimized. The resulting condition for setting the circuit parameters is given as:

$$C_{x(\min)} = \frac{R_b C_0 \ln(2)}{R_1 \ln(3)} \quad (10)$$

where $C_{x(\min)}$ represents the minimum value of C_x that the circuit can measure or convert into a voltage signal.

The second limitation requires that t_c must be less than or equal to T ($t_c \leq T$). This condition ensures that C_x is fully charged, reaching V_c=(2/3)V_{cc}, before V_{o1} transitions to logic 0. The corresponding condition for determining the circuit parameters is given as:

$$C_{x(\max)} = \frac{(R_a+2R_b)C_0 \ln(2)}{R_1 \ln(3)} \quad (11)$$

where $C_{x(\max)}$ represents the maximum value of C_x that the circuit can measure or convert into a voltage signal.

Analysis of Measurement Uncertainty Arising from Component Tolerances (R_a, R_b, R_1, C_0) and the Voltage Parameter $V_{o2(\max)}$: From Eq. (7) and Eq. (8), the output voltages $V_{o2(\mathrm{dc})}$ and V_{out} are theoretically independent of the supply voltage V_{cc}. However, the influence of V_{cc} implicitly appears through the parameter $V_{o2(\max)}$, which depends on the electrical characteristics of the 555-timer IC used.

When considering the tolerances of R_a, R_b, R_1, and C_0 together with the tolerance of $V_{o2(\max)}$, the corresponding measurement uncertainty can be evaluated as follows. Let ΔR_a, ΔR_b, ΔR_1, ΔC_0, and $\Delta V_{o2(\max)}$ denote the respective tolerances. By substituting each parameter with its nominal value plus its deviation, the resulting uncertainty in output voltage ΔV_{out} can be expressed as:

$$\Delta V_{\mathrm{out}} = \left[\frac{\Delta R_1}{R_1} + \frac{\Delta V_{o2(\max)}}{V_{o2(\max)}} + \frac{\Delta C_0}{C_0} + \frac{\Delta R_a + 2\Delta R_b}{R_a+2R_b}\right] V_{\mathrm{out}} \quad (12)$$

Analysis of the effect of the sensor's internal parasitic resistance: When the circuit is applied to a lossy capacitive sensor, it is assumed that a parasitic resistance R_x is in parallel with the capacitance C_x, as depicted in Fig. 3 The astable circuit has been excluded for simplicity. The voltage signal V_{o1} exhibits the properties defined by

Eq. (1)–Eq. (5). In the monostable section, the parasitic resistance R_x in parallel with the capacitance C_x affects the time duration t_c of the voltage signal V_{o2}. By employing the Thevenin equivalent circuit, as depicted in Fig. 4, the analysis for t_c proceeds as follows:

$$V_{\text{th}} = \frac{R_x}{(R_1+R_x)} V_{cc} \tag{13}$$

$$R_{\text{th}} = \frac{R_1 R_x}{(R_1+R_x)} \tag{14}$$

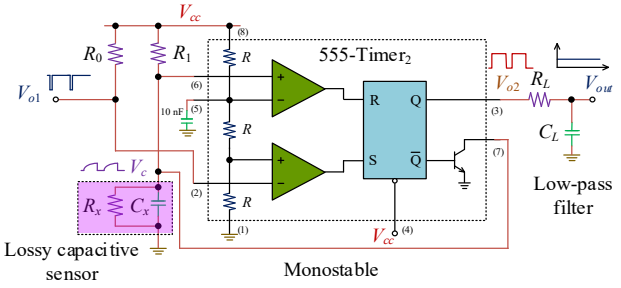


Fig. 3. The proposed CVC with lossy capacitive sensor.

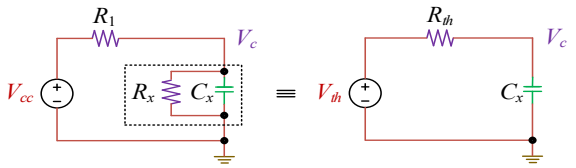


Fig. 4. Thevenin equivalent circuit for the lossy capacitive sensor.

As a result, the voltage signal V_{o2} will have a time duration t_c given by:

$$t_c = \left[\frac{R_1 R_x}{(R_1+R_x)} \ln\left(\frac{3R_x}{R_x-2R_1}\right)\right] C_x \tag{15}$$

This gives:

$$V_{o2(\text{dc})} = \frac{t_c}{T} V_{02(\text{max})} = \left[\frac{R_1 R_x}{(R_1+R_x)} \ln\left(\frac{3R_x}{R_x-2R_1}\right)\right] \frac{V_{02(\text{max})}}{T} C_x \tag{16}$$

$$V_{\text{out}} = V_{o2(\text{dc})} = HC_x \tag{17}$$

$$H = \left[\frac{R_1 R_x}{(R_1+R_x)} \ln\left(\frac{3R_x}{R_x-2R_1}\right)\right] \frac{V_{02(\text{max})}}{T} \tag{18}$$

From Eq. (16) to Eq. (18), it can be observed that the output voltage V_{out} remains directly proportional to the capacitance C_x. However, a concern when applying the circuit to lossy capacitive sensors is that the resistance R_x also influences the magnitude of the output voltage V_{out}. Nevertheless, calibrating the experimental results with the equation (or mathematical model) derived from the inversion of Eq. (16) can help develop a measurement system that produces results consistent with the sensor's input. An example of fitting the measurement data to the equation will be discussed in the Section IV.

III. Materials and Methods

The proposed circuit's performance was evaluated through two separate experiments. The first experiment measured the capacitance of laboratory capacitors, and the second applied the circuit to a cylindrical sensor for paddy rice moisture measurement. A prototype board was utilized in both experiments to allow for flexibility in modifying circuit parameters. A 5.02V DC power supply (V_{cc}) was used, and the NE555 timer IC was incorporated into the design. For the first part of the experiment, laboratory capacitors were employed as the devices under test. Under this condition, it is reasonable to assume that the parasitic resistance of the capacitors (R_x) is sufficiently large ($R_x > R_1$), such that its influence on the circuit operation is negligible. Consequently, the measured output voltage V_{out} is expected to conform closely to the analytical expression provided in Eq. (8). In contrast, in the second part of the experiment, the effect of the sensor's parasitic resistance is anticipated to influence the observed V_{out}. Following an initial examination of the measurement results, Microsoft Excel was subsequently utilized to aid in the calibration and refinement of the sensor-based measurements reported in this paper.

First Experiment: Based on the proposed circuit shown in Fig. 1, the parameters were set as follows: R_a=13kΩ, R_b=495Ω, R_0=100kΩ, R_1=995kΩ, R_L=1kΩ, C_0=100nF, and C_L=100μF. Ceramic capacitors with values ranging from 52.72pF to 807.61pF were used as the target capacitors for testing, and the output voltage V_{out} from the circuit was measured.

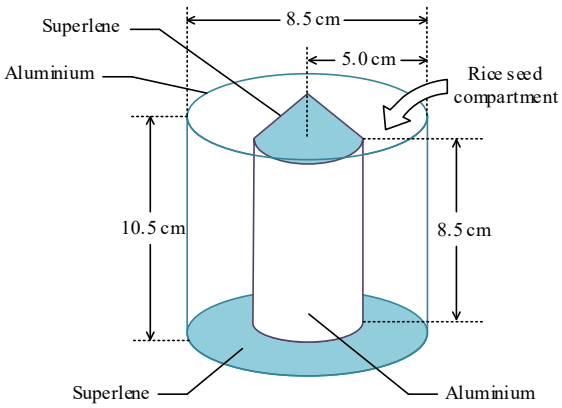


Fig. 5. Moisture sensor structure for paddy rice measurement.

Second Experiment: The parameters were set as follows: R_a=17.98kΩ, R_b=495Ω, R_0=100kΩ, R_1=995kΩ, R_L=1kΩ, C_0=10nF, and C_L=100μF. An aluminum tube was fabricated as a cylindrical sensor for measuring the moisture content of paddy rice, utilizing a capacitive sensor design. A superlene plastic base was used to support the bottom and seal the inner tube, as illustrated in the sketch shown in Fig. 5. To obtain paddy samples with different moisture levels, the sample preparation procedure consisted of four main steps: 1) removing foreign materials and impurities, 2) measuring the initial moisture content, 3) adjusting the moisture level by adding a calculated amount of water, and 4) storing the conditioned samples. After adjustment, each sample was sealed in an airtight zipper bag with as much air removed as possible and then refrigerated at 5 °C for seven days to ensure uniform moisture distribution throughout the grains. Following the conditioning period, the samples were used

for experimentation. The resistance (R_x) and capacitance (C_x) of the sensor were measured using a GW INSTEK LCR-819 at room temperature (25 °C). The sensor was subsequently connected to the proposed circuit, as illustrated in Fig. 6. The outer aluminum tube of the sensor was connected to the circuit ground, while the inner aluminum tube was connected to pins 6 and 7 of the second timer IC (corresponding to the position of C_x). Finally, the output voltage (V_{out}) was measured, and the results were analyzed.

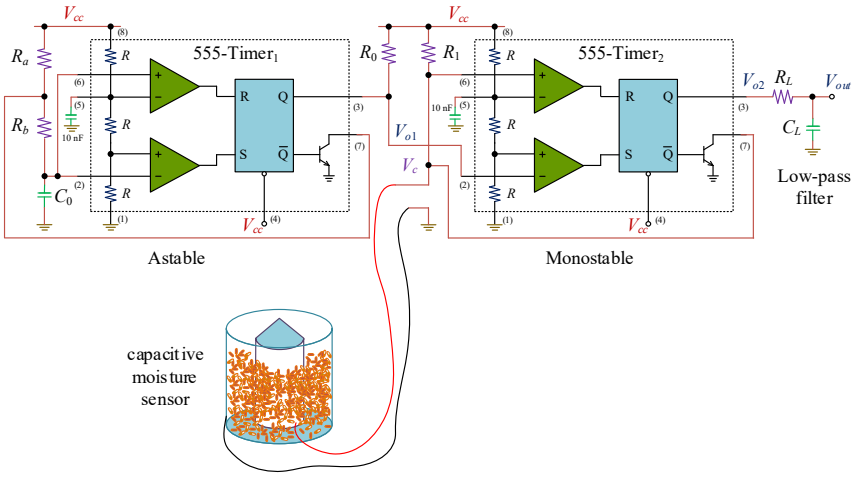
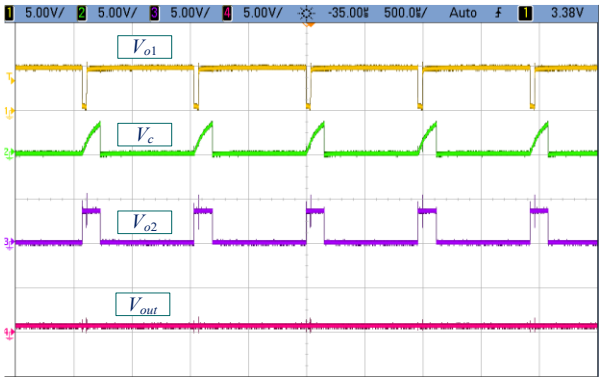


Fig. 6. Connection of the paddy rice moisture sensor to the proposed circuit.

IV. Experimental Results and Discussion

A. First Experiment

An example of the waveform shapes of V_{o1}, V_c, V_{o2}, and V_{out} captured using an oscilloscope for C_x=100pF is shown in Fig. 7. It can be observed that these waveforms align with the sketch illustrated in Fig. 2. Key characteristics of the signals V_{o1} and V_{o2} are presented in Table I. Based on this data, the minimum ($C_{x(min)}$) and maximum ($C_{x(max)}$) capacitance values that the circuit can measure are 31.39 pF and 887.11 pF, respectively. Additionally, for the maximum value of V_{o2} ($V_{o2(max)}$), it is determined that the maximum output voltage (V_{out}) is $V_{o2(max)}$=4.05V.



(Volts/Div.=5V, Time/Div.=500 us)

Fig. 7. Key signals of the circuit observed using an oscilloscope.

Table I: Circuit Features

Key Characteristics	Expected Value	Measured Value
T_1	34.31 µs	40 µs
T_2	935.40 µs	910 µs
T	969.71 µs	950 µs
Du	0.9646	0.958
f	1.0312 kHz	1.053 kHz
$V_{o1\,(max)}$	5.0 V	4.8 V
$V_{o2\,(max)}$	5.0 V	3.8 V

Fig. 8 illustrates the relationship between the measured output voltage (V_{out}) and the capacitance (C_x) obtained using an LCR meter, which is used as the reference and calibration tool for the measurements. The results demonstrate a linear relationship consistent with Eq. (8). The output voltage (V_{out}) exhibits a maximum deviation from the calculated (expected) values of −3.32 % error of full-scale (%FS). However, when integrating the circuit with a digital signal processor (such as a microcontroller), it is common practice to calibrate the system using reference capacitors for testing. In this study, a standard mathematical model based on linear equations in Excel was used for fitting and fine-tuning the relationship. This approach establishes the correlation between the measured capacitance ($C_{x(meas)}$) obtained from the measurement system and the output voltage (V_{out}) as follows:

$$C_{x(\text{meas})} = aV_{\text{out}} + b \tag{19}$$

where a = 241.45 pF/V and b = −29.987 pF.

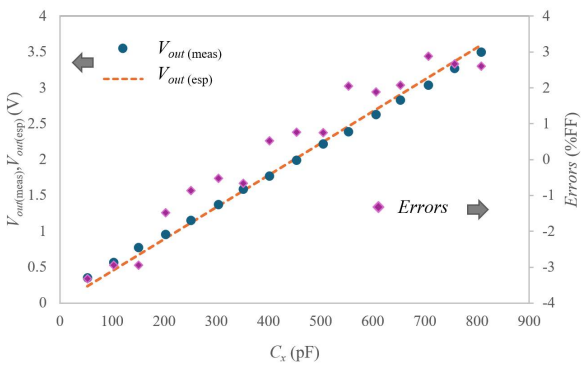


Fig. 8. Relationship between the measured output voltage V_{out} and the tested capacitance values.

This results in the analysis of $C_{x(meas)}$ compared to the experimental capacitance values C_x, as shown in Fig. 9 The

maximum error is 0.92 %FF, which is observed to be lower than the error prior to calibration.

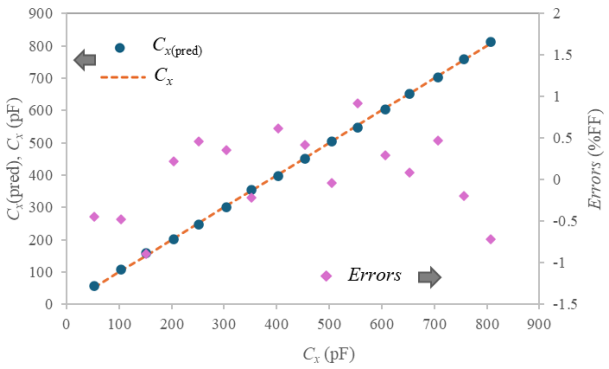


Fig. 9. Results of correlation adjustment using Microsoft Excel.

B. Second Experiment

The results of measuring the moisture content of paddy rice in the range of 12.1% to 23.2% showed that the proposed circuit successfully produced an output voltage (V_{out}). The measured capacitance (C_{sens}) obtained using the LCR meter could also be recorded under the same conditions. However, for the resistance (R_{sens}), it was found that at moisture levels below 15.8%, the measured R_{sens} exceeded 10 MΩ, which was beyond the measurable range of the instrument. In addition, at moisture levels above 21.8%, the measured R_{sens} was lower than twice the value of $2R_1$ used in the circuit (i.e., lower than 1,900 kΩ). According to the theoretical condition (Eq. (16)), the circuit would not be expected to operate properly under these circumstances. Therefore, for the initial comparison between the experimental results and the analysis based on Eq. (17), only the moisture range of 15.8% to 21.8% was considered. Fig. 10 and Fig. 11 illustrate the relationship between the capacitance C_{sens} and resistance (R_{sens}) values measured from the sensor using an LCR meter, and the moisture content of paddy rice (M) obtained from a grain moisture meter (brand KETT PM-450 (Type 4502). From Fig. 10, it can be observed that the capacitance of the sensor does not vary linearly with the moisture content of the paddy rice. By fitting the graph using the polynomial regression in Excel, the resulting relationship is given by:

$$C_{sens} = c_1 M^2 + c_2 M + c_3 \quad (20)$$

where $c_1 = 0.3164$ pF, $c_2 = -4.8173$ pF and $c_3 = 97.351$ pF.

The coefficient of determination (R^2) of the equation is found to be 0.9944. From Fig. 11, it can be observed that the electrical resistance of the sensor decreases as the moisture content of the paddy rice increases, similar to the behavior observed for the capacitance. By fitting the resistance data using the standard exponential function in Excel over the moisture range of 15.8% to 21.8%, the following relationship was obtained:

$$R_{sens} = r_1 M^{r_2} \quad (21)$$

where $r_1 = 7 \times 10^9$ kΩ and $r_2 = -4.952$. The coefficient of determination (R^2) of Eq. (21) was found to be 0.9658.

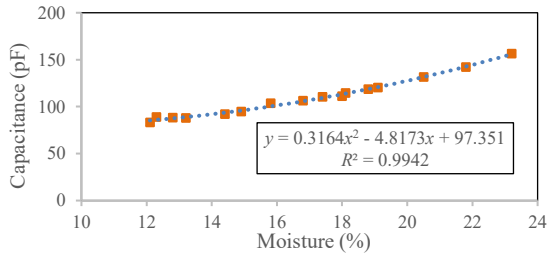


Fig. 10. Measured capacitance of the sensor as a function of paddy rice moisture level.

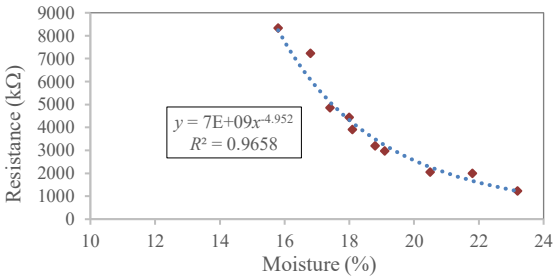


Fig. 11. Measured resistance of the sensor as a function of paddy moisture content.

Fig. 12 shows the results of plotting the output voltage (V_{out}) compared with the values obtained by substituting the measured capacitance and resistance values from the LCR meter, along with the V_{o2max} value from Table I, into Eq. (16). From the figure, it can be observed that the overall trends of the two plotted curves are similar, even though they do not perfectly overlap. We hypothesized that the values of C_{sens} and R_{sens} perceived by the circuit are lower than those measured by the LCR meter. Therefore, we introduced scaling factors to multiply with C_{sens} and R_{sens} before substituting them into Eq. (16). It was found that the scaling factor applied to C_{sens} directly affects the slope of the curve shown in Fig. 12, while the scaling factor applied to R_{sens} can be used to adjust the offset between the two curves. Another observation is that as the moisture content of the paddy rice increases and the resistance R_{sens} decreases, approaching the value of $2R_1$, the difference between the two V_{out} values becomes larger. This is due to the logarithmic (ln) term in Eq. (16). A widely adopted approach for constructing electronic measurement systems that incorporate digital signal processors, such as microcontrollers, with sensor readout circuits is to utilize spreadsheet software like Microsoft Excel to analyze and synthesize empirical relationship equations.

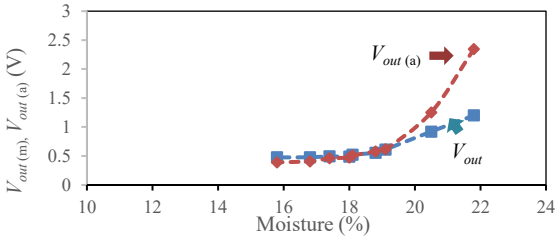


Fig. 12. Correlation between circuit output voltage (V_{out}) and paddy rice moisture level.

In this work, polynomial regression was employed to fit the correlation between the moisture content of paddy rice

(M) and the output voltage (V_{out}). The resulting curve is shown in Fig. 13, and the fitted equation is expressed as:

$$M = 16.039V_{\text{out}}^3 - 58.975V_{\text{out}}^2 + 69.026V_{\text{out}} - 4.4764 \quad (22)$$

By plotting the paddy moisture content obtained from Eq. (22) (denoted as $M_{(22)}$) against the actual moisture content (M_a) measured using the KETT PM-450 grain moisture meter, the results are illustrated in Fig. 14 The maximum deviation (error) observed throughout the entire measurement range was found to be 1.1%.

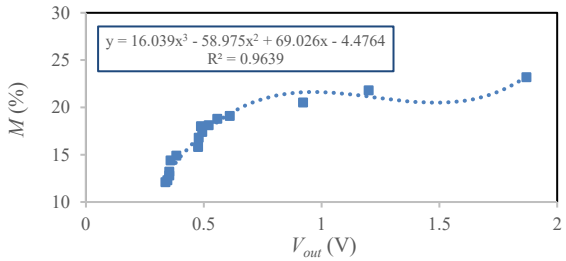


Fig. 13. Polynomial curve fitting result used to establish a functional relationship between paddy rice moisture content (M) and the measured output voltage (V_{out}) of the proposed circuit.

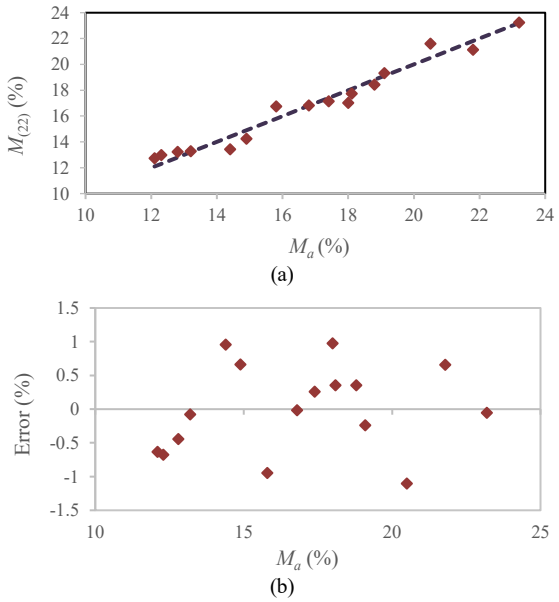


Fig. 14. Evaluated paddy moisture content based on fitted data plotted against original input values: (a) paddy moisture content and (b) estimation error.

V. Conclusions

The proposed Capacitance-to-Voltage Conversion (CVC) circuit was experimentally verified and found to perform in accordance with the theoretical principles presented. In the first phase of testing, it was confirmed that the circuit could convert capacitance values into a DC voltage output with a linear response, as predicted by the analytical models in Eq. (8) and Eq. (9). In the second phase, the circuit was interfaced with a capacitive sensor specifically designed for measuring the moisture content of paddy grains. It was observed that the sensor's capacitance exhibited a nonlinear relationship with respect to moisture content. Additionally, the sensor's parasitic resistance significantly influenced the circuit's output characteristics and thus had to be incorporated into the system modeling. When the measured values of sensor capacitance and parasitic resistance were substituted into the analytical expressions Eq. (17) and Eq. (18), the resulting output voltages closely matched the actual measurements, demonstrating a strong correlation. The practical implementation of the proposed CVC circuit can be readily achieved by interfacing it with a microcontroller-based processing unit, while employing Microsoft Excel as a calibration tool to refine the input–output relationship. As demonstrated in this work, applying polynomial regression of third order or higher enables the fitted model to closely reproduce the measurement results obtained from standard commercial instruments, thereby confirming the suitability of the proposed circuit for integration into low-cost capacitive sensing systems.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Conceptualization, Formal analysis, Anucha Kaewpoonsuk; Circuit implementation and testing, Sudarat Tokampang; Sensor preparation and measurements, Noppadon Sisuk; Writing–original draft, Apinai Rerkratn; Writing–review and editing, Wandee Petchmaneelumka; All authors have read and agreed to the published version of the manuscript.

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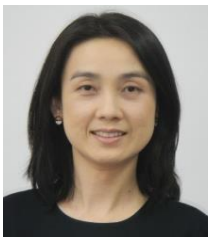

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