On the Design of Differential Difference Transconductance Amplifier (DDTA) and Its Applications

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Manuscript received January 10, 2026; revised February 8, 2026; accepted February 13, 2026
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***Abstract*—This paper presents the design and implementation of a novel active building block termed the Differential Difference Transconductance Amplifier (DDTA). The proposed DDTA integrates the characteristics of the Differential Difference Amplifier (DDA) and the Transconductance Amplifier (TA) to enhance flexibility in analog signal processing. It comprises three TA stages—two forming a DDA structure and one functioning as a TA—allowing independent electronic tuning of transconductance gain (g_m). The DDTA features a simple architecture, wide input capability, extremely high input impedance, and high output resistance at both intermediate and output current terminals, enabling accurate current-mode signal processing with minimal loading effects. To demonstrate its versatility, a voltage-mode universal biquadratic filter and dual-mode quadrature oscillator, both based on a single DDTA and utilizing only two capacitors, have been designed and simulated. PSPICE simulation results confirm wide linear voltage-to-current conversion, wideband transconductance performance, and robust impedance characteristics, all in excellent agreement with theoretical predictions. These features validate the effectiveness and practicability of the proposed approach for modern analog circuit designs.**

***Index Terms*—Differential Difference Transconductance Amplifier (DDTA), transconductance amplifier, analog Integrated Circuit (IC), electronic tunability, multifunction filter**

I. Introduction

The continuous scaling of CMOS technologies and the rapid expansion of wireless communication, Internet of Things (IoT), and low-power biomedical systems have renewed interest in compact, electronically tunable analog building blocks capable of operating under low supply voltages while ensuring wide bandwidth and high signal integrity. In recent literature [1–5], this demand has been further emphasized by the need for Voltage-Mode (VM) and Current-Mode (CM) signal processing blocks that simultaneously provide high-input impedance, accurate current transfer, and reduced component count, particularly for filters and oscillators implemented in deep-submicron CMOS technologies.

A wide variety of Active Building Blocks (ABBs) have been developed and refined over the past decades, including Current Conveyors (CCs) [6], Operational Transconductance Amplifiers (OTAs) [7], Differential Difference Amplifiers (DDAs) [8], Differential Difference Current Conveyors (DDCCs) [9, 10], Current Feedback Operational Amplifiers (CFOAs) [11, 12], Voltage Differencing Transconductance Amplifiers (VDTAs) [13, 14], and Voltage Differencing Gain Amplifiers (VDGAs) [15–17]. Recent focused on ABB as referenced in [1–5, 18, 19] have concentrated on low-voltage operation, enhanced electronic tunability, multi-input capability, and mixed-mode functionality, which confirms that ABB research remains an active and evolving field rather than a mature or saturated topic.

Among these ABBS, the Differential Difference Transconductance Amplifier (DDTA) has garnered increasing attention because it inherently combines multi-input voltage differencing with transconductance-based current outputs. This feature is particularly attractive for modern analog signal-processing systems [20]. Recent DDTA-based designs have demonstrated low-power mixed-mode filters, shadow filters, and oscillators with wide electronic tunability and reduced passive component count [1, 2, 5, 19]. Furthermore, fully differential DDTA architecture employing inverter-based CMOS realizations has been reported to improve low-voltage operation and power efficiency [3]. These findings demonstrate that DDTA-based circuits continue to be significant in recent research.

Despite this progress, a critical review of recent works reveals several persistent limitations. Many reported DDTAs provide only limited flexibility in controlling transconductance control, depend on a single bias parameter, or exhibit reduced output resistance at intermediate nodes when adapted to multi-input or mixed-mode configurations [1–3, 5]. To overcome these issues, alternative ABBs, such as Differential Difference Gain Amplifier (DDGA) and advanced VDTA-based structures, have been proposed to improve electronic control and multifunction capability [21, 22]. However, these solutions often lead to increased circuit complexity or introduce internal node loading, which can degrade CM accuracy in cascade applications.

This paper introduces a new CMOS implementation of a DDTA, motivated by these observations and the

continued relevance of DDTA-focused research. The proposed design employs three independent controllable transconductance stages, which enables flexible voltage differencing and current conversion while achieving very high input and high output impedances at both intermediate and output terminals. These characteristics effectively address the limitations found in current DDTA designs and correspond with the dominant design trends observed in recent ABB literature. To demonstrate the effectiveness of the proposed DDTA, two representative applications are suggested: (i) a single-DDTA VM universal biquadratic filter and (ii) a single-DDTA dual-mode quadrature oscillator, both realized using only two capacitors. Simulation results indicate that the proposed DDTA achieves performance that is competitive with, and in several aspects superior to, recent ABB-based implementations previously reported, particularly regarding impedance characteristics, electronic tunability, and component efficiency.

II. DDTA Conception and Description

The circuit diagram of the introduced DDTA is illustrated in Fig. 1. It features four high-impedance voltage input terminals (p_1, n_1, p_2, and n_2) and four high-impedance current output terminals (z+, z−, x+, and x−). The differential voltages (v_{p1}−v_{n1}) and (v_{p2}−v_{n2}) are converted into output currents at the z+ and z− terminals through the transconductance gains (g_{mF} and g_{mS}) of the first and second stages, respectively. The voltage across the z+ terminal is then transmitted to the third transconductor stage, where it is converted into output currents at the x+ and x- terminals (i_{x+} and i_{x-}) via the third-stage transconductance gain (g_{mT}). Based on the operation of the DDTA, its characteristic equation can be expressed as follows:

$$\begin{aligned} i_{z+} &= -i_{z-} = g_{mF}\left(v_{p1} - v_{n1}\right) - g_{mS}\left(v_{p2} - v_{n2}\right) \\ i_{x+} &= -i_{x-} = g_{mT} v_{z+} \end{aligned} \quad (1)$$

Eq. (1) reveals that both stages of differential input voltages are transformed into output currents through electronically controllable transconductance gains. This feature provides remarkable flexibility, making the DDTA particularly suitable for implementation in various analog circuits. Such adaptability enables analog designers to optimize performance for specific applications and solutions, including active amplifiers, tunable filters, and oscillators. As a result, the DDTA enhances functionality while minimizing the need for additional components, thereby streamlining circuit design and improving overall efficiency. The behavior model of the proposed DDTA is represented using simplified circuit blocks in Fig. 2, as indicated by Eq. (1).

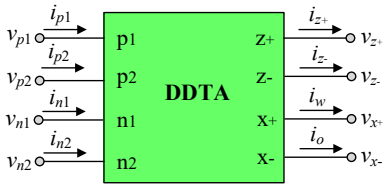


Fig. 1. Circuit diagram of the proposed DDTA.

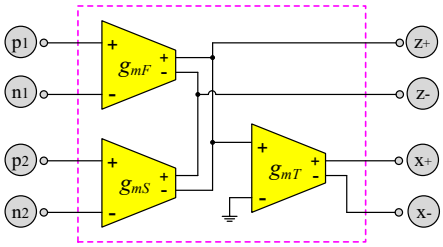


Fig. 2. Simplified block diagram of the DDTA.

Fig. 3 presents the CMOS-level circuit realization of the proposed DDTA based on the model presented in Fig. 2. The designed circuit consists of three transconductance gain cells, constructed using floating current sources M_{k1}–M_{k13} where k denotes F (first), S (second), and T (third) [23]. Transistors M_{k3}–M_{k4} and M_{k7}–M_{k8} serve as cascode devices and are for the signal path (input differential transistors, M_{k1}–M_{k2}). This configuration establishes M_{k3}–M_{k4} in a folded-cascode or gain-boosting g_m cell. Cascoding maintain the drain of M_{k1}–M_{k2} at a constant, higher voltage, which increases their intrinsic gain. By shielding the drain of M_{k1}–M_{k2} from large voltage swings, M_{k3}–M_{k4} keep V_{DS} of M_{k1}–M_{k2} nearly constant, reduce channel-length modulation (λ) effects, and ensure more accurate voltage-to-current conversion. This enhancement leads to an improved Common-Mode Rejection Ratio (CMRR) and greater linearity in the transconductance amplifier.

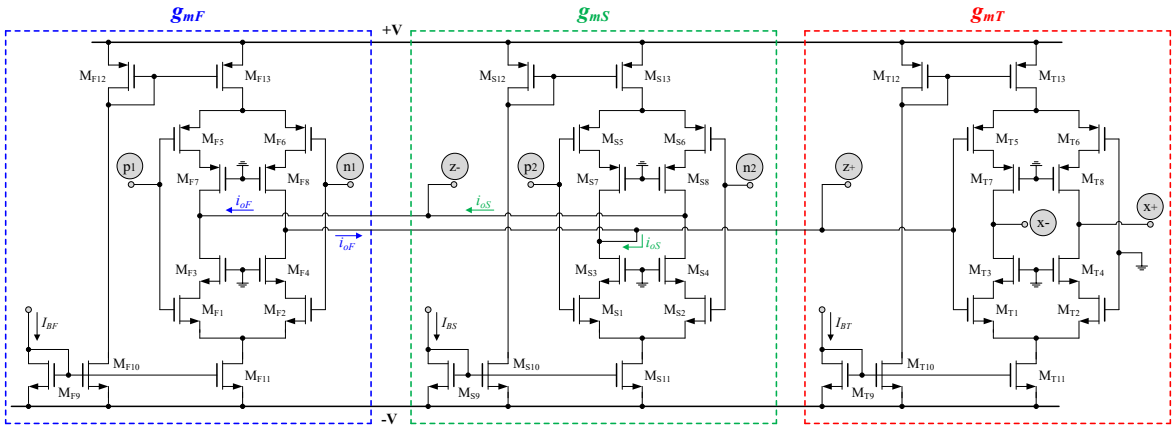


Fig. 3. CMOS transistor-level realization of the proposed DDTA.

M_{k7}–M_{k8} act as cascode devices for the bias tail current sources (M_{k5}–M_{k6}). They isolate the current-source transistors M_{k5}–M_{k6} from the large voltage variations occurring at the drains of M_{k1}–M_{k2}. This configuration stabilizes the bias current and improves g_m consistency. Also, M_{k7}–M_{k8} prevents signal variations in the differential pair from coupling back into the current source bias circuitry, which ultimately reduces distortion and noise.

Considering the symmetric transistors ($M_{k1} \approx M_{k2}$, $M_{k3} \approx M_{k4}$, $M_{k5} \approx M_{k6}$, and $M_{k7} \approx M_{k8}$) and the finite channel output resistance r_{ok1} of the input transistor M_{k1}, the small-signal current generated by the differential pair is partially lost through r_{ok1} due to variations in the drain-node voltage. Let R_{node} denote the equivalent resistance seen at the drain of M_{k1} when looking into the cascode and mirror/load network. The effective small-signal transconductance gain g_{mk} realized by each tunable gain cell (M_{k1}–M_{k13}) is then obtained as:

$$g_{mk} = g_{m0}\left(\frac{1}{1+R_{node}/r_{o1}}\right), \tag{2}$$

where g_{m0} is the intrinsic transconductance of the tunable gain cell and may be approximated as:

$$g_{m0} \cong \left(\frac{g_{mk1}g_{mk2}}{g_{mk1}+g_{mk2}}\right)+\left(\frac{g_{mk5}g_{mk6}}{g_{mk5}+g_{mk6}}\right). \tag{3}$$

In Eq. (3), the equation for g_{mki} is expressed as $g_{mki} = (\mu C_{ox} W_i I_{Bk}/L_i)^{1/2}$, for i = 1, 2, and 3. Here, I_{Bk} represents the external DC bias current, μ denotes the free carrier mobility in the channel, and C_{ox} is the gate-oxide capacitance per unit area, while W_i and L_i refer to the channel width and length of the transistor M_{ki}, respectively. According to Eq. (2) and Eq. (3), the tunability of g_{mk} is typically achieved by adjusting the associated bias current I_{Bk}.

The resistance R_{node} is primarily influenced by the cascode transistor M_{k3} and can be determined as:

$$R_{node} \cong r_{ok1}\left(1+g_{mk3}r_{o3}\right)+r_{ok3} \cong r_{ok1}\left(1+g_{mk3}r_{ok3}\right), \tag{4}$$

with g_{mk3} and r_{ok3} being the transconductance and output resistance of the cascode device M_{k3}.

Since both transistors M_{k7} and M_{k8} are the tail cascode for the current source and each output node (z+, z-, x+, and x-) is the drain of a stack that includes an output transistor and a cascode transistor above or below, the output resistance observed at the terminal z+ (R_{z+}) is derived as:

$$R_{z+} \cong \left[g_{mF4}r_{oF4}r_{oF2}\left(1+g_{mF8}r_{oF8}\right)\right] // \left[g_{mS3}r_{oS3}r_{oS1}\left(1+g_{mS7}r_{oS7}\right)\right], \tag{5}$$

The note above indicates that the factors $g_{mF4}r_{oF4}$ (or $g_{mS3}r_{oS3}$) arise from the cascode gain-boost of M_{F4} (M_{S3}), while r_{oF2} (or r_{oS1}) is the intrinsic output resistance of the output transistor (r_o). Additionally, the terms $(1+g_{mF8}r_{oF8})$ and $(1+g_{mS7}r_{oS7})$ reflect the finite output resistances attributed to the tail current-source cascodes M_{F8} and M_{S7}, respectively.

Similarly, the output resistances for the terminals z-, x+, and x- can be found as, respectively,

$$R_{z-} \cong \left[g_{mF3}r_{oF3}r_{oF1}\left(1+g_{mF7}r_{oF7}\right)\right] // \left[g_{mS4}r_{oS4}r_{oS2}\left(1+g_{mS8}r_{oS8}\right)\right] \tag{6}$$

$$R_{x+} \cong g_{mT4}r_{oT4}r_{oT2}\left(1+g_{mT8}r_{oT8}\right), \tag{7}$$

$$R_{x-} \cong g_{mT3}r_{oT3}r_{oT1}\left(1+g_{mT7}r_{oT7}\right). \tag{8}$$

III. Functional Verification and Simulation Results

The performance of the proposed DDTA in Fig. 3 was verified through PSPICE simulation using the 0.25-μm TSMC CMOS process parameter. The supply voltages were set to ±1 V. The aspect ratio of all MOS transistors employed in the DDTA circuit are summarized in Table I. Based on the designed simulation parameters, the total power dissipation for the proposed DDTA is measured at 3.07 mW.

Table I: Transistor Aspect Ratios (W/L) for the DDTA in Fig.3

Transistors	W/L (μm/μm)
M_{1k}, M_{2k}	16/0.25
M_{3k}, M_{4k}, M_{7k}, M_{8k}	55/0.25
M_{5k}, M_{6k}	40/0.25
M_{9k}–M_{11k}	2/0.25
M_{12k}, M_{13k}	3/0.25

To demonstrate electronic tunability, the bias currents of three transconductance stages, namely I_{BF}, I_{BS}, and I_{BT}, were independently adjusted. For the sake of simplicity in verification, all three transconductance gains were set to be equal, i.e., $g_m = g_{mF} = g_{mS} = g_{mT}$ with $I_B = I_{BF} = I_{BS} = I_{BT}$. The selected transconductance values were 0.691, 0.865, 1.000, and 1.150 mA/V, which corresponded to bias currents of 40, 70, 100, and 140 μA, respectively. The calculated and simulated transconductance gains under different bias currents are compared in Table II.

Table II: Theory and Simulated Values of the Transconductance Gain at Different Bias Current Values

I_B (μA)	g_m (mA/V)	
	Theory	Simulated
40	0.691	0.700
70	0.865	0.877
100	1.000	0.997
140	1.150	1.113

The DC voltage-to-current transfer characteristics were evaluated by sweeping the differential input voltage (v_{p1}–v_{n1}) while keeping (v_{p2}–v_{n2}) constant at 30 mV (peak). The resulting output currents at terminals z+ and z- are shown in Fig. 4, which demonstrates a highly linear voltage-to-current conversion over an input range of approximately ±150 mV. Within this range, the deviation from ideal linear behavior remains below ±1.5%, indicating excellent DC linearity of the proposed DDTA. Moreover, the output currents are equal in magnitude and opposite in phase, which confirms accurate differential-to-current conversion in accordance with the theoretical DDTA operation.

A similar procedure was conducted by sweeping (v_{p2}–v_{n2}) while maintaining (v_{p1}–v_{n1}) at a fixed value of 30 mV (peak). The corresponding responses shown in

Fig. 5 again demonstrate a wide linear input range of ±150 mV, with a maximum nonlinearity error of less than 2%, further validating the symmetry and independence of the two differential input stages. The small nonlinearity implies low harmonic distortion during large-signal operation. Hence, the DDTA is expected to exhibit low Total Harmonic Distortion (THD) in practical signal-processing applications, particularly within the verified linear operating range. Furthermore, the slopes of the DC transfer characteristics are in strong agreement with the programmed g_m values listed in Table II. This confirms that the output current scaling in Fig. 4 and Fig. 5 is effectively determined by the electronically tunable g_m. Since g_m is controlled by external bias currents, temperature-induced variations can be partially compensated through bias-current adjustment or bias stabilization circuits, which are common in CMOS analog designs.

Next, the AC behavior of the transconductance was analyzed under various bias conditions. Fig. 6 shows the simulated frequency responses for the selected transconductance values. The extracted transconductance values were approximately 0.700, 0.877, 0.997, and 1.113 mA/V, respectively, and remained almost constant over the frequency range from 1 kHz to 30 MHz. A gradual roll-off was observed beyond 30 MHz, while stable operation was preserved up to around 100 MHz, demonstrating the wideband capability of the proposed DDTA.

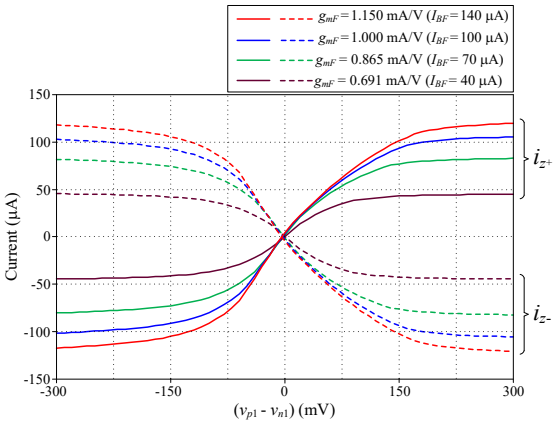


Fig. 4. DC transfer characteristic of the proposed DDTA, displaying the output currents i_{z+} and i_{z-} in relation to (v_{p1}–v_{n1}).

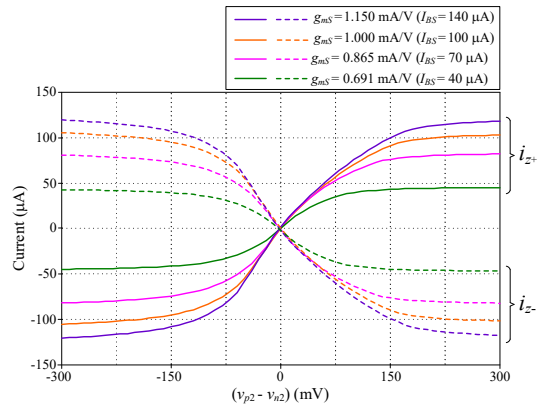


Fig. 5. DC transfer characteristic of the proposed DDTA, displaying the output currents i_{z+} and i_{z-} in relation to (v_{p2}–v_{n2}).

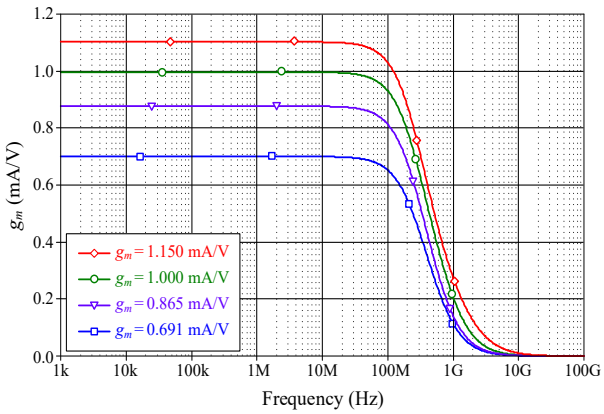


Fig. 6. AC frequency characteristic of the transconductance g_m.

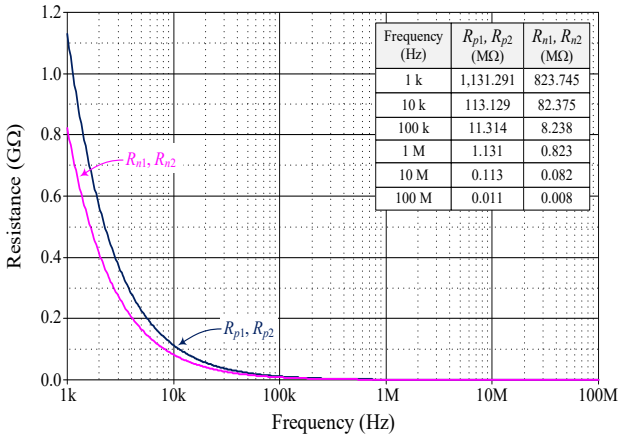
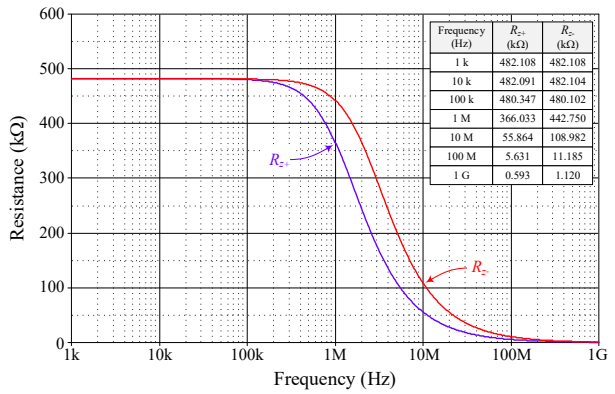


Fig. 7. Frequency behavior of the DDTA input resistances (R_{p1}, R_{p2}, R_{n1}, and R_{n2}).

In addition to evaluating the transconductance performance, the frequency-dependent behaviors of the input and output impedances were also investigated and are shown in Fig. 7 to Fig. 9. As depicted in Fig. 7, the input resistances at terminals p1, p2, n1, and n2 (R_{p1}, R_{p2}, R_{n1}, and R_{n2}) remain exceptionally high at low and mid frequencies, with values exceeding 1 GΩ at 1 kHz and remaining above 1 MΩ up to 1 MHz. This finding confirms the excellent voltage-mode input characteristics of the proposed DDTA and ensures negligible loading effects when interfacing with subsequent stages. A gradual reduction in input resistance is observed beyond 10 MHz due to the influence of parasitic capacitances; however, the resistance still remains in the tens-of-kilo-ohms range even at 100 MHz, which is sufficient for most high-frequency analog applications.

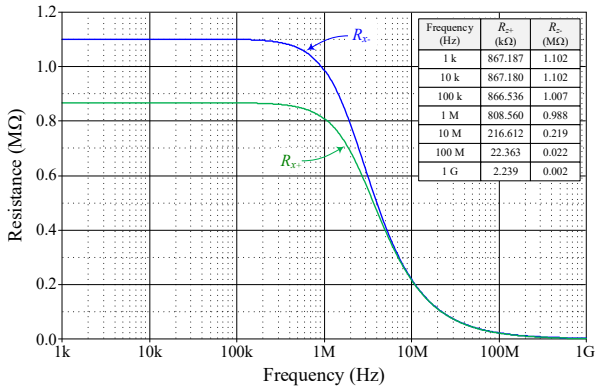
The frequency characteristics of the output resistances at the z+ and z- terminals (R_{z+} and R_{z-}) are depicted in Fig. 8. At low frequencies, both terminals exhibit high output resistances of approximately 482 kΩ, which remain well above 300 kΩ up to 1 MHz. This supports the effectiveness of the cascode-assisted current-source configuration predicted by the analytical expressions in Eq. (5) and Eq. (6). At higher frequencies, the output resistance gradually decreases; nevertheless, sufficiently large resistance values are still preserved for reliable current-mode signal processing.



Frequency (Hz)	R_{z+} (kΩ)	R_{z-} (kΩ)
1 k	482.108	482.108
10 k	482.091	482.104
100 k	480.347	480.102
1 M	366.033	442.750
10 M	55.864	108.982
100 M	5.631	11.185
1 G	0.593	1.120

Fig. 8. Frequency behavior of the DDTA output resistances (R_{z+} and R_{z-}).

Similarly, Fig. 9 shows the frequency behavior of the output resistance at the x+ and x- terminals (R_{x+} and R_{x-}). The resistance R_{x+} measures approximately 867 kΩ at 1 kHz and remains higher than 800 kΩ up to 1 MHz, while the resistance R_{x-} exhibits an even higher value exceeding 1 MΩ over the same frequency range. These results verify the strong current-source behavior of the third transconductance stage. The decrease in output resistance observed at frequencies above 10 MHz is again attributed to high-frequency parasitic effects. Nonetheless, the overall impedance performance indicates that the proposed DDTA maintains high input and output impedances over a wide frequency range, which is essential for achieving accurate signal processing, high isolation between stages, and minimal interaction with external loads in practical analog circuit implementations.



Frequency (Hz)	R_{x+} (kΩ)	R_{x-} (MΩ)
1 k	867.187	1.102
10 k	867.180	1.102
100 k	866.536	1.007
1 M	808.560	0.988
10 M	216.612	0.219
100 M	22.363	0.022
1 G	2.239	0.002

Fig. 9. Frequency behavior of the DDTA output resistances (R_{x+} and R_{x-}).

IV. DDTA Circuit Applications

This section demonstrates the applicability of the proposed DDTA through two example circuits: (i) a voltage-mode Triple-Input Single-Output (TISO) universal biquadratic filter and (ii) a dual-mode quadrature oscillator. Both configurations employ only a single DDTA together with only two capacitors, making them well suited for a compact design with a minimum component count.

A. Single DDTA-Based TISO Universal Biquadratic Filter

Fig. 10 illustrates the TISO universal biquadratic filter, which is implemented using one DDTA and two capacitors without needing any passive resistors. This topology is attractive for IC implementation due to its structural simplicity, reduced silicon area, and electronic tunability. Straightforward circuit analysis leads to the following voltage transfer function:

$$V_{\text{out}}(s)=\frac{\left[s^2+\left(\frac{g_{\text{mS}}}{C_2}\right)s\right]V_{i1}-\left(\frac{g_{\text{mT}}}{C_1}\right)sV_{i2}+\left(\frac{g_{\text{mF}}g_{\text{mT}}}{C_1C_2}\right)V_{i3}}{D(s)}, \quad (9)$$

where

$$D(s)=s^2+\left(\frac{g_{\text{mS}}}{C_2}\right)s+\left(\frac{g_{\text{mF}}g_{\text{mT}}}{C_1C_2}\right). \quad (10)$$

From the above expressions, the natural angular frequency (ω_o) and quality factor (Q) can be determined by:

$$\omega_o=2\pi f_o=\sqrt{\frac{g_{\text{mF}}g_{\text{mT}}}{C_1C_2}}, \quad (11)$$

$$Q=\left(\frac{1}{g_{mS}}\right)\sqrt{\frac{g_{mF}g_{mT}C_1}{C_2}}. \quad (12)$$

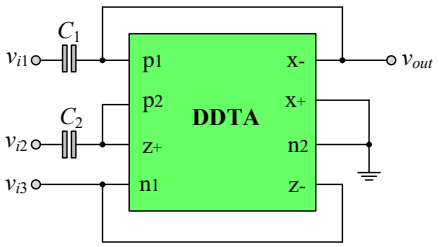


Fig. 10. Single DDTA-based TISO universal biquadratic filter configuration.

These results indicate that the filter parameter ω_o can be electronically adjusted using g_{mF} and g_{mT}, while the Q factor can be independently controlled through g_{mS} without disturbing ω_o. This capability for orthogonal tuning is a highly desirable feature in practical filter design.

By appropriate selection of the input voltages v_{i1}, v_{i2}, and v_{i3}, the suggested TISO filter can achieve all five standard biquadratic filter functions, i.e., Lowpass (LP), Bandpass (BP), Highpass (HP), Bandstop (BS), and Allpass (AP), at a single output terminal v_{out}. The specific input conditions required for each response are summarized in Table III.

To validate analysis, the realized filter shown in Fig. 10 was simulated using the proposed DDTA with g_m = g_{mF} = g_{mS} = g_{mT} = 1 mA/V (corresponding to I_B = 100 μA) and C_1 = C_2 = 100 pF. These parameters yield a theoretical natural angular frequency of f_o = 1.59 MHz with Q = 1. The maximum power consumption of the suggested TISO filter was found to be 3.09 mW. Fig. 11 shows the simulated gain-frequency responses for the LP, BP, HP, and BS configurations. All responses closely follow the ideal characteristics, with a simulated f_o of approximately 1.57 MHz. The small deviation from the

expected value is attributed mainly to parasitic impedances and nonideal transconductance behavior at high frequencies. The results confirm that the proposed filter achieves accurate pole placement and correct frequency selectivity using a single DDTA.

TABLE III: INPUT VOLTAGE SELECTION FOR EACH FILTER TYPE CONFIGURATION

Filter type	v_{i1}	v_{i2}	v_{i3}	Matching condition	Transfer function, $V_{out}(s)/V_{in}(s)$
LP	0	0	v_{in}	no	$\frac{(g_{mF}g_{mT})/(C_1C_2)}{D(s)}$
BP	0	v_{in}	0	no	$-\frac{(g_{mT}/C_1)s}{D(s)}$
HP	v_{in}	v_{in}	0	no	$s^2/D(s)$
BS	v_{in}	v_{in}	v_{in}	$g_{mS}=g_{mT}$, $C_1=C_2$	$\frac{s^2+(g_{mF}g_{mT})/(C_1C_2)}{D(s)}$
AP	v_{in}	$2v_{in}$	v_{in}	$g_{mS}=g_{mT}$, $C_1=C_2$	$\frac{s^2-\left(\frac{g_{mS}}{C_2}\right)+\left(\frac{g_{mF}g_{mT}}{C_1C_2}\right)}{D(s)}$

Note: v_{in} = input voltage signal, 0 = ground potential.

The AP response is depicted in Fig. 12. As expected, the gain response remains nearly constant over the frequency range of interest, while the phase response exhibits the desired frequency-dependent variation. The simulated phase transition aligns closely with the theoretical predictions, indicating the suitability of the proposed topology for phase-sensitive applications such as phase equalization and signal alignment.

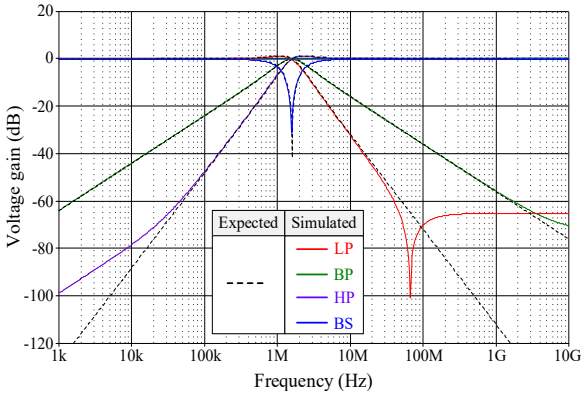


Fig. 11. Simulated gain responses of the LP, BP, HP, and BS filter outputs.

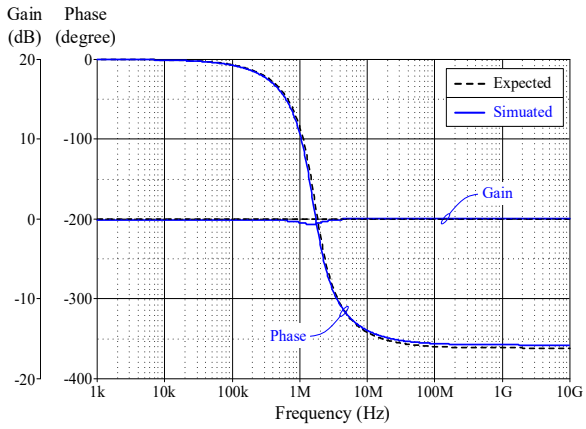


Fig. 12. Simulated frequency responses of the AP filter output.

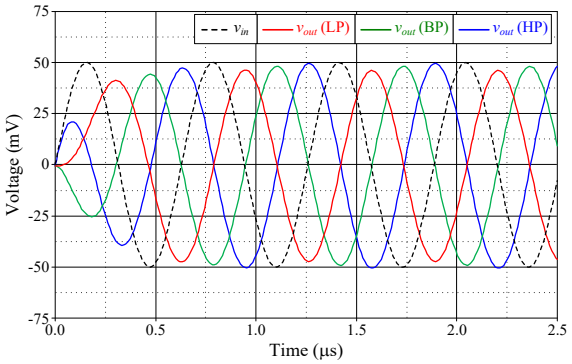


Fig. 13. Time-domain responses of the LP, BP, and HP filter outputs.

In Fig. 13, time-domain verification is presented, where a 50-mV sinusoidal input signal at 1.59 MHz is applied to the LP, BP, and HP filters. The output waveforms exhibit stable sinusoidal behavior without observed distortion or clipping, confirming linear operation within the intended signal range.

B. Single DDTA-Based Dual-Mode Quadrature Oscillator

As a second illustrative application, a compact dual-mode quadrature oscillator based on utilizing a single DDTA and only two grounded capacitors is shown in Fig. 14. Owing to its minimal component count and absence of resistors, the proposed topology is well suited for IC implementation. The configuration simultaneously generates both voltage and current outputs, thereby both voltage and current-mode signal processing within a unified structure. By routine circuit analysis, the characteristic equation of the oscillator can be derived as:

$$s^2+\left(\frac{g_{mS}-g_{mF}}{C_1}\right)s+\left(\frac{g_{mF}g_{mT}}{C_1C_2}\right)=0, \tag{13}$$

from which the condition for oscillation (CO) is obtained as:

$$g_{mS}=g_{mF}. \tag{14}$$

The angular frequency of oscillation is defined as:

$$\omega_{osc}=2\pi f_{osc}=\sqrt{\frac{g_{mF}g_{mT}}{C_1C_2}}. \tag{15}$$

These relations indicate that the CO can be tuned via control transconductance g_{mS} (adjusting I_{BS}), while ω_{osc} is independently adjusted through g_{mF} and g_{mT}. This orthogonal tunability offers clear design flexibility.

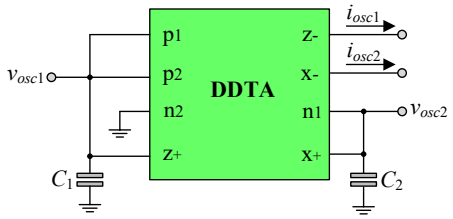


Fig. 14. Single DDTA-based dual-mode quadrature oscillator.

Furthermore, the relationships between the quadrature voltage and current outputs are described by:

$$\frac{V_{\text{osc2}}(s)}{V_{\text{osc1}}(s)} = \frac{g_{\text{mT}}}{sC_2}, \tag{16}$$

$$\frac{I_{\text{osc2}}(s)}{I_{\text{osc1}}(s)} = \frac{g_{\text{mT}}}{sC_1}, \tag{17}$$

which confirm the theoretical phase difference of 90° between the corresponding output signals.

For verification, the oscillator circuit in Fig. 14 was designed with parameters g_m = 1 mA/V and C_1 = C_2 = 100 pF, yielding a designed oscillation frequency of f_{osc} = 1.59 MHz. The simulated time-domain waveforms during the transient state for both quadrature voltage and current outputs are shown in Fig. 15. The waveforms exhibit stable oscillatory behavior with steady-state operation established within approximately 45 μs, confirming reliable startup under the derived oscillation condition.

The steady-state waveforms given in Fig. 16 reveal sinusoidal outputs with an oscillation frequency of about f_{osc} = 1.60 MHz, which closely matches the theoretical prediction. The measured phase differences are approximately 92° for the voltage outputs and 88° for the current outputs, reflecting phase errors of less than 2.30%. These small deviations are mainly attributed to device nonidealities and parasitic capacitances. The observed phase errors can be further reduced through careful device matching, symmetric layout techniques, and fine bias-current tuning, which help mitigate mismatch and parasitic effects.

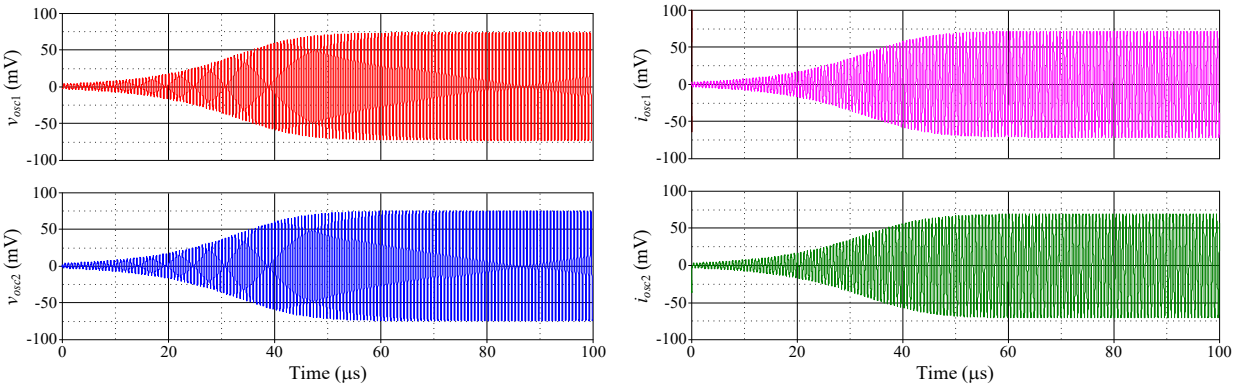


Fig. 15. Transient waveforms for quadrature outputs: (a) voltage-mode operation; (b) current-mode operation.

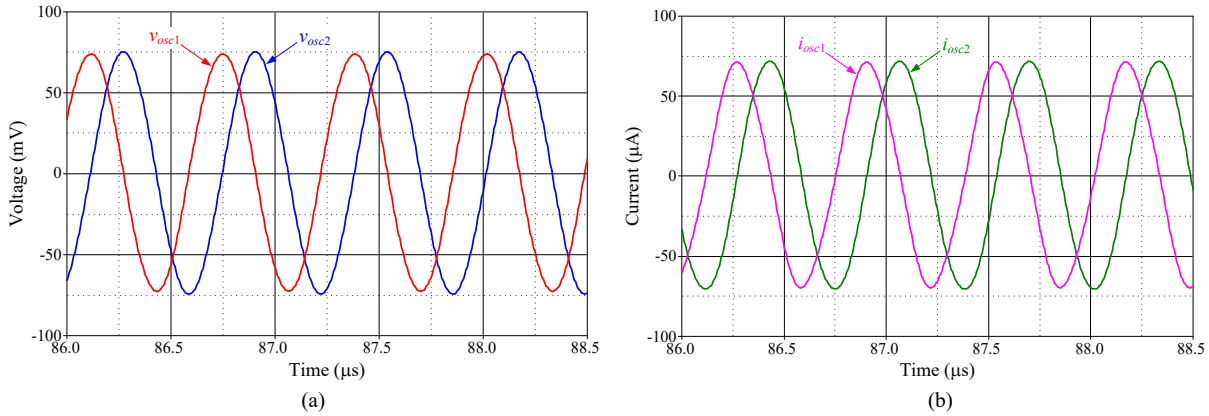


Fig. 16. Steady-state waveforms of quadrature outputs: (a) voltage-mode operation; (b) current-mode operation.

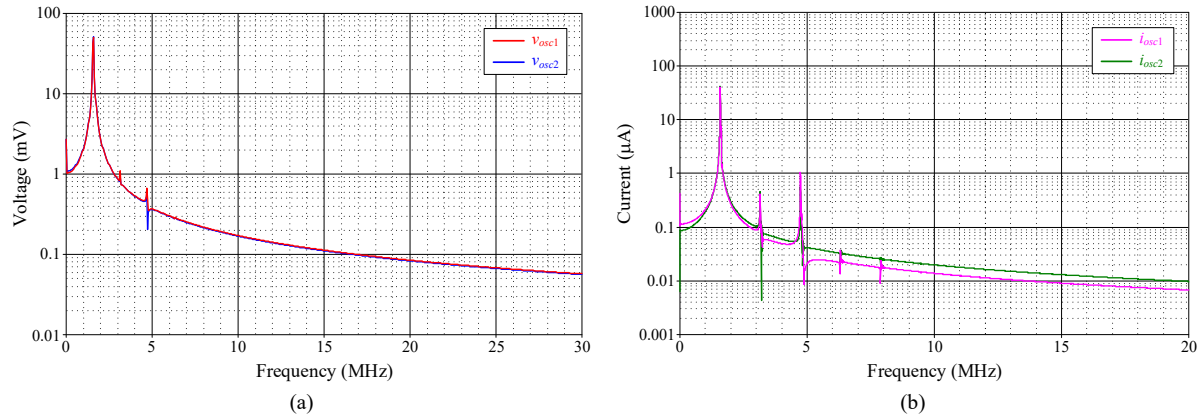


Fig. 17. Frequency spectra of quadrature outputs: (a) voltage-mode operation; (b) current-mode operation.

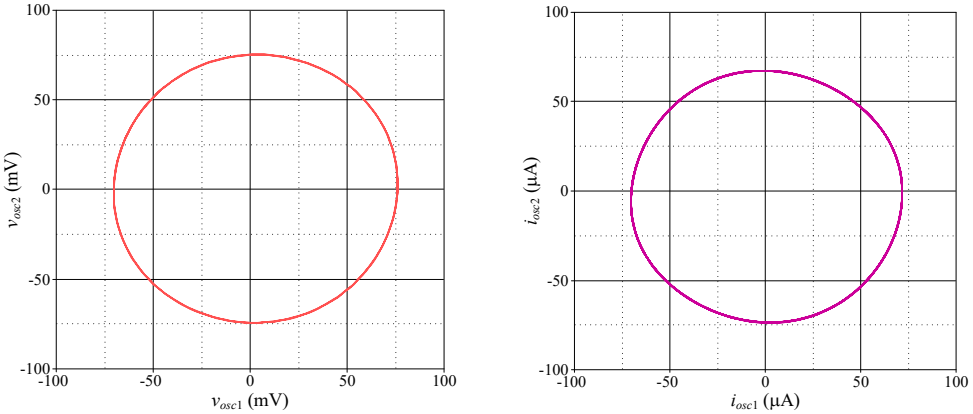


Fig. 18. Lissajous plots demonstrating quadrature phase relationship: (a) voltage-mode operation; (b) current-mode operation.

Fig. 17 displays the corresponding frequency spectra of the quadrature outputs. The dominant spectra components occur at the oscillation frequency, while higher-order harmonics are significantly suppressed. The Total Harmonic Distortion (THD) is approximately 0.96% for the voltage-mode outputs and 2.31% for the current-mode outputs, indicating good spectra purity suitable for practical quadrature signal generation.

Finally, the quadrature relationship is further validated by the Lissajous plots depicted in Fig. 18. The nearly circular trajectories observed for both VM and CM outputs verify the close-to-ideal 90° phase shift and amplitude balance; thereby validating the correct quadrature operation of the proposed oscillator.

V. Conclusion

This paper presents the design and implementation of a novel active building block termed the Differential Difference Transconductance Amplifier (DDTA). The proposed DDTA combines the functional features of the Differential Difference Amplifier (DDA) and the Operational Transconductance Amplifier (OTA) to provide multiple differential voltage inputs and electronically tunable transconductance outputs within a compact and symmetrical structure. The use of independent bias currents enables precise electronic tuning of all transconductance stages, thereby offering enhanced flexibility for a wide range of analog signal-processing applications.

Comprehensive DC, AC, and impedance simulations have confirmed the theoretical performance of the proposed DDTA. The device exhibits wide linear input voltage ranges, accurate voltage-to-current conversion, and a transconductance that remains nearly constant up to 30 MHz, demonstrating wideband capability. In addition, the DDTA achieves extremely high input resistance in the giga-ohm and mega-ohm ranges and high output resistances at both the z- and x-terminals over a broad frequency range, which are direct consequences of the cascode-enhanced transconductance and current-mirror architectures. These high impedances significantly reduce loading effects, improve signal isolation between stages, and ensure high accuracy in current-mode signal transmission.

The effectiveness of the proposed DDTA has been further validated by realizing a single-DDTA voltage-mode universal biquadratic filter and a dual-mode quadrature oscillator, both of which utilize only two capacitors. The close agreement between theoretical predictions and PSPICE simulation results confirms the validity, robustness, and practical feasibility of the proposed DDTA as a versatile active building block for modern low-voltage analog IC designs. As a direction for future work, the proposed DDTA can be further developed toward ultra-low-voltage and low-power realizations by utilizing inverter-based or bulk-driven CMOS techniques. In addition, exploring fully differential DDTA architectures may improve noise immunity, dynamic range, and robustness against process variations. To validate the practical feasibility and performance of the proposed DDTA-based circuits, experimental confirmation through IC fabrication and measurement is also planned.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

O. Channumsin, P. Yaruan, and W. Tangsrirat contributed the conceptual framework for the circuit idea. O. Channumsin gathered all the necessary information. P. Yaruan conducted an audit and reported on pertinent research articles. O. Channumsin, P. Yaruan, and W. Tangsrirat performed simulations, finalized the research, and authored this manuscript. W. Tangsrirat provided guidance and supervision throughout the research process and analysis. All authors reviewed and approved the final version of the manuscript.

Funding

This research project is supported by Rajamangala University of Technology Isan, Contract No. ENG 9/69.

Acknowledgment

The corresponding author expresses gratitude for the support and resources provided by the School of

Engineering at King Mongkut's Institute of Technology Ladkrabang, which contributed to the completion of this work.

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