Evaluation and Optimization of Novel Graphene Nanosheet FET: Analog/RF Perspectives

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***Abstract*—Graphene Nano-Sheet Field Effect Transistor (GNSFET) is designed using a new material (graphene) in the channel, marking advancement in Nano-Sheet Field Effect Transistor (NSFET) technology. The device's analog/Radio Frequency (RF) performance are evaluated with respect to the main geometric parameters of GNSFET, such as the gate-length, the channel-width, and the channel- thickness. Key analog/RF performance metrics, including the following: I_{ON}/I_{OFF} ratio, subthreshold-swing SS, transconductance g_m, transconductance efficiency g_m/I_d, output conductance g_{ds}, gate capacitance C_{gg}, cut-off frequency F_T, and intrinsic gain A_v. Output results reveal that scaling-down T_{ch} to 6 nm, W_{ch} to 14 nm, and L_g to 16 nm enhances the I_{ON}/I_{OFF} ratio to 5.2×10^{11} and reduces SS to 60.05 mV/dec, which creates better switching efficiency. Reducing T_{ch} from 8 nm to 6 nm, and W_{ch} from 18 nm to 12 nm boosts the I_{ON}/I_{OFF} ratio by 34.48% and 33.19%, respectively, highlighting the main role of device's small geometry in improving electrostatic control. Transconductance g_m increases by 22.51% when L_g is scaled from 16 nm to 12 nm, while C_{gg} decreases with reductions in L_g, W_{ch}, and T_{ch}, aligning with graphene's inherent high carrier mobility. Notably, F_T improves by 11.71% under T_{ch} scaling, underscoring graphene's potential for high-frequency RF applications. Although, intrinsic-gain (A_v) benefits from W_{ch} and T_{ch} scaling, it exhibits a significant augmentation of 38.88% when L_g is increased from 12 nm to 16 nm, reflecting a trade-off between gain optimization and speed.**

***Index Terms*—Analog/Radio Frequency (RF), graphene, Nano-Sheet Field Effect Transistor (NSFET), performances optimization**

I. Introduction

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology faces various challenges including electrostatics, leakage current (I_{OFF}), and Short Channel Effect (SCE), related to the lacking control of the gate within the channel [1]. Therefore, researchers and micro-nano electronics companies have developed and designed various kinds of Field Effect Transistor (FET) architectures in last years, such as Double-Gate Field Effect Transistor (DGFET), Triple-Gate (TGFET), Silicon-Nanotube (SiNT) and Silicon-Nanowire (SiNW), which enhanced channel control and mitigating SCE [2]. To achieve scaling objectives and sustain Moore's Law, the shift from Fin-FET to Gate-All-Around (GAA) Nano-Sheet Field Effect Transistor (NSFET) [3]. This innovation has led to the elaboration of nanosheet FET NSFET architecture, where GAA technique is implemented into one single device. The NSFET is introduced as one of the best emerging transistor technologies for highly devices' performances, boosting drive current and compatible with Complementary Metal Oxide Semiconductor (CMOS) circuits since it provides excellent control for the gate [4]. In this architecture, multiple channels referred to as nanosheets are vertically-stacked between the drain and source region. The electrode of the gate encircles these channels on every side, creating excellent control over the body channels [5, 6]. The NSFET is a Multi-Bridge-Channel FET (MBCFET) that offers several advanced features versus classical FinFETs (fin field effect transistor), including a wider channel, greater channel width efficiency within the same footprint, good electrostatic behavior, and excellent off-current I_{OFF} [7, 8].

To identify the research gap statement in an NSFET, it is essential to conduct an in-depth review of that topic and discover the specific problems that remain unaddressed. Nonetheless, there are possible research gaps in the domain of NSFETs, such as materials optimization. NSFET is preferred to the Nanowire Field Effect Transistor (NWFET) and Nanotube field effect transistor (NTFET) by many researchers [9, 10]. NSFET is poised to continue the trend of transistor scalability. As a result, NSFET device technology is moving toward large-scale production and widespread adoption in the manufacturing of advanced semiconductor devices [11, 12].

Nanosheet architectures exhibit variable sub-threshold swing SS according to performance characteristics [13]. The best frequency responsiveness, minimal junction capacitance between the body and drain-source, and self-heating effects. Increasing the number of nanosheets

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between the source and drain increased the device's switching speed. Lastly, NSFETs are suitable for logic and memory operations due to their lower packaging density [14, 15]. Current research developments in semiconductor FET fabrication focus on shrinking, reshaping, and adding novel materials into the device's structure [16]. The usage of graphene as a novel structure NSFET was the main goal of this study. Graphene exhibits superior electrical qualities, thermal conductivity as well as increased electron mobility and saturation velocity offers high switching speeds in radio frequency analog circuits [17]. Also, this paper evaluates and optimizes the Graphene Nanosheet Field Effect Transistor (GNFET) for both Direct Current (DC) and Analog/RF (Radio Frequency) performance metrics, such as the I_{ON}/I_{OFF} ratio, SS, g_m, g_m/I_d, g_{ds}, A_v, and F_T. The effects of key device parameters are also investigated, including gate length L_g, channel width W_{ch}, and channel thickness T_{ch}, on the overall performance of the GNSFET. Additionally, this work explores the impact of graphene as a material on the electrical characteristics and performance of NSFETs, underscoring its potential to drive progress in next-generation transistor technology.

II. Background and Research Motivation

For more than 50 years, Integrated Circuits (ICs) have been enhanced by the semiconductor industry that follows Moore's law. Several studies have demonstrated that FinFETs can be downscaled to a 10-nm node [18]. But eventually, FinFET devices face a limit that prevents them from being further scaled down [19]. Future nodes will need the switch for low power applications to high efficiency purpose and faster operation [20]. The device's capacity to increase output current was investigated using a prototype NSFET via a channel length of 5 μm. Next, an NSFET was built with a gate length of 250 nm [21]. Compared to multi-FinFET, vertically stacked nanosheet FET offers superior performance because of its wider effective width [22].

Prospective research gaps in NSFETs include the absence of systematic material optimization. Despite significant advances in developing NFETs with various materials, targeted optimization still offers substantial potential [23]. Researchers may explore novel materials to enhance the efficacy of devices. We employ a graphene NSFET as an innovative structural device owing to its superior characteristics, which boost NSFET performance [24, 25].

One suitable option, the graphene FET is utilized for fast and highly dense circuits [26]. Besides being flexible to the physical nanoscale, graphene also illustrates linear current-voltage characteristics. One intrinsic drawback of a material with nothing band gap's is the extremely low ON and OFF impedance ratio [27]. A challenge for graphene FET is the gap that opens of the band gaps stated size and reliable technique compatibles with a traditional semiconductor production [28]. Despite its exceptional channel mobility, the efficacy of graphene material may be limited by elevated contact resistance near the points of contact between graphene and metal electrodes. Digital applications circuits can benefit from graphene-FETs because of their high I_{ON}/I_{OFF} ratio and near-optimal value of SS 60mV/decade [29]. Graphene FET (GFET) is a possible alternative to CMOS because of its low power consumption. Thus, GFET continues to show promise for circuits with low power [30].

This present attempt is inspired by the crucial need for more research and study on nanosheet FET, and the importance of aligning their evaluation at the device/circuit levels with the foundational technological features of this innovative 3-D structure [31, 32]. In this context, a graphene-based NSFET has been designed for the first time, targeting higher analog RF performances.

III. Device Structure and Specifications

The graphene-based NSFET structure has been established and designed using Silvaco tools. Graphene material has been implemented to create the channel layers of the NSFET device, and sandwiched between the Source (S) and Drain (D) region as a part of Silicon sheet. The FET features a metal electrode-gate which encircles the channel layer in all directions. The graphene channel layers are also encapsulated by 0.5nm of Silicon-Dioxide (SiO_2) and 1.5nm of Hafnium-Oxide (HfO_2) thickness [33], corresponding to an Equivalent-Oxide-Thickness (EOT) of 0.78 nm. Table I shows a recap of the technology parameters for the designed graphene-based NSFET.

Table I: Technology Parameters of the Elaborated Graphene-based NSFET

Parameters	Symbol	Value
Number of Nano sheet	N	2
Device Length	L	80 nm
Device Width	W	44 nm
Device Height	H	90 nm
Gate Length	L_g	12,14,16 nm
Channel Width	W_{ch}	12,14,16,18 nm
Channel Thickness	T_{ch}	6,7,8 nm
Spacing between channel layers	NSP	8 nm
Equivalent Oxide Thickness	EOT	0.78 nm
Gate Work function	ϕ_{ms}	4.95 eV
Temperature	T	300 K

IV. Simulation Methodology

The graphene substance is not available in the Silvaco tool library for simulation. Consequently, the structure of the graphene NSFET is executed by incorporating graphene as a new material. ATLAS was used to investigated the electrical properties that were connected to the given bias voltage settings. Gate to source voltage (V_{gs} = 1V), drain to source voltage (V_{ds} = 0.5 V to 1.0 V), EOT=0.78 nm and temperature (T=300) k for all simulation condition and the result of the figures. Several models, including as the (CVT) model and (SRH) model, are used in the physically based ATLAS simulator to create NSFETs [34]. The current density Auger model has been considered. These models describe how a semiconductor attempts to regain equilibrium as it is disrupted as well as how carrier mobility in the reverse layer affects the semiconductor's bulk and electronic transport [35].

Quantum effects are becoming more and more significant in nanoscale electronics. Therefore, density-

gradient drift-diffusion equations are used in the device simulations to take into consideration for the quantum restriction of carriers in the inversion layer, which is near the Si–SiO_2 interface [36, 37]. Fig. 1 illustrates the graphene-based NS-GAA FET device. The calibration and validation of the constructed device are performed using experimental data using the Silvaco Atlas tool [17, 24, 33]. NSFET can potentially be fabricated using current manufacturing methodologies, therefore connecting theoretical simulation with a real device. Major semiconductor manufacturers have declared that GAA-NSFET designs would support their 2nm and 1.8nm manufacturing nodes. Research publications by these companies show how to make working NSFET devices [7]. Experimental prototypes have demonstrated multiple advantages and innovative functionalities that graphene offers [25].

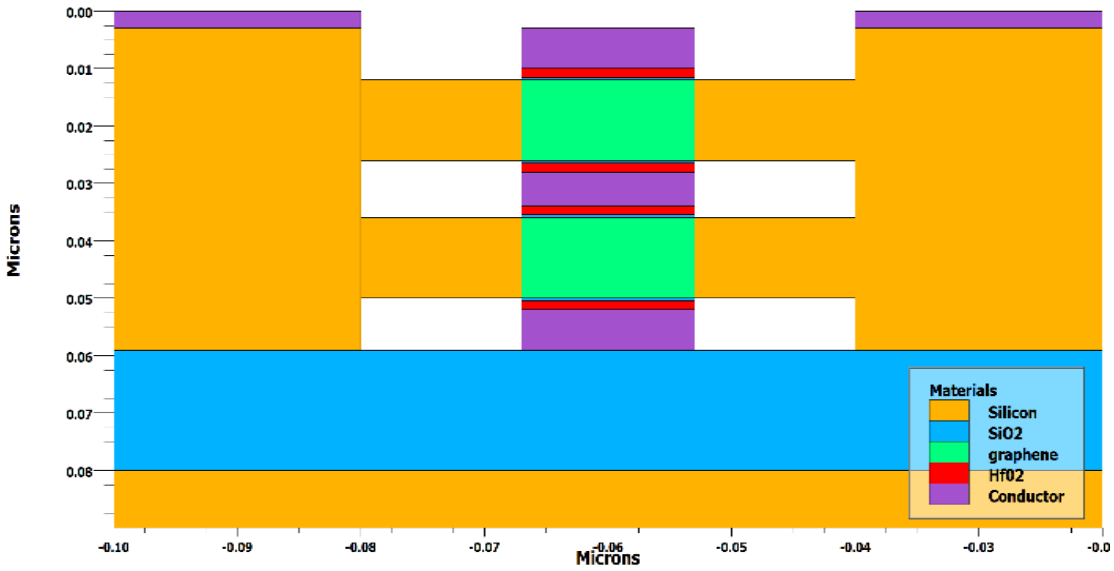

Fig. 1. Schematic view of designed GNSFET.

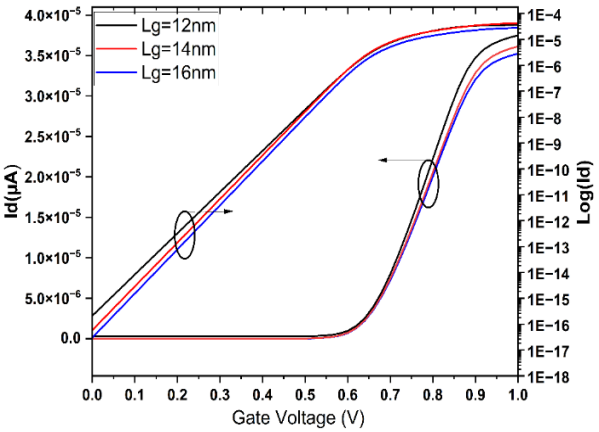

Fig. 2. I_d-V_{gs} characteristic of GNSFET for various L_g.

V. Results and Discussion

A. Impact of Gate Length (L_g) Variation

This sub-section investigates impact of the variation in gate length (12nm, 14nm and 16nm) on DC and analogue/RF parameters like I_d -V_{gs} characteristics, on-current I_{ON}, off-current I_{OFF}, I_{ON}/I_{OFF} ratio, subthreshold-swing SS, transconductance g_m, output conductance g_{ds}, gate capacitance C_{gg}, transconductance efficiency (g_m/I_d), Intrinsic gain A_v, and cutoff-frequency F_T. To explore the behaviors of the NSFET device regarding the L_g variation, the channel width W_{ch} and channel thickness T_{ch} are fixed at 14nm and 7nm consecutively. Fig. 2 shows the characteristics for the simulated NSFET.

The drain current I_d versus the gate voltage V_{gs} for different gate lengths L_g for both linear and logarithm scale is illustrated in Fig. 2. We observed that drain current I_d increased when L_g was scaled down. Transconductance efficiency g_m/I_d plays a significant part in the design of analog/RF devices, and it is defined as the attainable gain for each power consumption unit [38]. In the circuit with capacitive load, higher g_m/I_d amounts signify better input drivability and lower power consumption. Fig. 3 represents g_m/I_d with respect to $I_d/(W/L)$, an enhancement in g_m/I_d performance was observed when L_g increases.

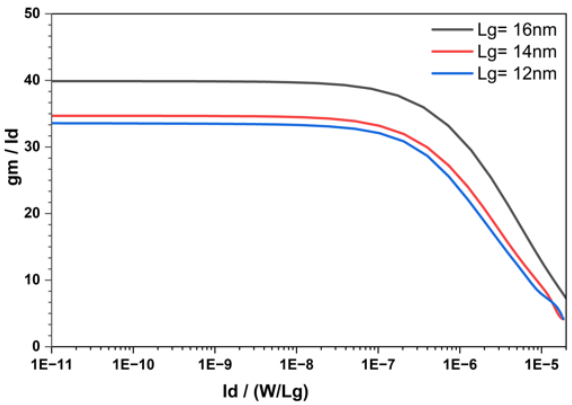

Fig. 3. g_m/I_d vs $I_d/(W/L)$ of GNSFET for various L_g.

Fig. 4 showcases on-current I_{ON} and off-current I_{OFF} with respect to L_g. Our results indicate the decrease in L_g lead to the increase in I_{OFF} and I_{ON}. The increase in I_{ON}

while the downscaling of L_g can be comprehended with the drain current (I_D) equation of NSFET which is mathematically given by [39]:

$$I_D = q\mu N_D \frac{T_{NS}\, W_{NS}}{L} V_{ds} \quad (1)$$

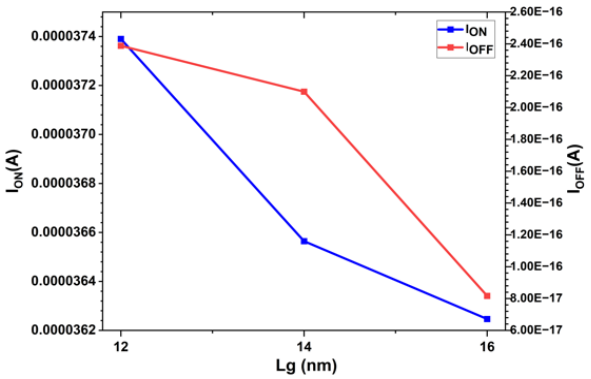

Fig. 4. I_{ON} and I_{OFF} currents of GNSFET for various L_g.

According to the equation, I_D and L_g have an inverse relationship. When L_g decreases, the I_D (I_{ON}) increases. T_{NS} and W_{NS} refer to are thickness and width of nanosheet (channel), respectively. q is the electron charge, μ is the carrier mobility and N_D is the concentration of donor.

As a result, shown in Fig. 5, an enhancement in I_{ON}/I_{OFF} ratio has obtained as L_g increases. Because of the increase in I_{OFF} current which is significantly greater than that in I_{ON} current (2.98×10^{-7} to7.97×10^{-7}) at downscaling of L_g, I_{ON}/I_{OFF} ratio of NSFET device increases as L_g increased. Nevertheless, the NSFET performs exceptionally well for all gate lengths L_g and its ratio of more than 10^7 makes it suitable for digital logic circuit applications. Subthreshold-Swing (SS) must be as low as possible due to its significant effects on the static power consumption and graphene nanosheets exhibit optimal gate coupling and superior electrostatic properties. Demonstrate exceptional (SS) at the thermionic limit (60 mV/dec) [40, 41]. It has been noted that, if L_g rises from 12 nm to 16 nm, SS goes down signifying moves in direction of the optimal level of 60 mV/dec. and then assuring improved gate control.

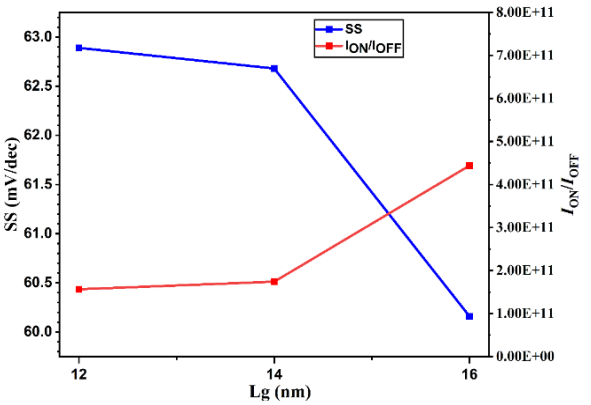

Fig. 5. SS and I_{ON}/I_{OFF} ratio of GNSFET for various L_g.

Additionally, the effect of transconductance g_m and output conductance g_{ds} for various L_g with respect to $I_d/(W/L)$ drawn in Fig. 6 and Fig. 7. It is observed that the g_m and g_{ds} are decreased linearly with a decrease in $I_d/(W/L)$ for all gate lengths L_g's. It's further found that the g_m and g_{ds} are increases with decrease in L_g. The reason for this is that as L_g decreases, the gate's electrostatic effect on the channel significantly enhances. This improved control results in a lower (SS) and a more sudden turn-on, both of which increase the peak g_m. Also, when L_g decreases, the gate's electrostatic effect on the channel near the drain becomes less, enabling the drain voltage to have a lesser impact on the current and resulting in an increase in I_d, even within saturation. This results in an increased g_{ds} and a reduced intrinsic gain. The increase in both g_m and g_{ds} with reducing L_g obtained is presented in Fig. 6 and Fig. 7 are according to Eq. (2) and Eq. (3) [33]:

$$g_m = \partial I_d / \partial V_{gs} \quad (2)$$

$$g_{ds} = \partial I_d / \partial V_{ds} \quad (3)$$

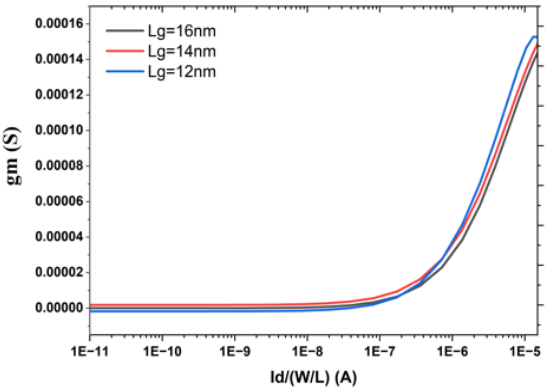

Fig. 6. Transconductance g_m of GNSFET for various L_g.

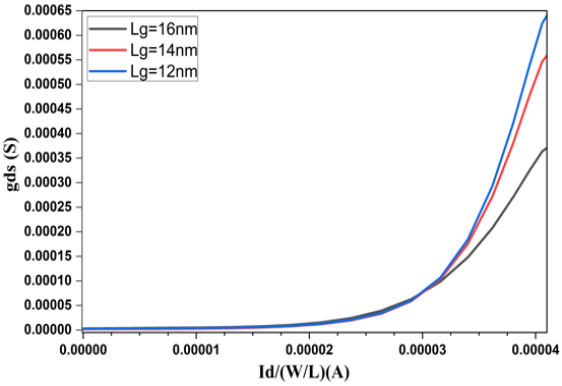

Fig. 7. Output conductance g_{ds} of GNSFET for various L_g.

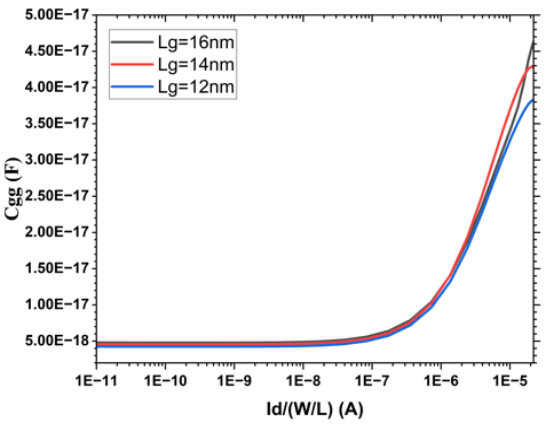

Fig. 8. Gate capacitance C_{gg} of GNSFET for various L_g.

Transconductance g_m and Output conductance g_{ds} are defined as change in drain current (I_d) to the corresponding change in V_{gs} and V_{ds} respectively. It is also observed that the gate capacitance C_{gg} in Fig. 8 decrease with the decrease in L_g because of the rise in inverted charge density and the effective channel region.

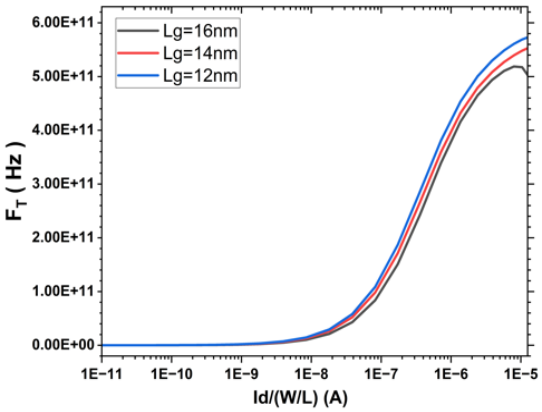

Fig. 9. Cut-off frequency F_T of GNSFET for various L_g.

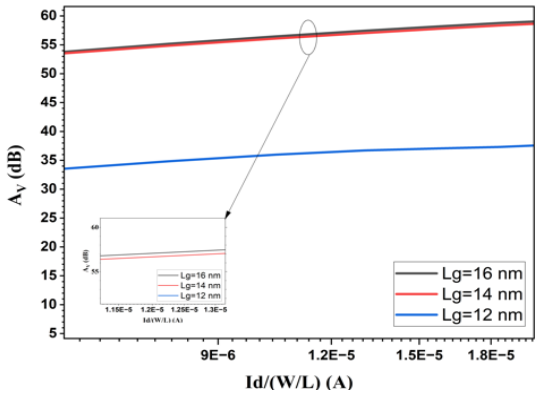

Fig. 10. Intrinsic gain A_v of GNSFET for various L_g.

Fig. 9, it is observed that the Cut-off frequency F_T increases with the decrease in L_g because of C_{gg} decrease as indicated in Eq. (4) [2]. Finally, the intrinsic gain A_v is shown in Fig. 10, decrease with a downscaling of L_g. This could be as a result of decreased g_{ds} values brought about by the increase in L_g as indicated in Eq. (5) [24].

$$F_T = \frac{g_m}{2\pi C_{gg}} \tag{4}$$

$$A_v = 20\log_{10}\frac{g_m}{g_{ds}} \tag{5}$$

By the way, gate capacitance C_{gg} is the summation of both gate source capacitance C_{gs} and gate drain capacitance C_{gd}, i.e., C_{gg}=C_{gs}+C_{gd}. F_T and A_v are significant parameters to take into account. So, according to the above equations, greater g_m values result in greater F_T and greater g_{ds} values result in lower A_v values.

B. Impact of Channel Width (W_{ch}) Variation

The channel nanosheet width W_{ch} is a key parameter that has a significant impact on devices performance. The W_{ch} is ranged from 12 mm to 18 nm using L_g and T_{ch} are set at 16 nm and 7 nm respectively. Different DC and analogue/RF parameters like I_d-V_{gs} characteristics, g_m/I_d, I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS, g_m, g_{ds}, C_{gg}, A_v, and F_T are examined to enhance the design of the graphene NSFET.

Fig. 11 showcases the $I_d - V_{gs}$ characteristics curve for different W_{ch} in both linear and logarithmic scale. It is observed the expansion of W_{ch} increases the I_d. A wider nanosheet offers an expanded cross-sectional region for higher carrier to flow, hence enhancing the total driving current. The g_m/I_d gets better with the W_{ch} scaling down as shown in Fig. 12. The I_{ON} and I_{OFF} current are decreases as the W_{ch} scaling down from 18 nm to 12 nm as shown in Fig. 13. But the decrease in I_{OFF} (1.58×10^{-11} to 8.93×10^{-11}) is significantly greater than that in I_{ON} and have an important effect on the I_{ON}/I_{OFF} ratio.

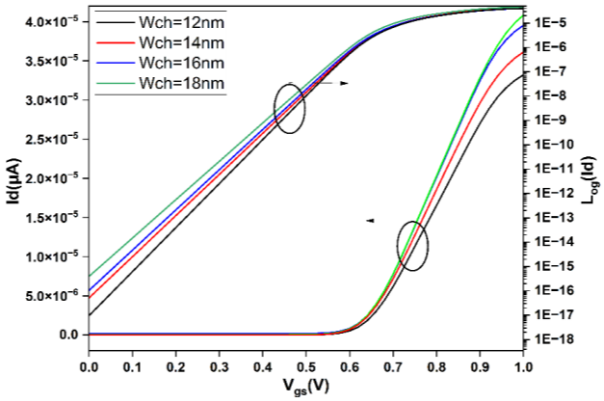

Fig. 11. I_d - V_{gs} characteristic of GNSFET for various W_{ch}.

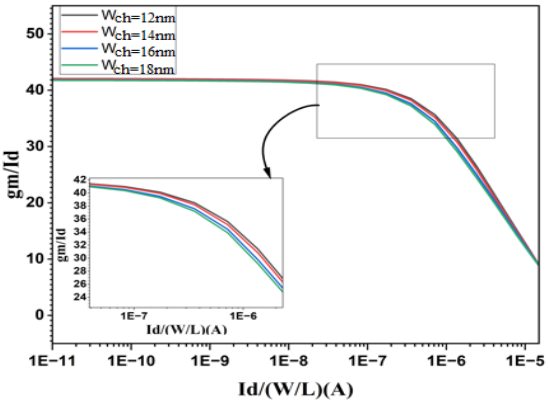

Fig. 12. g_m/I_d vs $I_d/(W/L)$ of GNSFET for various W_{ch}.

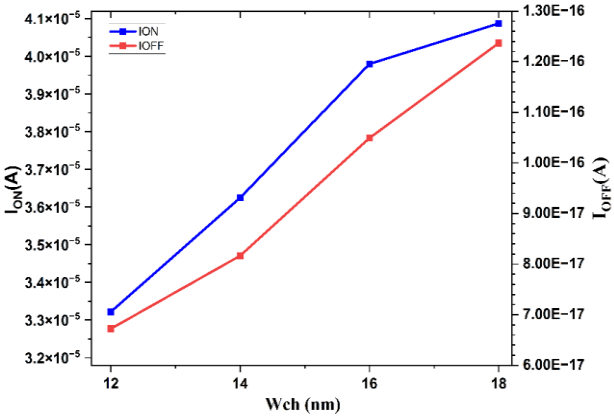

Fig. 13. I_{ON} and I_{OFF} currents of GNSFET for various W_{ch}.

The overall increase in I_{ON}/I_{OFF} ratio when W_{ch}

decreased is a result of the decrease in I_{OFF} current as plotted in Fig. 14. The SS improvement is enormous when the W_{ch} is downscaled. Additionally, this sub-section looks at the analog/RF performance with respect to $I_d/(W/L)$. Fig. 15 illustrates that when the W_{ch} is scaling up from 12 nm to 18 nm, g_m increases due to the increase in I_d directly correlates with an increased g_m according to Eq. (2) which will be reflected in the increase of the gain.

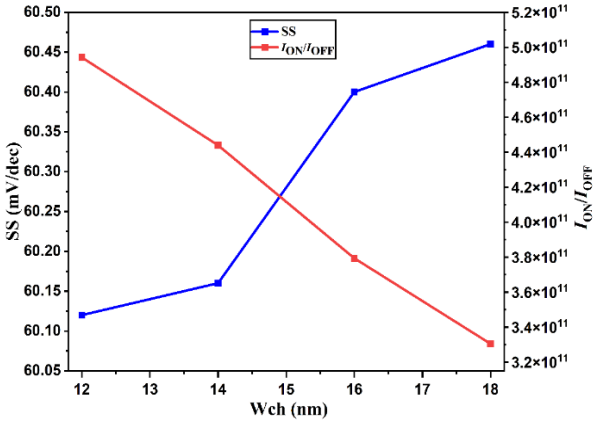

Fig. 14. SS and I_{ON}/I_{OFF} ratio of GNSFET for variation W_{ch}.

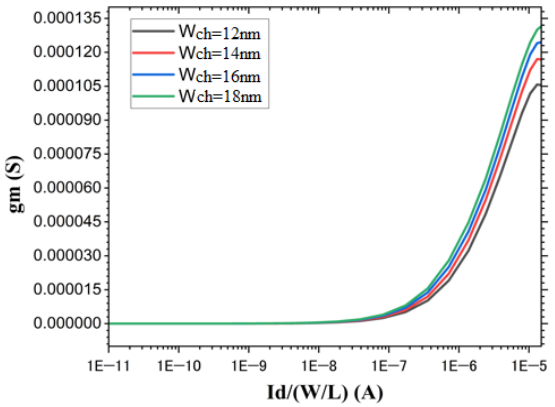

Fig. 15. Transconductance g_m of GNSFET for various W_{ch}.

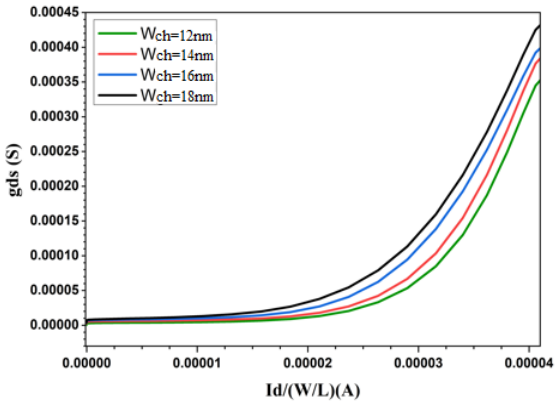

Fig. 16. Output conductance g_{ds} of GNSFET A for various W_{ch}.

The g_{ds} similarly increases effectively as W_{ch} scaling up due to the increase in I_d directly correlates with an increased g_{ds} according to Eq. (3) which will be reflected in the decrease of on-resistance (R_{on}), assuring an excellent electrical performance regarding the intrinsic gain A_v as shown in Fig. 16. Furthermore, the C_{gg} likewise increases as the W_{ch} is scaling up as illustrated in Fig. 17 which in turn enhances the F_T with the upscaling of the W_{ch} as in Fig. 18. Although both g_m and C_{gg} increase with W_{ch}, the rise in g_m is generally more dominant, leading to an overall enhancement in F_T. As a conclusion, a lower W_{ch} (=12 nm) ought to be adopted for enhanced analog/RF parameters of NSFET design. As W_{ch} is scaled down, A_v increases, leading to improved electrical efficiency, as shown in Fig. 19.

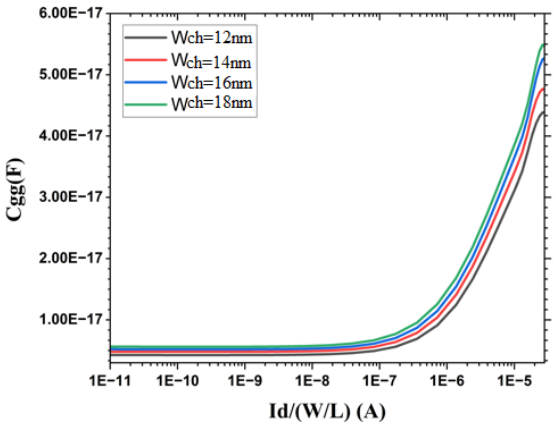

Fig. 17. Gate capacitance C_{gg} of GNSFET for various W_{ch}.

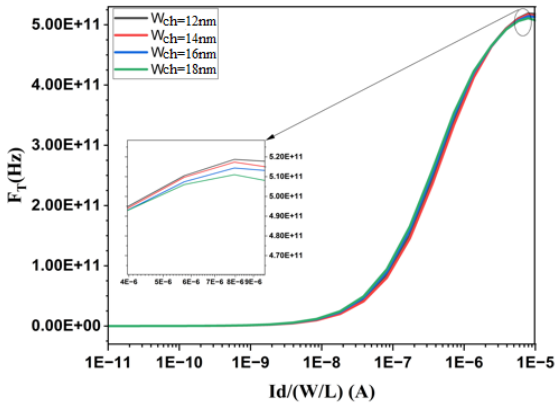

Fig. 18. Cut-off frequency F_T of GNSFET for various W_{ch}.

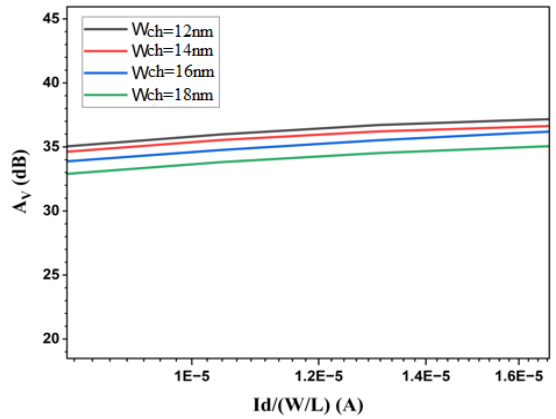

Fig. 19. Intrinsic gain (A_v) of GNSFET for various W_{ch}.

C. Impact of Channel Thickness T_{ch} Variation

The impact of channel nanosheet thickness T_{ch} on NSFET performance is examined in this sub-section. The range of T_{ch} is 6 nm to 8 nm. For the purposes of analysis,

both L_g and W_{ch} are maintained at 14 nm and 16 nm consecutively. This sub-section examines the effect of channel nanosheet thickness T_{ch} on many DC and analog parameters like I_d-V_{gs} characteristics, g_m/I_d, I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS, g_m, g_{ds}, C_{gg}, A_v, and F_T. Fig. 20 demonstrates I_d-V_{gs} characteristics for different T_{ch} in linear and logarithmic scale.

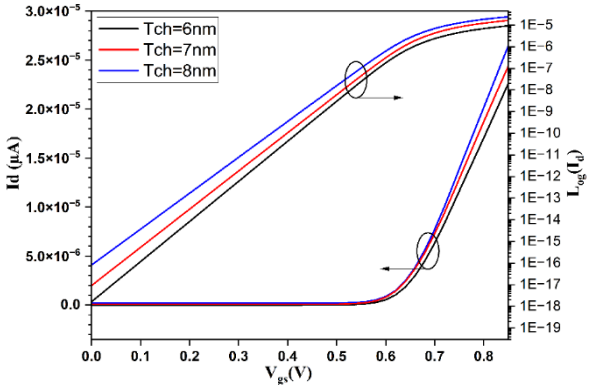

Fig. 20. I_d-V_{gs} characteristic of GNSFET for various T_{ch}.

It has been noticed that the downscaling of T_{ch} results in a decrease in I_d. Also, the g_m/I_d optimizes through the reduction of T_{ch} as illustrated in Fig. 21. It is seen that from Fig. 22, the current I_{ON} increase as the T_{ch} scaling up from 6 nm to 8 nm. Eq. (6) [42] can be used to explain why I_{ON} increase with T_{ch} scaling up. The increase in I_{OFF} current is because of the decrease in quantum-confined effects with upscaling T_{ch} as also seen in Fig. 22.

$$I_d \propto H_{NS}\left(W_{NS}/L\right) \tag{6}$$

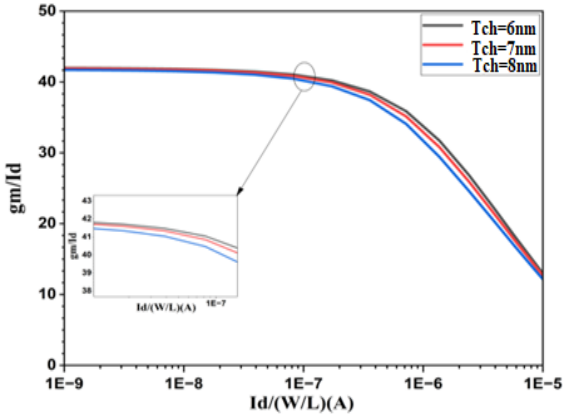

Fig. 21. g_m/I_d vs $I_d/(W/L)$ of GNSFET for various T_{ch}.

Based on the above-mentioned results, the I_{ON}/I_{OFF} ratio increase with the scaled down of the T_{ch} from 8 nm to 6 nm as showed in Fig. 23. The I_{ON}/I_{OFF} ratio increases as the reduction in I_{OFF} (6.95×10^{-10} to 3.77×10^{-12}) is significantly greater than that in I_{ON}. When T_{ch} is downscaled from 8 nm to 6 nm. Additionally, it is seen that from Fig. 23, the reducing in T_{ch} improves the SS. The analogue/RF performance regarding $I_d/(W/L)$ for various T_{ch} is analyzed in this sub-section. The scaling down of T_{ch} leads to an intriguing performance for g_m, g_{ds}, C_{gg}, F_T and A_v. Fig. 24 and Fig. 25, they demonstrate that the g_m and g_{ds} increase as the T_{ch} is upscaling. As the T_{ch} narrows significantly, quantum confinement compels charge carriers to move into higher energy states. This reduction in carrier mobility is caused by surface roughness scattering. Impaired mobility may cancel out the advantages of enhanced gate control, resulting in a reduction of g_m for extremely thin channels. The reason for the increase in g_m and g_{ds} is related to the increase in I_d as T_{ch} is scaled up, as clarified in Eq. (4) and Eq. (5).

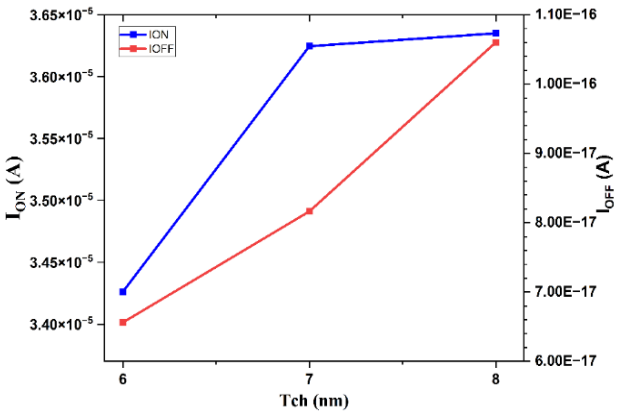

Fig. 22. I_{ON} and I_{OFF} currents of GNSFET for various T_{ch}.

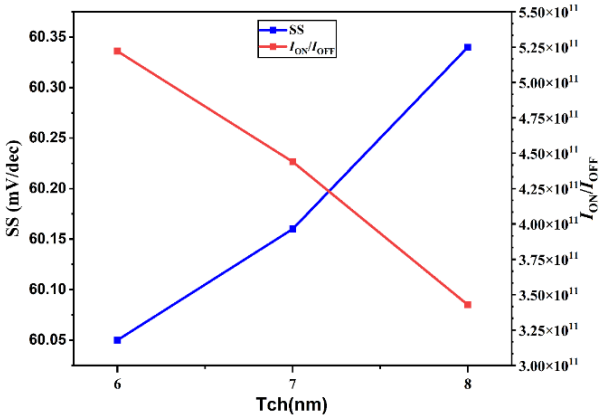

Fig. 23. SS and I_{ON}/I_{OFF} ratio of GNSFET for various T_{ch}.

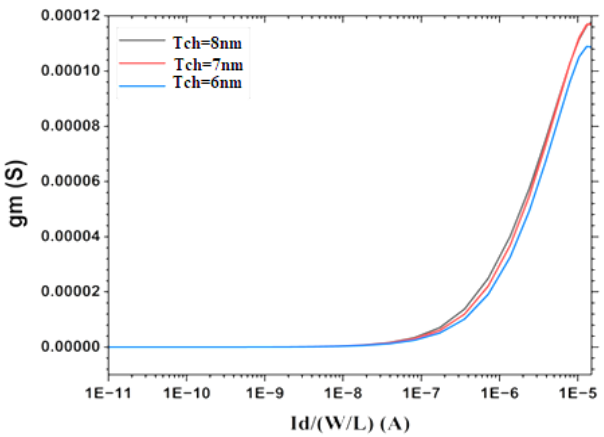

Fig. 24. Transconductance g_m of GNSFET for various T_{ch}.

Then, as seen in Fig. 26, C_{gg} have a similar behavior to enhance the performance of the NSFET device. Where C_{gg} increase with up scaling the T_{ch} from 6 nm to 8 nm. The

greater values of F_T are seen with the down scaling of T_{ch} as depicted in Fig. 27. This increases in F_T due to lower C_{gg} values with lower T_{ch}.

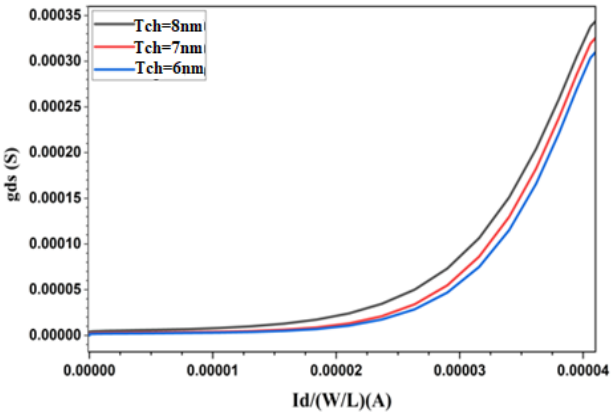

Fig. 25. Output conductance g_{ds} of GNSFET for various T_{ch}.

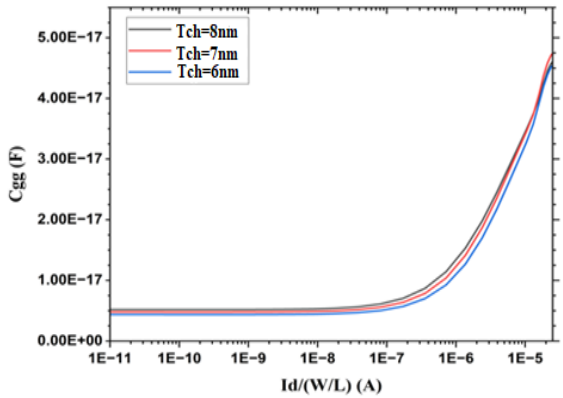

Fig. 26. Gate capacitance C_{gg} of GNSFET for various T_{ch}.

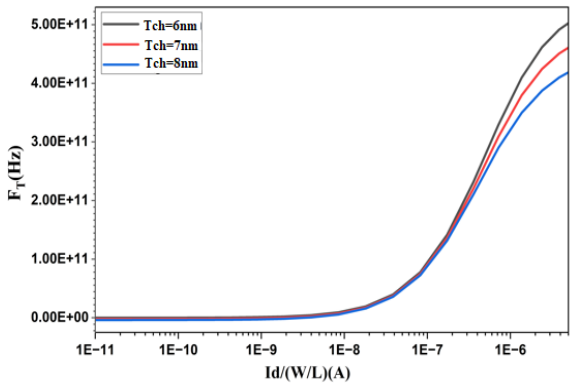

Fig. 27. Cut-off frequency F_T of GNSFET for various T_{ch}.

Finally, we noticed that the intrinsic gain A_v is decreased with up scaling T_{ch} and its lowest value when T_{ch} equal to 8 nm, as illustrated in Fig. 28. This increase (in A_v) is due to lower g_{ds} values at lower level in T_{ch}. Table II presents a recap of the essential device parameters in comparison to existing published research. Obtained results with other studies share the same parameters, including the number of sheets =2, ϕ_{ms} = (4.6–4.9) eV, EOT= 0.78 nm, and T = 300 K. Additionally, the dimensions of the devices are specified as L_g = 16 nm, W_{ch} = (10–50) nm, and T_{ch} = (5–9) nm—finally, V_{ds} = 1V.

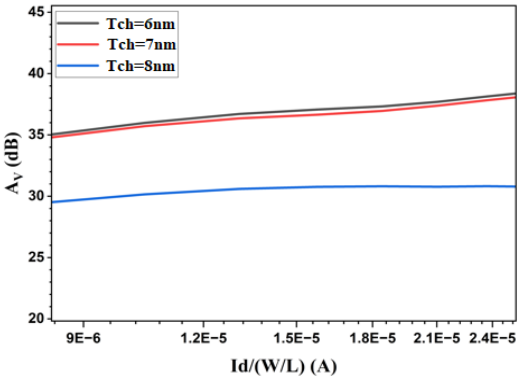

Fig. 28. Intrinsic gain A_v of GNSFET for various T_{ch}.

TABLE II: DEVICE PARAMETERS AGAINST EXISTING PUBLISHED WORKS

Ref.	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)	F_T GHz
[33]	6.8×10^{-5}	6.7×10^{-12}	$2.3\times10^{+7}$	71.0	404
[30]	2.37×10^{-5}	1.15×10^{-10}	$2.0\times10^{+5}$	70.8	3790
[37]	83.2×10^{-5}	13.3×10^{-9}	$6.3\times10^{+4}$	74.0	-
[33]	68×10^{-6}	6.7×10^{-12}	$1.01\times10^{+7}$	71	-
[33]	61.7×10^{-6}	20.6×10^{-12}	$2.99\times10^{+6}$	65.4	-
[33]	2.45×10^{-5}	1.24×10^{-14}	$1.98\times10^{+9}$	62.48	300
This work	3.42×10^{-5}	6.56×10^{-17}	$5.22\times10^{+11}$	60.05	509

VI. CONCLUSION

This article presents the design of a Graphene Nanosheet FET (GNSFET) with the goal of optimization the device' RF analog performances. The simulation studies of different DC and analog/RF parameters are performed with respect to the gate-length L_g, the channel-width W_{ch}, and the channel-thickness T_{ch} of GNSFET. The proposed GNSFET is novel and could be considered as a good candidate in analog RF application. The sub-threshold swing (SS) has been enhanced to the theoretical value (60mV/dec) and the I_{ON}/I_{OFF} ratio boost due to the significant drops in off-current I_{OFF}. Furthermore, according to the analysis, when L_g is scaled down, there are an increase in g_m, g_{ds}, F_T, decrease in gate capacitance C_{gg}, transconductance efficiency g_m/I_d, and intrinsic gain A_v. Also, there is a significant optimization in g_m and F_T. The down scaling of W_{ch} results in a significant improvement in I_{ON}/I_{OFF} ratio, A_v, F_T, and SS. Finally, the down scaling of T_{ch} increases I_{ON}/I_{OFF} ratio, g_m/I_d, A_v, and F_T. As a result, the GNSFET is a viable option for analog nanosheet-based RF applications with adequate the geometry parameters, such as L_g = 16 nm, W_{ch} = 12 nm, and T_{ch} =6 nm and RF applications when designed with L_g = 12 nm, W_{ch} = 12 nm, and T_{ch} = 6 nm.

CONFLICT OF INTEREST

The authors declare no competing interests.

AUTHOR CONTRIBUTIONS

All authors included in the research manuscript have equal contribution; all authors had approved the final version.

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