Bulk Cum QFG-Driven FVF Double Recycling Current Mirror Subthreshold OTA Based CCII+ Cell and Applications

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***Abstract*—This paper presents a low-voltage low-power second generation CCII+ cell using bulk-driven FVF class AB mode operated double recycling current mirror OTA. The OTA is used in the input core of CCII+ cell utilizes bulk-cum Quasi Floating Gate (QFG)-based voltage to current converter and Partial Positive Feedback (PPF) to enhance the performance of the circuit. The circuit permits closely rail-to-rail input common mode range, high output current drive capability with low dual power supply of ± 0.25 V. This circuit produces low input referred noise of 1.65 µV/sqrt Hz, dissipates ultra-low power of 342 nW and is suitable for low-frequency applications, such as bio-signal processing. Further, to validate this design, a MISO type voltage mode biquadratic filter and voltage mode two phase quadrature oscillator are currently being implemented using this CCII+ cells. The circuit is simulated in tanner EDA tools using 180 nm n-tub CMOS process technology with low bias current of 18 nA.**

***Index Terms*—Current Mirror (CM), Bulk-Driven (BD), Flip Voltage Follower (FVF), Quasi Floating Gate (QFG), Partial Positive Feedback (PPF), MISO Biquadratic filter**

I. Introduction

In the growing Very Large-Scale Integration (VLSI) technology, portable devices are in more demand due to Low Voltage (LV) Low Power (LP) as well as its compactness. Such compact devices are required in medical equipment, telecommunication devices and consumer electronics in the recent years. A lot of work were presented using Current Conveyor (CC) such as active grounded inductor for high frequency applications [1]. As the battery technology is not so much improved, hence circuit equipped in these devices must be compact, faster, and highly power efficient and long lasting. Due to miniature of the devices the electronic gadgets, such as laptops, cell phones, and wearable heart monitors, pace-makers are fabricated on a single chip within a very few cm^2 of the area. Physiological, bio-signals in medical field are confined to few Hz to few hundreds Hz frequency range and at most few mV in amplitude which are more prone to flicker noise and some other external noise sources. Such type of devices is used in the analog front-end circuitry of medical applications must consume ultra-low power on one hand and produce very low noise on the other hand. The circuit employing Bulk-Driven Metal Oxide Semiconductor (BD-MOS) technique is capable to provide wide input voltage range while the MOS operates in subthreshold region to obtain low-voltage low-power operation [2].

Some of the specific Complementary Metal Oxide Semiconductor (CMOS) design techniques that are used nowadays for low voltage and low power operations. The techniques are Metal Oxide Semiconductor Transistor (MOSTs) operating in subthreshold (weak inversion) region, Bulk-Driven (BD) MOST, Quasi Floating Gate (QFG), Floating Gate (FG), Flipped Voltage Follower (FVF), level shifter, self-cascode structure which provides the optimise level of performances that are needed in modern circuit design within various analog design trade-offs. The QFG technique is quite popular nowadays to enhance the transconductance of a circuit. The BD, QFG and FG are used in the circuit to reduce the requirement of power supply which decreases the power consumption of the circuit. There are various applications like Multiple Input Single Output (MISO) type voltage mode biquadratic filter and voltage mode two phase quadrature oscillator by the utilization of QFG technique. In fact, for the bulk driven topology; the threshold voltage lies out of the signal path which offers LV-LP design [3, 4]. Further, the weak-inversion or subthreshold region operation ensures ultra-low-power design and offers maximum g_m/I_D value among all the inversion types. It facilitates an energy and area efficient design of Operational Transconductance Amplifier (OTA) which is the input core of second generation positive current conveyor (CCII+) cell.

The remaining portion of the paper is organized as follows: Section II presents literature review of the related works. Section III presents second generation Current Conveyor (CCII) and quasi floating gate. Section IV illustrates double recycling current mirror OTA and quasi floating gate based CCII+ cell, Section V presents

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simulation results of the proposed CCII+ cell. Section VI presents usability of proposed CCII+ cell as voltage mode second order biquadratic filter, two phase quadrature oscillator and concerned simulation results. Finally, Section VII concludes the paper.

II. Literature Review

The second-generation Current Conveyor (CCII) is an important and very useful analog building block in the current mode approach for LV-LP applications. The circuit was based on subthreshold biased Bulk Driven (BD) MOS transistors allow the circuit designer to operate the circuit with sub 0.5 V supply and rail to rail signal swing [3].

In the past few years, several circuits were implemented based on CCII cell, a class AB CCII+ cell based on floating gate folded cascode OTA with ± 0.5 V power supply and 10 µW power dissipation was reported in [4]. A CCII based on bulk-driven folded cascode OTA with ± 0.4 V voltage supply and 64 µW power consumption was addressed in [3]. A VCII based electronically tunable multi-mode filter structure with fourth order low-pass function for the HF band applications and 0.769 µW power consumption was presented in [5]. A Novel FDNR, FDNC and lossy inductor simulators employing second generation voltage conveyor (VCII) using ±0.9 V supply and bias current of 25 µA was presented in [6]. A Current-Mode Self-Sensing Temperature Sensor Using DC-CCII for Optoelectronic Devices using ±0.75 V voltage supply and power consumption of the circuit ranges between 240 µW at a gain of 0 dB and 700 µW at a gain of 16.9 dB was reported in [7]. A new first-order universal filter consisting of two ICCII+ s and a grounded capacitor using ±0.75 V supply was presented in [8]. An improved CMOS second-generation current controlled conveyor with enhanced tunable range of R_X and its applications using supply voltage of ±1.5 V was presented [9]. A bulk driven current conveyor using 0.3 V supply and extremely ultra-low power dissipation of 19 nW was reported in [10]. A Novel carbon nanotube field effect transistor based dual output second-generation current conveyor: Design and applications using supply voltage of ±0.5 V and power consumption of 90.9 µW was reported in [11].

In the recent years, some of the circuits available in literature are based on bulk-driven, floating gate, quasi floating gate topologies to design second-generation CCII cell. The circuit reported in [12] used the supply voltage of ± 1.25 V; ensured *X* and *Z* node impedances of 2 Ω and 72 kΩ, the circuit reported in [13] used the supply voltage of ± 1.25 V; and claimed *X* and *Z* node impedances as 4.2 Ω and 92 MΩ, the circuit reported in [14] utilised supply voltage of ± 1.3 V; and provided the *X* and *Z* node impedances of 1.12 kΩ and 2.44 MΩ, the circuit reported in [15] used supply voltage of ± 0.9 V; and ensured *X* node impedance 134 Ω up to 1 MHz and *Z* node impedance 353 MΩ up to 1 MHz, and power dissipation of 47.1 µW, respectively. The VCII± cell reported in [16] used the supply voltage of ± 0.5 V; and ensured *X* node impedance and power dissipation of 16 MΩ, and 390 nW, respectively, the VCII+ cell reported in [17] utilized the supply voltage of ± 0.45 V; and ensured *X*, *Y*, *Z* node impedances and power dissipation of 156.5 kΩ, 2.7 kΩ and 38.2 Ω, and 79.3 µW, respectively. The BD-SC (Bulk-driven self cascode) CCII cell reported in [18] used the supply voltage of ± 0.25 V; and ensured *X*, *Y*, *Z* node impedances and power dissipation of 3.1 kΩ, 103.75 MΩ, 14 MΩ and 504 nW, respectively, the BD-CII cell reported in [19] utilized the supply voltage of 0.3 V; and ensured *X*, *Y*, *Z* node impedances and power dissipation of 52 kΩ, 734 MΩ, 112 MΩ, and 37 nW, respectively.

The advantage of Bulk-Driven Current Conveyors (BD-CCs) over other traditional Gate Driven Current Conveyors (GD-CCs) are that former can operate on low voltage power supply as well as dissipates extremely low power. The BD-CC cells are used in various fields like biomedical or bioelectronics circuits, Internet of Things (IOTs), smart phones which utilizes LV-LP and need to process low frequency confined very weak amplitude signals. Most of the wave shaping techniques such as Sine wave, Square/Triangular waveform generators are used in instrumentation, communication systems and signal processing applications. The CCIIs are also used to design Voltage Mode (VM) and Current Mode (CM) Single Input and Multiple Output (SIMO), Multiple Input and Single Output (MISO) type second order biquadratic filter, oscillators, Half-Wave (HW) and Full-Wave (FW) rectifiers, Instrumentation Amplifiers (IA), Proportional-Integral-Derivative (PID) controllers, integrators [20, 21].

III. Second Generation Current Conveyor

The second-generation current conveyor is a three-terminal device, the two input terminals *X* and *Y* and one output terminal *Z* as shown in Fig. 1. The *Y* terminal is high impedance voltage input terminal whereas *X* terminal offers very low input impedance. There is voltage buffering action between terminal *X* and *Y* and current buffering action between *X* and *Z* terminals. Hence the voltage of *X* and *Y* terminals are closely equal and current at *X* terminal is conveyed to the *Z* terminal. The impedance at *X* terminal is ideally zero, impedance at *Y* terminal is infinite while impedance at *Z* terminal is very high, also current flowing at *Y* terminal is zero due to high impedance. The voltage of *X* terminal is fixed by voltage on *Y* terminal and *X* terminal voltage is independent of the current set through *X* node [22, 23].

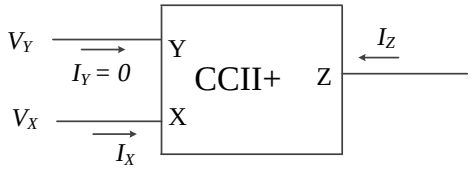

Fig. 1. Block diagram of CCII+ cell.

The second-generation current conveyor operational matrix is given in (1):

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

When the direction of currents from *X* node and *Z* node entering toward CCII cell, then the circuit is called as

positive CCII cell (CCII+) and the direction of currents from *X* node is entering and direction of current from *Z* node is leaving, then the circuit is called as negative CCII cell (CCII−). Equation (2) and (3) relates the voltage and current between input and output terminal for CCII+ and CCII− cells.

$$V_Y = V_X, I_X = I_Z, I_Y = 0 \text{ (for CCII + cell)} \quad (2)$$

$$V_Y = V_X, I_X = -I_Z, I_Y = 0 \text{ (for CCII − cell)} \quad (3)$$

The voltage gain is represented by, $\alpha = V_X/V_Y$ and current gain is $\beta = I_Z / I_X$. The ideal value of α and β are unity.

A. Quasi Floating Gate

The capacitively coupled *N*-input quasi-floating gate (QFG) transistor is shown in Fig. 2 for the pMOS device.

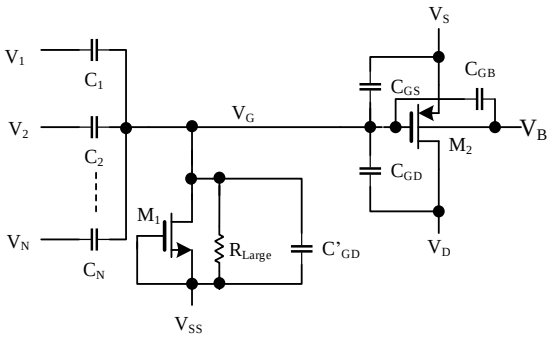

Fig. 2. QFG pMOS transistor equivalent circuit [24].

The floating gate (FG) MOS transistor is also a low-voltage design method; however, it has shortcoming of charge accumulation and DC bias saturation effects for amplifiers. The floating gate transistor voltage are very much close to V_{DD} supply rail when using nMOS transistor and V_{SS} supply rail while using pMOS transistor, when there are multiple inputs at floating gate. This problem voltage (charge) trap and DC biasing shift is not present in QFG based amplifiers. This difficulty is rectified by using a large, valued resistor connected across the gate terminal and one of the power supply rails. One large, valued resistor R_{Large} is connected for both pMOS and nMOS input devices to set their gate voltage either to V_{SS} or to V_{DD} level, respectively.

The R_{Large} resistor which has non-linear characteristic, is generally a MOS resistor made of source to gate shorted nMOS transistor offers large resistance of reverse biased p-n junction and operates in cut-off region (see Fig. 2) [24].

Using the s-domain analysis, the ac voltage; V_G at the quasi-floating gate is given by [24]

$$V_G = \frac{sR_{\text{Large,PD}}}{1 + sR_{\text{Large,PD}}C_T} \times \left(\sum_{k=1}^{N} C_k V_k + C_{\text{GS}}V_S + C_{\text{GD}}V_D + C_{\text{GB}}V_B\right) \quad (4)$$

where C_k is the coupling capacitance of the *k*th input branch and C_{GS}, C_{GD} and C_{GB} are gate to source, gate to drain and gate to bulk capacitances of the quasi-floating gate, respectively.

The total capacitance C_T is given by

$$C_T = \sum_{k=1}^{N} C_k + C_{GS} + C_{GD} + C_{GB} + C'_{\text{CD}} \quad (5)$$

where C'_{CD} is the gate to drain resistance of large, valued resistor made with nMOS transistor connected at gate terminal of quasi-floating gate [24].

Equation (4) reveals that it has high pass (HP) filter response in which frequency can be made very low using the cut-off frequency $1/(2\pi R_{\text{Large,PD}}C_T)$.

When the ac voltage given by (4) is superimposed on dc voltage made equal to the negative rail by large resistor R_{Large}, then the gate voltage can be made lower than V_{SS}. Hence, the problem is rectified if the gate voltage cannot exceed the cut-in voltage of nMOS transistor which is made of p-n body source junction while implementation of R_{Large} and junction never becomes forward-biased [24–26].

IV. Proposed BD-DRCM-QFG OTA Based CCII+ Cell

Fig. 3 shows the CCII+ cell using CMOS inverter approach. The block diagram shows one OTA cell and two identical CMOS inverters. The aspect ratios of pMOS and nMOS transistors forming inverters are set to have equal current driving capabilities to cope with differences in mobilities of holes and electrons. If 100% negative feedback is applied from the output of inverter 1 to the inverting terminal of OTA cell, then it becomes *X* terminal of CCII+ cell. Due to this negative feedback, it severely reduces the impedance of *X* terminal while other terminal of OTA does not offer any such negative feedback, called as *Y* terminal of CCII+ cell, hence impedance of *Y* terminal becomes very high; ideally infinite. The output of inverter 2 is *Z* terminal of CCII+ cell and offers very high impedance. The *Z* node is neither connected to the output of an inverter nor to the output of the OTA directly, however; it is connected to the output of an OTA through the compensation capacitor (C_{C2}). The *Z* node current, I_Z when flows either through parasitic capacitance at *Z* node or through resistive load connected there or combination of both; it generates a voltage at *Z* node. Two compensation capacitors C_{C1}, C_{C2} of equal values are used between input and output of both the CMOS inverters to set better phase margin.

N. Deo, *et al.* were reported a performance enhanced low-voltage low-power subthreshold region operated bulk-driven double recycling current mirror OTA in 2020 [27]. Like this CCII+ cell utilizes a low-voltage low-power subthreshold region operated bulk cum quasi-floating gate driven double recycling current mirror OTA (BD-DRCM-QFG OTA) in its input core. Fig. 4 shows the circuit schematic of proposed CCII+ cell based on BD-DRCM-QFG OTA.

The input core of the proposed CCII+ cell is a BD-DRCM-QFG OTA (See OTA section of Fig. 4). The differential input transistors of conventional bulk-driven current mirror OTA are splits into three parts (M_{1A}, M_{1B}, M_{1C}) and (M_{2A}, M_{2B}, M_{2C}) in the left and right halves, respectively. The bulk terminals of each of the transistors in left half are tied together and presents one input terminal, which is termed as the *Y* terminal of CCII+ cell. The *Y*

terminal has very high impedance, ideally infinite as this terminal is of capacitive type. The bulk terminal of each of the transistors in right half are tied together and form the *X* terminal of the CCII+ cell, as 100% negative feedback is provided from the output of CMOS inverter 1 consisting of transistors M_{17} and M_{19} which severely reduces the impedance of *X* terminal (Explained in Fig. 3). There are three current mirrors below the drain terminals of input transistors in left and right halves consisting of the transistors (M_3, M_5), (M_7, M_9), (M_{11}, M_{13}) and (M_4, M_6), (M_8, M_{10}), (M_{12}, M_{14}), respectively.

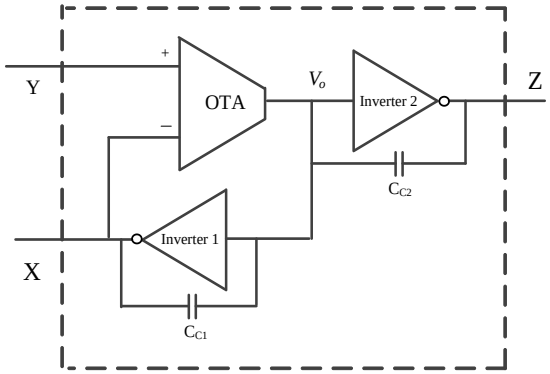

Fig. 3. Block diagram of CMOS CCII+ cell [20].

The current mirror ratios are *P*, *Q*, *R*, *S*, *T* and *U* as 2, 3, 1, 3, 1 and 6, respectively for the simulation. The drain terminal current of the transistor M_{1B} is conveyed to drain of M_6 and M_8 from left half input terminal to the right half current mirror which sets recycling structure. Similarly, the drain terminal current of the transistor M_{2B} is conveyed to drain of M_5 and M_7 from right half input terminal to the left half current mirror which also sets recycling structure. Due to current mirrors and appearance of the signal in either side, it forms the double recycling structure in the OTA section.

The source terminals of input transistors in left and right halves are connected to the drain of M_{P1} and M_{P2} which are comprised of two flipped voltage followers (FVFs) consisting of the transistors (M_{P1}, M_{P3}, M_{N3}) and (M_{P2}, M_{P4}, M_{N4}) which increases the current driving capability and favours LV-LP applications. The circuit utilizes the QFG structure (See Fig. 4 in blue box) in both two FVFs as well as the two input cores of recycling parts. The transistor pair (M_{P3}, M_{P4}) forms FVF pair and transistors (M_{N5}, M_{N6}) presents a very large MOS resistance required for the operation of the QFG. Similarly, in double recycling core structure; the transistors M_{N7} and M_{N8} presents a very large MOS resistance required for the operation of the QFG. The gate and source of M_{N5}, M_{N6}, M_{N7} and M_{N8} are shorted together to act as MOS resistor. The input signal is directly fed to bulk terminals of FVF transistors as well as bulks terminals of double recycling input pairs, whereas this input signal is capacitively coupled to the gate terminals of FVF transistors as well as gate terminals of double recycling input pairs. The use of FVFs and QFG enhances the transconductance of internal OTA circuit as the transconductance values for the conventional gate driven for QFG, FG and BD MOSTs are in descending order of $g_m > g_{m,\mathrm{QFG}} > g_{m,\mathrm{FG}} > g_{\mathrm{mb}}$ [26]. Further, to improve the performance of the circuit; PPF is utilized comprising of the transistors M_{N1} and M_{N2} which further enhances the transconductance of the circuit.

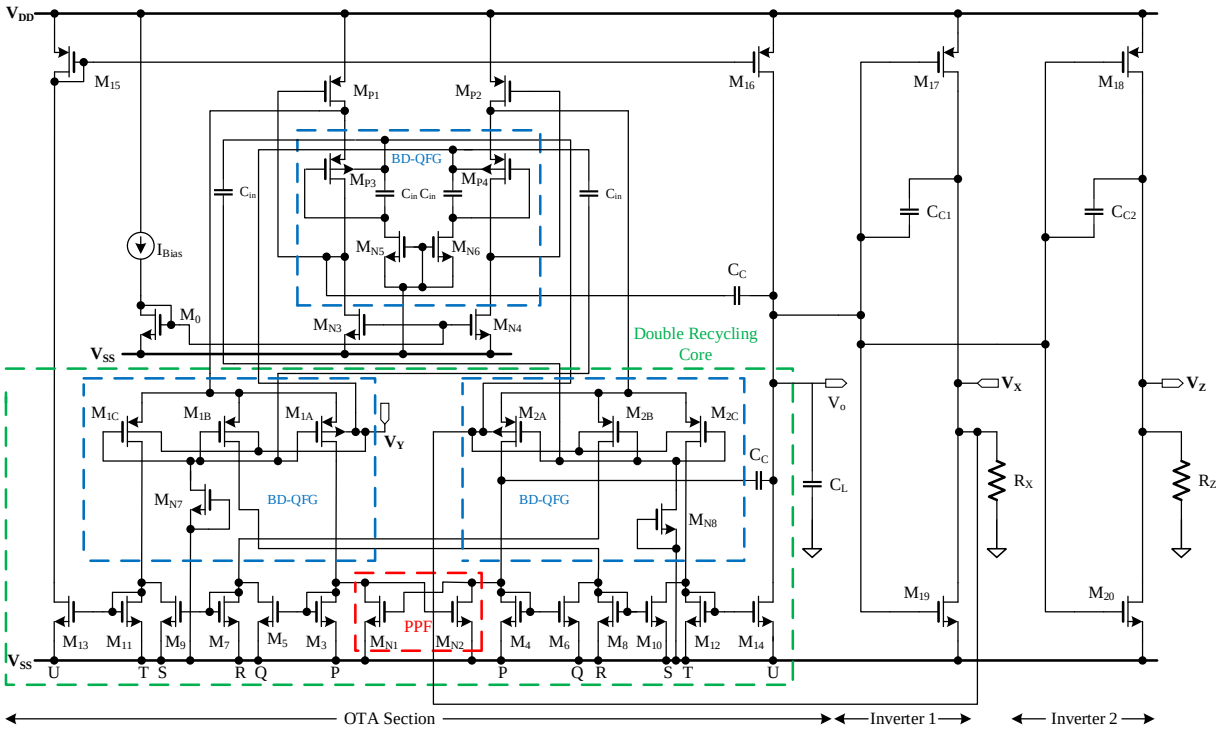

Fig. 4. Proposed BD-DRCM-QFG OTA based CCII+ cell.

Now, two-CMOS inverters are connected at the output of the OTA circuit to realize the CCII+ cell. The output of CMOS inverter 1 act as a *X* terminal as stated earlier and the output of CMOS inverter 2 which is comprised of

transistors (M_{18}, M_{20}) act as a *Z* terminal of the CCII+ cell. As there is no feedback provided to the *Z* terminal, the *Z* impedance is very high.

V. Simulation Results

The proposed CCII+ cell is simulated using 180 nm n-tub CMOS process technology and utilizing dual power supply of ±0.25 V with the bias current (I_{Bias}) of 18 nA at room temperature, i.e., at 27ºC. The common mode voltage (V_{CM}) is equal to zero for dual power supply-based design. The proposed CCII+ cell utilizes two compensation capacitors ($C_{C1} = C_{C2} = 0.2$ pF) of equal values between input and output of two-CMOS inverters that are connected at the output of BD-DRCM-QFG OTA. The circuit also uses two equal value of load resistors ($R_X = R_Y = 10$ kΩ) at *X* and *Z* terminals. The aspect ratios of the CMOS devices used for the design of the proposed CCII+ cell is shown in Table I.

A. AC Analysis

The voltage buffering between *X* and *Y* nodes and current buffering between *Z* and *X* nodes expect unity gain plot for *Y* and *X* nodes as well as for *X* and *Z* nodes. When V_{ac} signal is applied at the *Y* terminal of the proposed CCII+ cell, and output response is considered at both the *X* and *Z* nodes individually, then gain response of 0 dB is expected up to certain frequency of interest. The load resistances at *X* node, say R_X and *Z* node, say R_Z are set to 10 kΩ in this AC simulation set up. The 3-dB frequency of the *Y*-*X* follower was reported in [10] and is shown in (6)

$$f_{3dB} \approx \frac{g_{m_{M\,1A}} \| g_{m_{M\,1B}} \| g_{m_{M\,1C}} \| g_{m_{M\,P4}}}{2\pi C} \tag{6}$$

where *C* is the capacitor at the output of the OTA circuit.

TABLE I: Dimensions of the Components Used in Proposed CCII+ Cell

Device	*W*/*L* (µm/µm)	Device	*W*/*L* (µm/µm)
M_{1A}, M_{2A}	5.22/0.54	M_{P3}, M_{P4}	10/0.5
M_{1B}, M_{2B}, M_{1C}, M_{2C}	6.48/0.54	M_{N5}, M_{N6}, M_{N7}, M_{N8}	60/1, *M*=2
M_3, M_4	2.16/1.08	M_{17}, M_{18}	50/0.18, *M*=2
M_5, M_6, M_9, M_{10}	3.24/1.08	M_{19}, M_{20}	40/0.18
M_7, M_8, M_{11}, M_{12}	1.08/1.08	$C_C = C_{C1} = C_{C2}$	0.2 pF
M_{13}, M_{14}	6.48/1.08	C_{in}	0.05 pF
M_{15}, M_{16}	9.72/0.54	C_L	15 pF
M_{N1}, M_{N2}	1.7/1.08	R_X	10 kΩ
M_0, M_{N3}, M_{N4}	2/1	R_Z	10 kΩ
M_{P1}, M_{P2}	50/1	I_{Bias}	18 nA

Fig. 5 shows the ac analysis result when ac signal is applied at the *Y* terminal.

This figure depicts the −3dB bandwidth of 7.4 kHz with C_L of 15 pF for both of *X* and *Z* nodes as output terminal nodes. The power dissipation of proposed CCII+ cell is 342 nW.

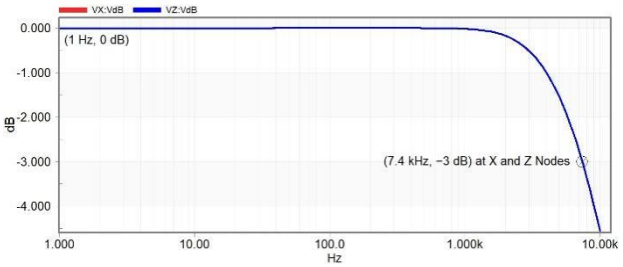

Fig. 5. –3 dB bandwidth under AC response.

B. Voltage and Current Gain

There is very good voltage buffering action between *Y* and *X* nodes, which means *X* node voltage follows the *Y* node voltage. So, if V_{ac} input signal is applied at *Y* input terminal and output is determined for *X* node; unity gain is expected. Similarly, there lies very good current buffering action between *X* and *Z* nodes. So, output *Z* node current follows the input *X* node current.

Applying the routine analysis for this CCII+ cell, the voltage gain (α) is expressed in (7)

$$\alpha = \frac{V_X}{V_Y} = \frac{\left(g_{m_{M17}} + g_{m_{M19}}\right)\left(R_{0_{M17}} \| R_{0_{M19}}\right) A_v}{\left\{1 + \left(g_{m_{M17}} + g_{m_{M19}}\right)\left(R_{0_{M17}} \| R_{0_{M19}}\right) A_v\right\}} \tag{7}$$

The current gain (β) is obtained by (8)

$$\beta = \frac{I_Z}{I_X} \cong \frac{g_{m_{M20}} + g_{m_{M18}}}{g_{m_{M19}} + g_{m_{M17}}} \tag{8}$$

where $R_{0_{M17(19)}}$ are the output impedances of $M_{17(19)}$, $g_{m_{M17(19)}}$ and $g_{m_{M18(20)}}$ are the transconductances of $M_{17(19)}$ and $M_{18(20)}$, respectively and the open loop gain of BD-DRCM-QFG OTA is A_v [28].

Fig. 6 and 7 shows the voltage gain and current gain of the proposed CCII+ cell respectively.

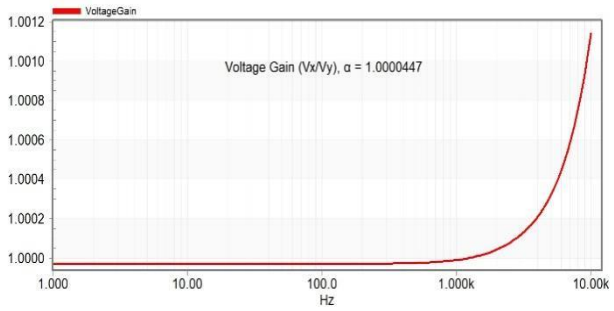

Fig. 6. Voltage gain response.

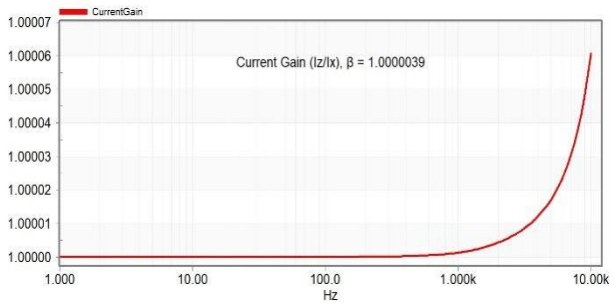

Fig. 7. Current gain response.

The mean of voltage gain (α) and current gain (β) (for 1 Hz to 10 kHz range) are found to be 1.0000447 and 1.0000039, respectively. If the circuit is physically implemented then a various design tolerances like device corner effect comes into picture which may shift the α and β values to some extent.

C. Impedances at Different Nodes

The parasitic impedances at *X*, *Y* and *Z* node are obtained by applying a test signal at concerned node and determining the current drawn by this test signal. The ratio of test voltage and current sets the node impedance. The resistive and inductive behaviour are observed by node *X* which is the input current signal, at lower and higher frequencies, respectively. The impedance at *X* node is very low, ideally zero because negative feedback is applied on this terminal. The *Y* node impedance is ideally infinite and practically very high because of SiO_2 layer at gate/bulk terminals. Since *Y* node does not receives any such negative feedback, hence impedance of *Y* node is very high. The *Y* impedance is capacitive type that depends on the input transistors aspect ratios. The very high input impedance at *Y* node avoids loading effect for voltage mode inputs. The *Z* node impedance is high as no feedback is applied on this terminal [29].

The impedances at node *X*, *Y* and *Z* are obtained by (9), (10) and (11), respectively.

$$R_X = \frac{V_X}{I_X} = \frac{\left(R_{0_{\mathrm{M17}}} \| R_{0_{\mathrm{M19}}}\right)}{\left\{1+\left(g_{m_{\mathrm{M17}}}+g_{m_{\mathrm{M19}}}\right)\left(R_{0_{\mathrm{M17}}} \| R_{0_{\mathrm{M19}}}\right)A_v\right\}} \quad (9)$$

$$R_Y = \frac{1}{2\pi f C_Y} \quad (10)$$

where C_Y is the total capacitance at *Y* node.

$$R_Z = R_{0_{\mathrm{M18}}} \| R_{0_{\mathrm{M20}}} \quad (11)$$

According to (9), R_X tends to be very small due to high value of closed loop gain $\left\{1 + \left(g_{m_{\mathrm{M17}}} + g_{m_{\mathrm{M19}}}\right)\left(R_{0_{\mathrm{M17}}} \| R_{0_{\mathrm{M19}}}\right)A_v\right\}$. R_Y is very large as *Y* node is input terminal and output impedance at *Z* node is large if the output resistor of CMOS inverter 2 comprising of transistors M_{18} and M_{20} is large [28].

The impedances at *X*, *Z* and *Y* nodes are found to be 10.2 kΩ, 1.7 MΩ and 1.9 TΩ and listed in Table II.

D. Noise Analysis

The noise is the unwanted and unpredictable signal that occurs in the circuits, devices or the networks due to voltage and current variations along with the original signal received at the output. The noise occurs mainly due to internal or external inferences in the signal. The external interferences are due to variations in the supply voltage, wires or electromagnetic waves coming from external sources that can be reduced by proper wiring and layout. The internal noises are thermal, shot and flicker due to physical fluctuations to the devices which can be reduced by proper design of transistor sizes.

The total input thermal and flicker noise power spectral density (PSD) in weak inversion operation at gate-terminal $\bar{V}_{\mathrm{sn}}^2$ are expressed as

$$\bar{V}_{\mathrm{sn}}^2 = \bar{V}_{\mathrm{sn,th}}^2 + \bar{V}_{\mathrm{sn},(1/f)}^2 = \frac{2q_i d_i}{g_m^2} + \frac{1}{g_m^2}\frac{K'_{\mathrm{FP}} g_{\mathrm{mi}}^2}{(W/L)_i f} \quad (12)$$

The total input thermal and flicker noise power spectral density in weak inversion operation at bulk-terminal $\bar{V}_{\mathrm{snB}}^2$ are expressed as:

$$\bar{V}_{\mathrm{snB}}^2 = \bar{V}_{\mathrm{snB,th}}^2 + \bar{V}_{\mathrm{snB},(1/f)}^2 = \frac{2q_i d_i}{g_{\mathrm{mbi}}^2} + \frac{1}{g_{\mathrm{mbi}}^2}\frac{K'_{FP} g_{mi}^2}{(W/L)_i f} \quad (13)$$

where g_m and g_{mbi} are the gate and bulk-transconductances of the input pair. In 180 nm CMOS process n = 4/3 and (n−1) is 1/3, so $g_m = 3g_{\mathrm{mb}}$, and $g_m^2 = 9g_{\mathrm{mb}}$. Thus, input referred noise at bulk terminal is 9 times greater than the gate terminal.

If V_{ac} input is applied at *Y* terminal, the output noise may be observed at *X* and *Z* nodes of CCII+ cell. The output noise associated at *X* and *Z* nodes when referred to input terminal is called input referred noise which is found to be 1.65 μV/sqrt Hz (same for both *X* and *Z* nodes) at 1 kHz frequency. Fig. 8 shows simulated input referred noise for this CCII+ cell.

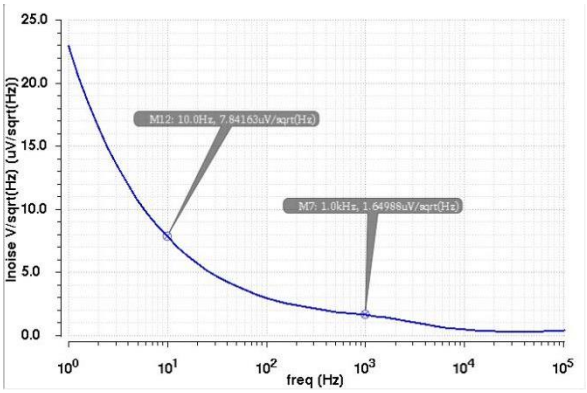

Fig. 8. Input referred noise.

E. Response under Unity Gain Configuration

In CCII+ structure, there lies 100 % negative feedback between *X* terminal and one terminal of input pair which offers voltage buffering action between *Y* and *X* nodes. This CCII+ cell is utilized OTA cum two CMOS inverters-based design topologies, so voltage buffering is expected for both of *X* and *Z* nodes w.r.t. *Y* terminal. Fig. 9 shows the DC sweep response in which *X* and *Z* node voltages closely follow the *Y* node voltage showing very good linearity between input and output terminals. It is ensured that the input common-mode range (ICMR) of −230 mV to +230 mV. The errors (deviation) at −200 mV and +200 mV of input voltage levels are found to be 594.2 μV and −18.9 μV, respectively. The DC offset error, when no signal is applied at *Y* input node (V_{in} = 0 mV) are found to be −1 μV associated with both *X* and *Z* as output nodes.

The slew rate (SR) determines the processing speed and is simulated in pulse transient mode of simulation set up.

The input pulse of 230 mV amplitude and 1 kHz frequency is applied at *Y* node and output pulse is produced at *X* and *Z* nodes. It is found that the average slew rate of the circuit to be 34 V/ms for the loads $R_X = R_Z = 100$ kΩ.

Fig. 10 shows the total harmonic distortion (THD) when sinusoidal input is applied at *Y* terminal and output responses are considered at *X* and *Z* nodes. The THD is found to be −43 dB at *X* and *Z* nodes, when input of 250 Hz frequency with 230 mV (peak) amplitude is applied.

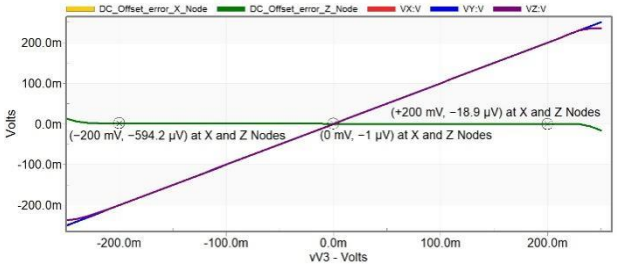

Fig. 9. DC sweep analysis.

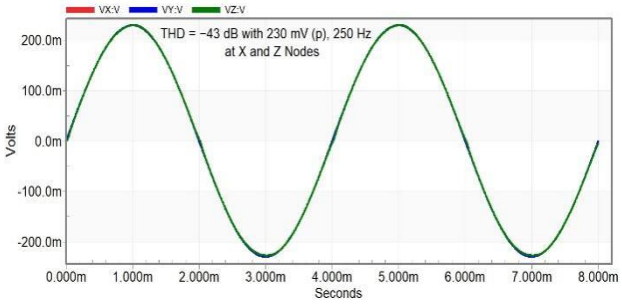

Fig. 10. Input and Output response for THD.

F. Layout and Figure of Merit of Proposed CCII+ cell

Fig. 11 shows the layout of the proposed CCII+ cell, that occupies the chip area of 112 µm × 54.4 µm, i.e., 6092.8 µm^2. The Table II shows the comparison of pre-layout and post layout simulation of the proposed CCII+ cell, it shows very high degree of closeness between pre-layout and post layout results which validates the usability of this CCII+ cell under various layout to post-layout mismatches occurring due to several process variations.

For accounting the performance of the circuit, Figure of Merit (FOM) is introduced which correlates the quantities BW which is directly proportional and PD which is inversely proportional to the FOM and is defined by (14):

$$\text{FOM} = \frac{\text{BW}\frac{\text{DR}}{\text{PS}}}{\text{PD}} \tag{14}$$

where BW is the bandwidth of the current gain, DR is the dynamic input range, PS is the total power supply, and PD is the power dissipation [28].

The novelty of the proposed circuit is that when applying the techniques of FVF, PPF, QFG and double recycling structure in conventional current mirror OTA; the transconductance of internal OTA circuit is increased, as the transconductance values are in descending order of $g_m > g_{m,\text{QFG}} > g_{m,\text{FG}} > g_{\text{mb}}$ [26]. This enhances the performances of CCII+ cell such as the power dissipation is in ultra-low power range among all references were used in comparison Table II except [19]. The −3 dB bandwidth is quite low except [19] which is suitable for low frequency biomedical applications. The *X* node impedance is low except [18]. The ICMR is in wide range from −230 mV to +230 mV and DC offset error is extremely low, which indicates the linearity of the circuit is quite better among all the references were used except [9] in the comparison Table II. The average slew rate, that determines the processing speed of the circuit is high as compared to all references were used in the comparison Table II. The THD of the designed circuit is better than the references were used in the comparison Table II, as minimum THD should be less than 1% or −40 dB for the system to be stable and another parameter to check the linearity of the circuit. Another advantage of the designed circuit is that it occupies minimum possible chip area as compared to the references were used in the comparison Table II except [17].

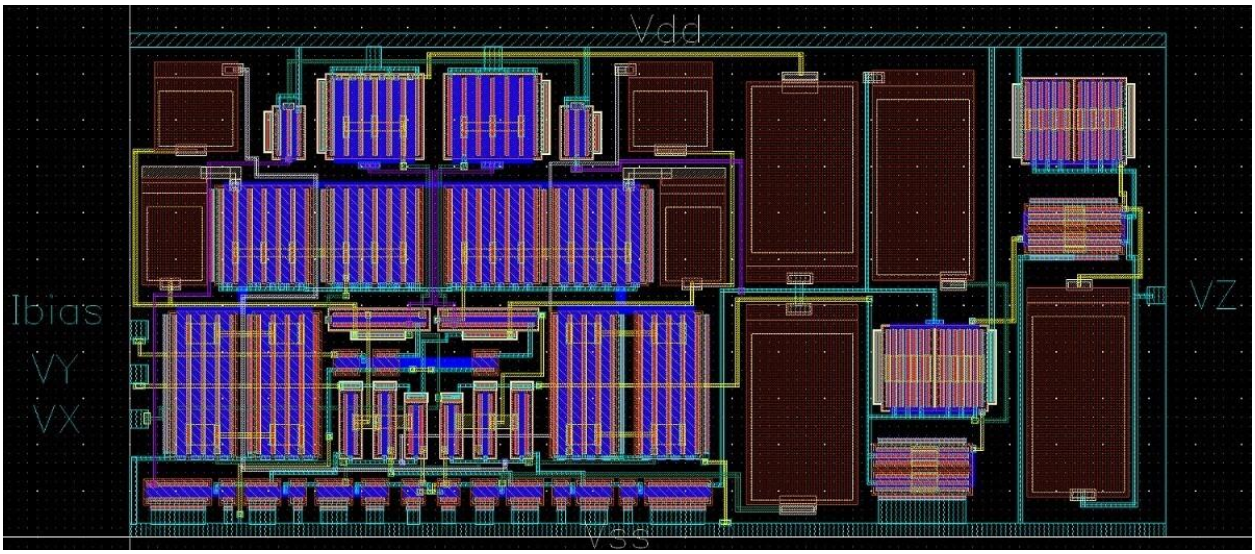

Fig. 11. Layout of proposed CCII+ cell.

TABLE II: COMPARISON OF THE PROPOSED CCII+ CELL PERFORMANCE TO THAT OF REF NOS. [9, 16–19]

Parameters	This Work		[9]	[16]	[17]	[18]	[19]
	Pre-layout Results	Post Layout Results					
Process (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18
I_{Bias} (nA)	18	18	100	20	--	40	2
Power Supply (V)	±0.25	±0.25	±1.5	±0.25	±0.45	±0.25	0.3
C_L (pF)	15	15	--	--	--	30	30
Power dissipation (nW)	342	342.2	6630	390	79300	504	37
−3 dB bandwidth (kHz)	7.4 @ X, Z	7.6 @ X, Z	2300	74.3	49200	50	2.79
Impedances at Y, Z (MΩ)	1.9×10^6, 1.7 @ Y, Z	1000002, 1.6 @ Y, Z	49, 100	0.00563, 0.00563	0.0027, 38.2 × 10^{-6}	103.75, 14	743, 112
Impedance at X node (kΩ)	10.2	10.4	138	16100	156.5	3.1	52
Voltage gain α, (V_X/V_Y)	1.0000447	1.0000892	1.002	0.999	0.972	0.998	0.999
Current gain β, (I_Z/I_X))	1.0000039	1.000014	0.997	0.999	0.987	0.999	0.999
ICMR (V)	±0.23	±0.22	±1.4	±0.2	0.45 to 0.060	−0.14 to +0.25	0.05 to 0.275
DC offset error (µV)	−1 @ X, Z	−0.96 @ X, Z	--	2000	386000	16.75	−33000 to 11000
SR_{avg} (V/ms)	34	33	--	--	--	23.75	2.7
THD (dB)	−43[a] @ X, Z	−43.8 @ X, Z	−32	--	--	<−40	−40
I_{noise} (µV/√Hz) @ 1 kHz	1.65 @ X, Z	1.67 @ X, Z	--	0.5	0.02167 @ 10 MHz	--	--
FOM (kHz/nW)	0.0199	0.0194	0.324	0.152	0.3143	0.077	0.0566
Area (µm)^2	--	6092.8	43627.3	22120	509.6	--	--
Simulated/ Post-layout	Simulated	Post-layout	Post-layout	Post-layout	Post-layout	Simulated	Simulated

[a]for 230 mV peak @ 250 Hz

VI. APPLICATION BASED ON PROPOSED CCII+ CELL

To ensure and validate the usability of BD-DRCM-QFG OTA based CCII+ cell, it is utilized to design MISO (multiple input single output) type voltage mode biquadratic filter and two-phase Quadrature oscillator as analog signal processing applications.

A. MISO Type Biquadratic Filter

Fig. 12 shows the circuit diagram of MISO type voltage mode biquadratic filter using single CCII+ cell. The filter has three inputs V_1, V_2 and V_3 and one output V_{out}. It comprises of two resistors and two capacitors [30].

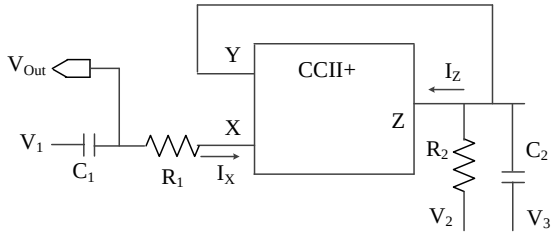

Fig. 12. MISO type voltage mode biquadratic filter [30].

Using nodal analysis, the output voltage V_{out} that correlates inputs, resistors and capacitors is given by (15)

$$V_{out} = \frac{V_1 R_1 R_2 C_1 C_2 s^2 + (V_3 R_2 C_2 + V_1 R_1 C_1 - V_1 R_2 C_1)s + V_2}{R_1 R_2 C_1 C_2 s^2 + \{R_1 C_1 + R_2 C_2 - R_2 C_1\}s + 1} \quad (15)$$

The Table III shows various input conditions for biquadratic filter responses.

TABLE III: INPUT CONDITIONS FOR BIQUADRATIC FILTER RESPONSES.

Sl. No.	Filter type	Input conditions
1.	Low-pass (LP)	$V_1 = V_3 = 0$ and $V_2 = V_{in}$
2.	High-pass (HP)	$V_2 = V_3 = 0$, $V_1 = V_{in}$ and R_1=R_2
3.	Band-pass (BP)	$V_1 = V_2 = 0$ and $V_3 = V_{in}$
4.	Band-reject (BR)	$V_3 = 0$, $V_1 = V_2 = V_{in}$ and R_1=R_2

The central frequency ω_0 and quality factor Q are given by (16) and (17), respectively.

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \quad (16)$$

and quality factor,

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{(R_1 C_1 + R_2 C_2 - R_2 C_1)} \quad (17)$$

Fig. 13 shows MISO type biquadratic filter responses that are simulated for the equal value of the capacitors C_1 = C_2 = 10 nF and R_1 = R_2 = 100 kΩ. It is found that for the LP response, f_H = 202.4 Hz, for the HP response, f_L = 125 Hz, for BP response f_L = 98.5 Hz, f_H = 257.4 Hz, BW = 158.9 Hz, central frequency f_0 = 159.2 Hz and the quality factor Q are obtained as Q = 1.002; and for BR response f_L = 98.1 Hz, f_H = 257.6 Hz, BW = 159.5 Hz, central frequency f_0 = 160 Hz and the quality factor Q is obtained as Q = 0.997. Each filter response dissipates a power of 342.2 nW.

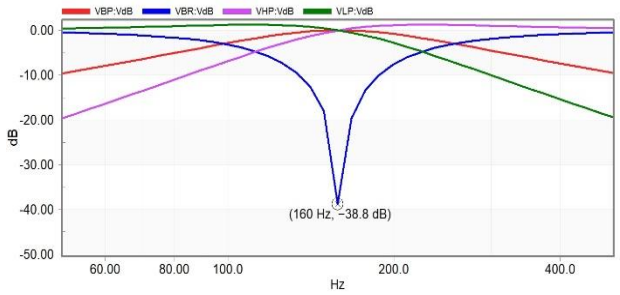

Fig. 13. MISO type voltage mode biquadratic filter responses.

The application example demonstrates as an EEG filter in the real time systems. The EEG signals' frequencies ranges from 1 Hz to 70 Hz, however the neurophysiological signals may have higher frequency

than it. This designed biquadratic filter is utilized as a frequency selective circuit (basically the band -pass filter) to study different range of frequency contained in this frequency spectrum of biomedical signal. The biomedical signal selection is done using both LP and BP filters as anti-aliasing filters, however the BR filter is used to remove the impulsive noise of certain frequency, say power supply frequency disturbances.

The other biomedical engineering applications in the real time systems includes the development of biocompatible prostheses, imaging technologies such as MRI and EKG/ECG.

B. Two Phase Quadrature Oscillator

The voltage mode two phase quadrature oscillator were proposed by [20, 31] as is shown in Fig. 14. This circuit utilizes three CCII+ cell, four resistors R_1, R_2, R_3 and R_4 and two capacitors C_1 and C_2. The parallel RC network is connected at the Z terminal of first CCII+ cell. The resistors R_2, R_3 and R_4 are connected at X terminals and Z terminal of second and third CCII+ cell, respectively. The capacitor C_2 is connected at Z terminal of second CCII+ cell. The two-phase output voltages are obtained on the nodes 2 and 4.

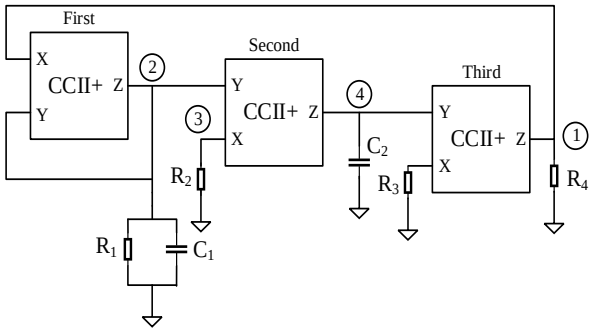

Fig. 14. Voltage mode two-phase Quadrature Oscillator [20].

By applying routine analysis on the circuit, the characteristic equation is obtained in (18)

$$s^2 + s\left[\frac{1}{R_1C_1} - \frac{1}{R_4C_1}\right] + \frac{1}{R_2R_3C_1C_2} = 0 \tag{18}$$

The condition of oscillation is given by:

$$R_1 \geq R_4 \tag{19}$$

and the frequency of oscillation is given by:

$$\omega_0 = \frac{1}{\sqrt{R_2R_3C_1C_2}} \tag{20}$$

From (19) and (20), it indicates that frequency of oscillation does not depend on the resistors R_1 and R_4 and are controlled by the resistors R_2 and R_3 independently.

If assume that $R_2 = R_3 = R$ and $C_1 = C_2 = C$, then the frequency of oscillation reduces to

$$\omega_0 = \frac{1}{RC} \tag{21}$$

When the oscillator is switched on, the voltage built up process is as shown in Fig. 15, thereafter output gets saturate to full supply swing.

In the simulation set-up of this two-phase quadrature oscillator, two equal value of resistors R_2=R_3 =12 kΩ and two equal value of capacitors C_1=C_2=20 nF are chosen. It is determined that the theoretical frequency of oscillation calculated from (21) is 663 Hz, and the simulated frequency of oscillation from the waveform is 659 Hz.

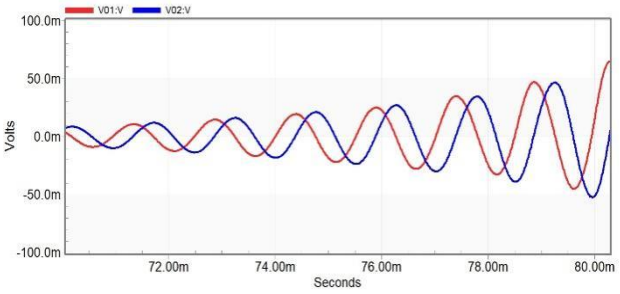

Fig. 15. Response of voltage mode two phase quadrature oscillator.

VII. Conclusion

In this paper, a bulk driven double recycling current mirror quasi floating gate (BD-DRCM-QFG) OTA and 2-CMOS inverters based CCII+ cell with power dissipation of 342 nW is presented. The circuit utilizes the dual power supply of ± 0.25 V and the bias current of 18 nA. The circuit offers a very good input common mode range and very close rail to rail operation of about ±230 mV. The circuit has good linearity and DC offset errors are −1 µV at X and Z node, respectively. The circuit provides input referred noise of 1.65 µV/sqrt Hz at 1 kHz and total harmonic distortion of −43 dB when 230 mV of peak value at 250 Hz is applied. To validate this design, layout is made and post-layout simulation is done and the circuit shows very good agreement between pre-layout and post-layout results for any design mismatches. To demonstrate the workability of the proposed circuit, voltage mode MISO type biquadratic filter using single CCII+ cell and voltage mode two phase quadrature oscillator are designed as an application example. The proposed circuit is used for LV-LP applications like bioelectronics, biosensors and extended to the biomedical systems.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

The concept, investigation, circuit analysis, software simulation, and manuscript preparation have been done by Anil Kumar Gautam. The guidance, supervision and validation of the proposed work have been done by Tripurari Sharan. All authors have approved the final version.

Acknowledgment

The proposed CCII+ cell was designed in 180 nm n-tub bulk CMOS process technology using Mentor Graphics

Tanner EDA Tools v 16.1 available in PG Lab-2 in the department of Electronics and Communication Engineering, NERIST, deemed to be University, Nirjuli, Itanagar, Arunachal Pradesh, India.

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