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Research Paper

LOW POWER BUS ENCODING FOR DEEP SUB MICRON VLSI CIRCUITS

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In recent year's low power and power aware has become a driving force in the semiconductor industry. This is due to the growth of portable electronics industry and to the growing cost of the power dissipation on buses. Because, the power dissipation related to the bus is becoming the major part of the total power dissipation in low power VLSI. The power dissipated by DSM bus is directly related to the switching activity of the coupling capacitance that exist between the bus lines and also the switching activity of the self capacitance present between the bus interconnect and the ground. In this paper we develop a new technique to reduce the switching activity of both self and coupling capacitances through encoding the data on buses.

Keywords: DSM, VLSI, Self transitions, Coupling transitions, CODEC

INTRODUCTION

In CMOS circuits most power dissipated as dynamic power for charging and discharging of internal node capacitances. Thus, the power dissipated by an IC at these I/O pins is even greater than that dissipated at internal capacitance. In general, four sources of power dissipation can be given by Yan *et al.* (2002).

$$P_{Bus} = P_{Static} + P_{dynamic} + P_{Leakage} + P_{Shortckt} \quad ...(1)$$

The dynamic power dissipated in a bus is expressed as the following equation (Weste and Eshraghian, 1998).

$$P_{Bus} = \Sigma C_{load} V^2_{dd} f_{clk} \alpha \quad ...(2),$$

C_{load} is the total load capacitance attached to a bus line, V_{dd} is the voltage swing at operation, and α is the transition activity factor. Power dissipated by bus can be reduced by reducing either by reducing C_{load}, or V_{dd} or f_{clk} or α. The transition activity factor α is given by Sainarayanan *et al.* (2006).

$$\alpha = \alpha_s C_s + \alpha_c C_c \quad ...(3)$$

where α_s is the self transition activity factor which arises from the changes from the changes in a particular bus line, C_s is the self capacitance, i.e., the capacitance between the bus wire and the ground, α_c is the coupling

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transition activity factor which arises due to the difference in bits carried by adjacent bus lines and C_c is the coupling capacitance, i.e., the capacitance between two adjacent bus wires.

In DSM technology coupling capacitance is comparable to or exceeds the self and substrate capacitance. Therefore techniques for minimizing switching activity at external buses and data buses, even at the expense of a slight increase in switching activity at internal capacitances, are being investigated for reducing power consumption (Stan and Burleson, 1995; and Sotiriadis and Chandrakasan, 2000). In paper Ravindra *et al.* (2005), both coupling and self transitions have been considered and a new technique is proposed for reduction of both coupling and self transitions. In this paper a new technique is proposed to reduce coupling and self transitions.

BACKGROUND

Several techniques exist in literature for reducing power dissipation in VLSI circuits. Some of them aim at reducing data bus transitions (switching activity) during transmission of data. They attempt to reduce the power dissipation by minimizing the bus transitions. Among them, Bus Invert method (BINV) introduced by Stan and Burleson (1995), attempts at reducing the power dissipation by minimizing the number of self transitions. In this paper, encoding was performed to reduce the dynamic power dissipation per cycle of a bus line due to self switching was effective when the coupling capacitance C_c was negligible compared to line-ground capacitance. It needs one extra line to send the coding information to the decoder. In deep sub micron technology, coupling transitions also affect the power dissipation predominantly. The fact that power dissipation due to coupling transitions, is appreciably more (75%) than that due to self transitions, (25%) (Bakoglu, 1990), necessitates the need for reducing the number of coupling transitions also. This makes the Bus Invert method incomplete in reducing the power dissipation.

Another similar technique introduced by Natesan and RadhaKrishnan (2004) also suffers with the same limitation. Yan *et al.* (2002) introduced a new technique which considers reduction of both self and coupling transitions. In this paper, odd and even data items are considered individually for encoding. Another author Ravindra *et al.* (2005) also aims to reduce the total number of transitions. The technique developed in this paper reduces the total number of transitions more effectively than all the above techniques. We also require two extra lines to send the control information. Another encoding technique was introduced by Naveen *et al.* (2004) in their paper for coupling transition reduction.

In our paper, we develop a new technique to reduce coupling and self transitions through data encoding on bus. It is presented later with an example followed by simulation results and conclusions.

ALGORITHM

B = Bus width,

N = Number of data items to be transmitted,

C_1C_2(0) = 00; Case0 //direct transmission of data //

C_1C_2 (1) =01; Case1 // shift left the data and transmitted //

C_1C_2 (2) = 10; Case2 //odd lines of the data encoded

and transmitted //

C_1C_2 (3) = 11; Case3 // even lines of the data encoded

and transmitted //

K = 2 to N;

D_1 = First data item {a_1 a_2 a_3 a_4 a_5 a_6 a_7 a_8 C_1 C_2}

D_K = Next data item

= {B_1 B_2 B_3 B_4 B_5 B_6 B_7 B_8}

D_K = Complement of D_K.

D_K^1 = {B_1 B_3 B_5 B_7 B_2 B_4 B_6 B_8} // regrouped data//

D_K^{11} = Encoded form of data D_K.

$OG(D_K)$ = {B_1 B_3 B_5 B_7} // odd bit nibble of regrouped data //

$OGT(D_K)$ = CT + ST w.r.t the first four bits of D_1.

$EG(D_K)$ = {B_2 B_4 B_6 B_8} // even bit nibble of regrouped data //

$EGT(D_K)$ = CT + ST w.r.t the next four bits of data D_1.

Start: If $CT(D_K) > [(B/2) — 1]$

begin

Case 3: If $EGT(D_K) > OGT(D_K)$ then

D_K^{11} = {B_1 B_3 B_5 B_7 followed by 1 0 1 0xnor (B_2 B_4 B_6 B_8) C_1C_2 (3)}

D_K^{11} = {b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 C_1C_2 (3)}

else

Case 2: D_K^{11} = {1 0 1 0 xnor B_1 B_3 B_5 B_7 followed by B_2 B_4 B_6 B_8 C_1C_2 (2)}

D_K^{11} = {b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 C_1C_2 (2)}

Bus ← D_K^{11}

$D_K = D_K + 1$;

$D_1 = D_K^{11}$;

If K ≤ N, go to Start;

end

else

begin

If ($ST(D_K) > N/2$) then

Case 1: D_K^{11} = {B_2 —— B_1 C_1C_2 (1)}

D_K^{11} = {b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_1 C_1C_2 (1)}

else

Case 0: $D_K^{11} = D_K$

= {b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 C_1C_2 (0)}

Bus ← D_K^{11}

$D_K = D_K + 1$;

$D_1 = D_K^{11}$;

If K ≤ N, go to Start;

end.

DECODER HARDWARE IMPLEMENTATION

The decoding hard ware is shown in Figure 1. It generates the final data received in the correct form. In the xnor block of Figure 2, the xnor logic will be performed between the encoded nibble and 1010. The shift left data is decoded by shift right module present in the decoder circuit.

SIMULATION RESULTS

The algorithm has been simulated for 10^5 random vectors generated in C. The simulation

Figure 1: Hardware Implementation of Decoder

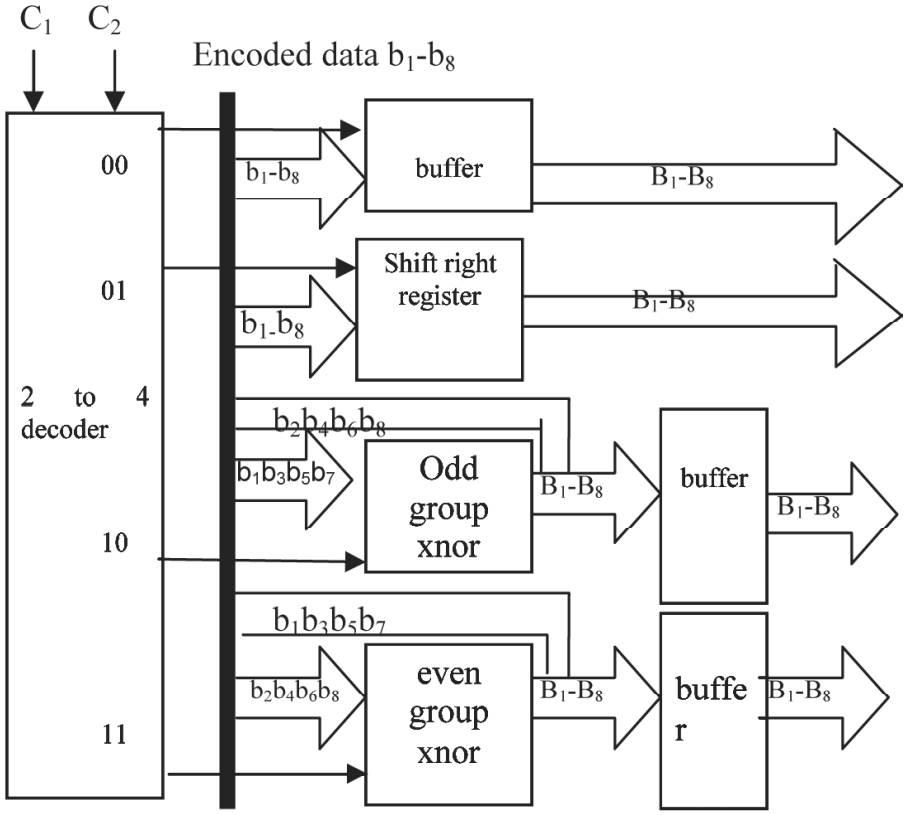


Figure 2: Xnor Decoder

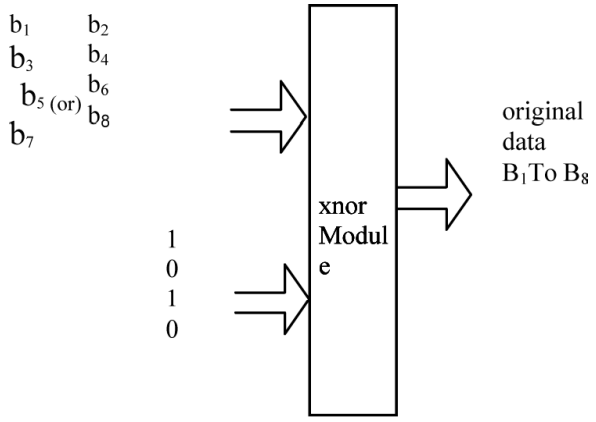
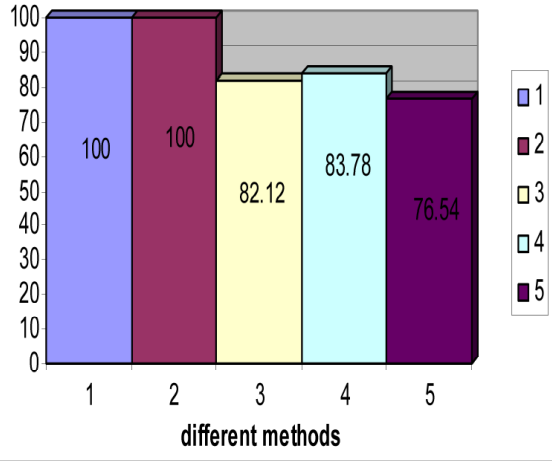


Figure 3: Reduction in CT



results are shown in Figure 3 for reduction in CT. The results show clearly a reduction of:

- Coupling transitions by 23.46%,
- Self-transitions by 15%.

CONCLUSION

Our algorithm results in reducing the coupling transitions better than any other scheme reported so far. In the case of standard one

lakh randomly generated data vectors the percentage of reduction in coupling transitions is found to be higher than the nearest reported value. Various other algorithms using xor, complement and shift right are tried and results are being processed. They will be reported at an appropriate time.

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