

Effect of Multi-fin with Independent LER on Intrinsic Statistical Variability Sources

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Abstract—FinFET devices are more prone to variations introduced by various intrinsic sources in the sub-nanometer region. In the present work, an effect of multi-fin with independent Line Edge Roughness (LER) has been analyzed to observe its influence on threshold voltage variation on intrinsic variability sources for a 14-nm FinFET device. The multi-fin analysis has been performed using the full 3-D device simulator for different fin shapes, i.e., curve-bent FinFET and thin-fat FinFETs. These independent LER FinFET devices parameters have been compared with the ideal FinFET (without LER) device. The result shows that multi-fin architecture helps mitigate intrinsic statistical variabilities adverse effects. For instance, the multi-fin device has 76.13% and 74.48% improvement in curve-bent FinFET and thin-fat FinFETs, respectively, compared to the single-fin devices. Finally, this work suggests that multi-fin devices are robust from variations introduced by various intrinsic variability sources.

Index Terms—FinFET, Line Edge Roughness (LER), multi-fin, nanotechnology, microelectronics, Very-Large-Scale Integration (VLSI)

I. INTRODUCTION

The semiconductor industry has continuously pursued better alternatives to conventional MOSFETs as device dimensions have shrunk below the sub-nanometer regime [1]. Many researchers have proposed several innovative novel devices that could be used to reduce the effect of Short Channel Effect (SCE) in MOSFETs [2–5]. Among these new alternative devices, the FinFET device has attracted a lot of interest because of its manufacturing process compatibility with conventional MOSFET devices [6–9]. Furthermore, FinFET devices have better electrostatic control of the gate region and can tolerate low-channel doping [5]. Rathore, Srivastava *et al.* [10, 11] revealed the difficulties introduced by various variability sources in single-fin FinFETs devices. However, Rathore and Rana [12] showed that FinFET devices are more susceptible to variability due to the limitation of the manufacturing process. Braravelli, Marchi *et al.* [13] revealed that maintaining constant body thickness (fin-width) along the channel region is quite challenging because fin-width varies in the vertical direction due to Line Edge Roughness (LER).

Gustin *et al.* [14] have discussed the fin-width variation's role in the FinFET device's lateral direction due to the Line Width Roughness (LWR). The LER and LWR mostly appear during the resist-defined patterning technique used to fabricate FinFET devices. The LER and LWR are mostly caused by the slow dissolving of large polymer aggregates during the removal of unwanted photoresist material [15]. Therefore, this will lead to variations in the electrical parameters of the FinFET device.

The threshold voltage (V_{TH}) is a key parameter for FinFET devices. All other electrical performance parameters, viz. power (P), OFF-current (I_{OFF}), and ON-current (I_{ON}), are directly dependent upon the value of V_{TH} . Slight variation in V_{TH} will be reflected on the transistor's P, I_{ON} , and I_{OFF} . This work analyses the effect of multi-fin with independent LER on intrinsic statistical variability sources.

This paper is organized as follows. Section II proposes the design of the multi-FinFETs. Section III presents the result analysis of multi-fin on threshold voltage (V_{TH}) variation. Finally, Section IV concludes the work and recommends the future aspects.

II. DESIGN AND CONSIDERATIONS OF MULTI-FIN FINFET

The design of multi-fin FinFET with independent LER for 14-nm FinFETs has been realized in this work. The effect of independent LER for spacer (i.e., bent+curve fins)-and resist (fat+thin fins) defined multi-fin FinFET architectures have been studied using TCAD simulation. A fin pitch of 42 nm has been taken for 14-nm FinFET, while fixing the fin height to 20 nm [16]. The remaining parameters are the same as calibrated earlier for single-fin FinFET in the author's previous publications [12].

In summary, Fig. 1 depicts the underlap FinFET device structure in 3-D and from a cross-sectional perspective. The underlap FinFET in the current work was developed in accordance with predictions made by the International Technology Roadmap for Semiconductors (ITRS) [16]. The source/drain extension region has been modified to integrate the gradient Gaussian doping profiles. The Titanium Nitride (TiN) metal has been used for the gate electrode because TiN shows low resistivity, high melting, thermal stability, and compatibility with the standard CMOS process [17]. Here, V_{TH} is considered by applying the maximum transconductance ($g_{m,max}$) method [18]. In

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this method, an intercept of the tangent is drawn to the point of maximal transconductance in the transfer characteristic.

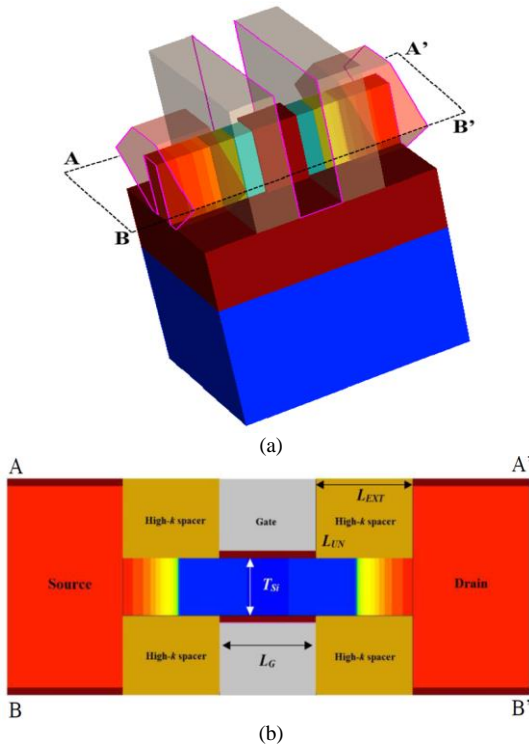
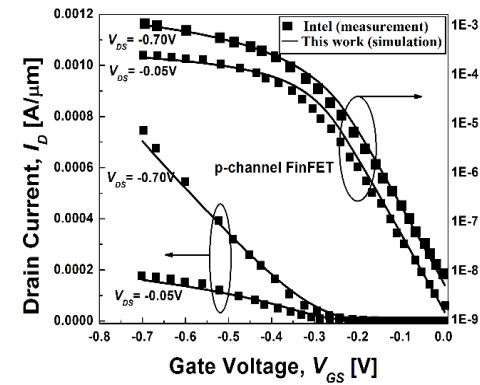
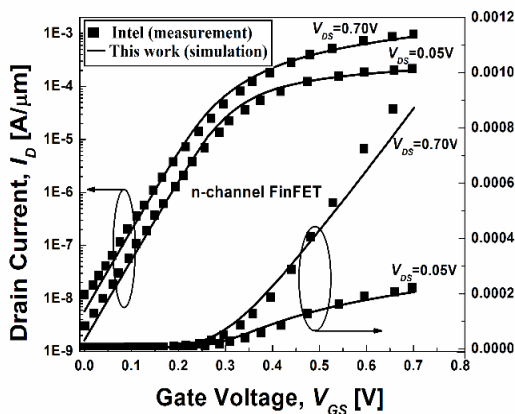


Fig. 1. The FinFET structure: (a) Three-dimensional full view and (b) cross-sectional view of the underlap FinFET device.



(a)



(b)

Fig. 2. I_D - V_{GS} characteristics calibrations with fabricated Intel 14 nm FinFET structure: (a) p-channel FinFET and (b) n-channel FinFET.

The I_D - V_G characteristics of our FinFET device are calibrated with 14 nm FinFET fabricated by Intel [12], [19]. Similarly, p-type 14 nm FinFET structure is calibrated. The calibrated I_D - V_G characteristics of the p- and n-channel FinFETs are shown in Fig. 2(a) and (b), respectively. The characteristics results of the Intel experimental device and our simulated FinFET are showing promising overlapping as shown by Fig. 2. This gives reason to believe that the TCAD simulator can accurately mimic the behavior of the 14 nm FinFET structure developed by Intel.

The overall body thickness changes in FinFET structures are mainly caused by LER. The LER has a major impact on the device performance characteristics in the sub-20 nm technology node [20]. LER is a result of lithography and etching process limitations in fabrication process of the FinFET device [21]. This will result in changes to the fin's vertical and lateral orientation in the FinFET structure. This is important to distinguish between line edge roughness (LER) and line width roughness (LWR). Thus, the LER and LWR patterns are seen in Fig. 3. In Fig. 3(a), LER reflects the differences in both sidewall line pattern of the fin about its average value, whereas as shown in Fig. 3(b), the deviations in line width to the average value to fin thickness are known as LWR.

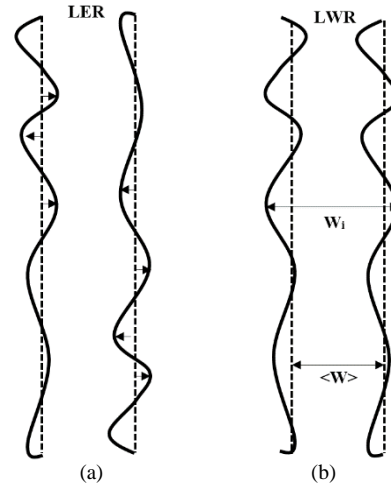


Fig. 3. LER and LWR patterns: (a) LER is fluctuation of real edge position (solid line) about its average value (dotted line) and (b) LWR is deviation of line width along the line pattern.

The expression of LWR is given by [12],

$$A_{LWR}^2 = \frac{1}{N-1} \sum_{i=1}^N (W_i - \langle W \rangle)^2 \quad (1)$$

where N is the number of samples along the length of the fin sidewall, W_i is the width of i th sample, and $\langle W \rangle$ is the mean value of fin thickness. LWR describes the magnitude of fin width roughness. The following equation illustrates the relationship between the individual left- and right-edges of the fin and LWR:

$$A_{LWR}^2 = A_L^2 + A_R^2 - 2\rho_x A_L A_R \quad (2)$$

where ρ_x stands for the cross-correlation coefficient between the left and right edges of the fin, and A_R and A_L

are the fluctuation in the right and left edges of the fin, respectively. The value of ρ_x fully relies on the fabrication method and it ranges from -1 to $+1$, with $+1$ denoting perfect-correlation between the left-and right-edges of the fin and -1 denoting anti-correlation of edges. If we assume that the left-and right-edges of the fin fluctuate by the same amount, then equation (2) can be simplified as follows to yield the magnitudes of LER and LWR:

$$A_{LWR}^2 = 2A_{LER}^2 (1 - \rho_x) \quad (3)$$

Thus, from Eq. (3) if $\rho_x = 1$, then $A_{LWR} = 0$. If LER is not equals to zero, it still produces a perfect correlation between the left and right edges of the fin. This indicates that LER has no effect on the overall thickness of the fin. Using the spacer specified patterning method rather than the traditional resist defined patterning methodology will result in perfect correlation between the two fin edges.

The geometric shapes of resist-defined FinFETs has been mathematically modelled and generated by MATLAB, which is further integrated into the TCAD simulation. A set of models have been created to capture V_{TH} variation in scaled CMOS devices. These models show the scaling pattern of arbitrary V_{TH} fluctuations and assist in assessing the effect on circuit performance. For a resist-defined gate electrode the variation in A_L is given by authors' previous work [12].

The high performance of FinFET is strongly dependent on the fin Aspect Ratio ($AR = H_{fin}/T_{si}$) for multi-fin FinFETs larger AR enhances the channel controllability. The $AR=2.5$ has been taken as a nominal device. The design of FinFETs with vertical channels is impacted by the varying AR of fins, which represents the various charge-control capabilities.

III. RESULTS ANALYSIS OF V_{TH} VARIATION

The effects of fin-width lateral variations on threshold voltage (V_{TH}) have been analyzed for single-fin FinFET structures. The V_{TH} sensitivity to T_{si} is calculated at nominal T_{si} with ± 4 nm variation, as shown in Table I.

TABLE I: FIGURES OF MERIT FOR REALISTIC PROCESS CORNERS FOR THE SPACER-AND RESIST DEFINED FINFETs

Type	Width control (nm)	$V_{T, min}$ (mV)	$V_{T, max}$ (mV)	V_T range (mV)	V_T range (%)
Spacer defined	± 4	222.05	232.61	10.56	4.75
Resist defined	± 4	240.58	262.22	21.64	10.74

The simulation results show for spacer-based lithography, ΔV_{TH} variations are the smallest among all the structures. However, it increases to the same level as resist-based lithography structures due to degraded electrostatic integrity. For resist-based FinFET structures designs, ΔV_{TH} increases because the electrostatic potential around the channel region is asymmetrical with respect to spacer-defined FinFET structures; thus, the V_{TH} variations induced by the spacer-defined lithography devices are $\sim 50\%$ smaller than the resist-defined FinFET

structures. In the following analysis, we assume, in the FinFET case, a processed induced variation ($\pm 3\sigma$) of fin width ± 4 nm. Table I summarize the calculated shift in threshold voltage. The spacer-based lithography structures will have a V_{TH} range improved by more than $2x$.

The electron current density profile with independent LER is shown in Fig. 4. Here, independent LER results in the body/channel region of multi-fin structures bending and curving (spacer-defined) or becoming fat and thin (resist-defined), which results in a different electron density in the middle of the fin compared to the rectangular multi-fin FinFET structure. Therefore, the path of charge carriers should generally correspond to the geometry of the fins.

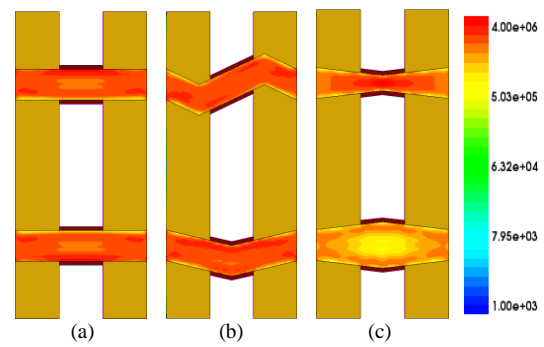


Fig. 4. Device structures and electron current density profile with independent LER (a) Rectangle (without LER), (b) curve-bent FinFET and (c) thin-fat FinFET.

The channel of spacer-defined FinFETs has a more uniform electron density distribution under the gate electrode than the resist-defined FinFETs, which demonstrates that both multi-fins have different channel controllability. Fig. 5 compares the σV_{TH} of intrinsic parameter fluctuations for single and multi-fin in both spacer-and resist-defined FinFETs with independent LER. It is clear from Figure that σV_{TH} for the individual and combined impact of Random Dopant Fluctuation (RDF), Oxide Thickness Variation (OTV), and Work Function Variation (WfV) can be suppressed using the multi-fin architecture in both the spacer- and resist-defined FinFETs. The overall σV_{TH} decreases from 32 mV to a reputable 8 mV, as shown in Fig. 5(a), i.e., the σV_{TH} improvement of 76.13% for multi-fin w.r.t. single fin spacer defined FinFETs. Similarly, for resist-defined FinFETs, the σV_{TH} decreases from 38 mV to 10 mV, i.e., the reduction of σV_{TH} variability is about 74.48%. This is because AR remains unchanged as in the case of spacer-defined FinFET as the overall thickness remains the same i.e., 8 nm but in case of resist-defined FinFET AR is a function of fin thickness, it changes dramatically with a low value for thin FinFET and high value for Fat FinFET leads to more fluctuations.

The device with a higher AR and a greater number of fins possesses a large on-state current. Moreover, the Multi fin FinFETs offer better driving capability than that with a single-fin structure. There is a significant improvement in σV_{TH} , especially in resist-defined FinFETs this is because we have taken an independent

LER profile for multi-fin (i.e., fat+thin fin). Finally, as shown in Fig. 5(c), comparing resist-defined FinFET structures with spacer-defined FinFET structures possesses a smallest σV_{TH} variation. The σV_{TH} differences for spacer-and resist-defined FinFET structures are 57.11% and 39.90%, respectively. The results of this study indicate that the σV_{TH} variations of the multi-fin structure is significantly smaller than that of the single-fin one, and the structures with multi-fins and a large AR as in the case of spacer-defined FinFETs may exhibit better fluctuation suppression.

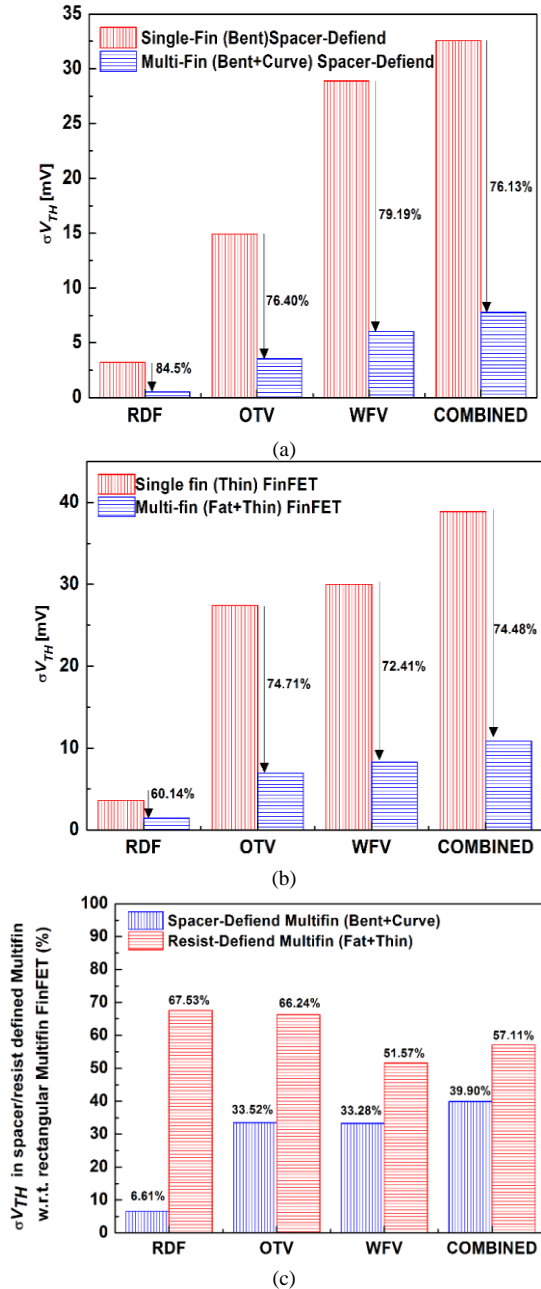


Fig. 5. σV_{TH} of intrinsic parameter fluctuations as a function of single and multi-fin (a) Spacer defined, (b) resist defined and (c) spacer-resist defined.

Furthermore, impact of multi-fin has been analyzed for SRAM cell due to various variability sources. Fig. 6 shows the variation in SNM due to the contribution of

various intrinsic variability sources for spacer-and resist-defined FinFETs w.r.t. rectangular FinFET. It is observed that, the suppression of variability sources within the SRAM bit-cell is least affected in spacer-defined FinFETs as compared to resist-defined FinFET. This is due to, in an ideal case of spacer defined FinFET the in-phase correlation between LER on the both edges of the fin results in zero fin width fluctuations. But it is totally uncorrelated in resist defined FinFET hence these non-zero and random uncorrelated values of fin width give rise to more SRAM variability. Fig. 6 also shows the SNM performance due to the combined sources of intrinsic variability. It is clear from figure that rectangular FinFET exhibit the best SNM performance followed by the spacer-defined FinFET structure. Therefore, it is suggested that using spacer defined patterning technique improves the intrinsic matching with respect to resist defined FinFET, thus allowing the mainstream use of FinFET in aggressively scaled SRAM circuits.

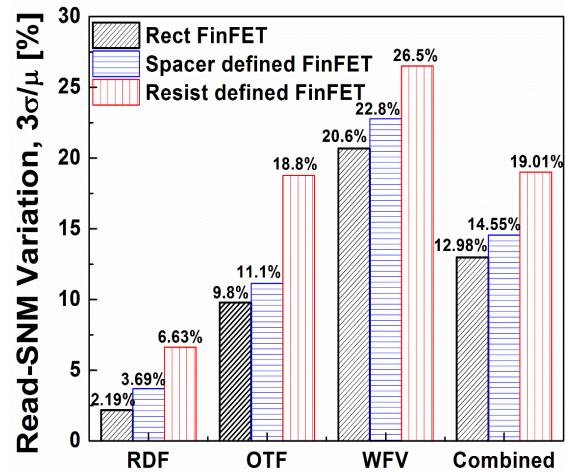


Fig. 6: Read-SNM Variability in rectangular, spacer and resist defined 6-T SRAM bit-cell.

IV. CONCLUSIONS AND FUTURE RECOMMENDATIONS

This research work presents the effect of multi-fin with independent LER for 14-nm FinFETs. Two different Fin shapes, i.e., curve-bent FinFET and thin-fat FinFETs. Have been taken to observe its impact on V_{TH} variations. All results have been compared with the ideal FinFET (without LER) device. It is found that the multi-fin device has 76.13% and 74.48% improvement in spacer-and-resist defined techniques, respectively, as compared to the single-fin devices. The σV_{TH} differences for spacer-and resist-defined FinFET structures are about 57.11% and 39.90%, respectively. Spacer-defined FinFET shows ~5% improvement in SRAM performance over resist-defined FinFETs.

However, multi-fin structure faces some issues, such as increased device area, complex fabrication, and higher fabrication cost. Therefore, it is concluded that this work gives insight to the designers to optimize the performance of FinFET devices for reduced variation caused by intrinsic statistical variations.

In future, this work can include different materials to design the FinFET and its realization with fabrication.

CONFLICT OF INTEREST

The authors declare that they have no known competing financial interests that could have appeared to influence the work reported in this paper.

AUTHOR CONTRIBUTIONS

Rituraj Singh Rathore conducted the research; Viranjay M. Srivastava and Rituraj Singh Rathore analyzed the data; Rituraj Singh Rathore wrote the paper; both authors had approved the final version of this paper.

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