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Research Paper

SINGLE EVENT TRANSIENT HARDENING TECHNIQUE FOR LOGIC GATES BASED ON RADIATION HARDENING BY DESIGN (RHBD)

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Single event transients (SETs) have become increasingly problematic for both combinational and sequential VLSI circuits in the deep submicron technology (DSM). This is due to continuously decreasing feature sizes, lower supply voltages and higher operating frequencies. Many critical applications such as biomedical, space and military electronics as well as several mainstream computing applications demand reliable circuit functionality. Therefore, the circuits used in these application must be tolerant to SEU/SET events and therefore, these circuits are designed using circuit hardening approaches. Hardening by design techniques based on increasing the amount of charge representing the bit and redundancy techniques have been used over the years. In this paper, we present a novel design strategy to reduce the impact of radiation-induced single event transients (SET) on combinational logic circuits. This design style achieves SET mitigation by using C element and strengthening the sensitive output node. In order to check the accuracy of our proposal, we compare it with others techniques for hardening radiation at the transistor level against a single event transient. Simulation results show that the proposed method has a good soft error tolerance capability as well as better noise immunity.

Keywords: Single event transients (SET), Radiation hardening, Soft errors, C Element, Strengthening

INTRODUCTION

As today's process technologies scale down to DSM technology, keeping the signal integrity becomes increasingly very difficult. Transient errors created by ground bounce and IR drop in voltage supply, signal cross-coupling effects, and terrestrial radiation cause reliability issues and compromise security in unpredictable

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ways. The errors due to radiation effects from high energy neutrons, alpha particles and protons can cause either soft errors or hard errors in the digital circuits. The circuits in the DSM technology are more susceptible to the radiation effects which have recently become a growing concern. This is mainly due to shrinking feature sizes and increasing clock frequencies in CMOS logic. The soft errors are mainly induced by the alpha particles and cosmic rays striking the sensitive area within a combinational circuit. The sensitive areas are the depletion regions of the transistor drain or the reverse biased p-n junctions. The radiation strike causes electron hole pairs and these free carriers drift under the applied electric field and cause a transient voltage pulse or a single event transient (SET) (Pitsini Mongkolkachit and Bharat Bhuva, xxxx). The SET can pass through a series of gates and if reaches a memory element then it becomes a single event upset (SEU) (Sohan Purohit *et al*., 2010).

The main reason for increased sensitivities to transient pulses caused by SE particles is the simultaneous reduction of both the transistor size and the supply voltage V_{dd}, which occurs with scaling. As a result, the charge to store a logic "1" at a circuit node ($Q = V_{dd} * C_{node}$) also reduces. In other words, a significantly lower charge deposed by a particle strike suffices to flip the logic value of a node. Increasing clock frequencies also increases the circuit vulnerabilities to these transients as the chance to capturing these transients also increases. Advances in technology scaling cause increased coupling effects due to decreased spacing and increased thickness to width ratio of interconnects. With enough coupling, an SET pulse can easily spread from one part of the circuit to unrelated parts of CL causing SE crosstalk noise effects.

When a charged particle strikes at a sensitive node such as the drain node of an OFF-transistor in a CMOS gate, electron – hole pairs are created along an ionization track. Finally, a transient current pulse is generated following the drift and diffusion mechanisms. The current pulse generated is usually modeled by the following double exponential waveform:

$$I(t) = \frac{Q}{\tau\alpha - \tau\beta}\left(e^{\frac{-\tau}{\tau\alpha}} - e^{\frac{-\tau}{\tau\beta}}\right)$$

where Q is the charge (positive or negative) deposited by the particle strike, ôá is the collection time constant of the p-n junction, and ôâ is the ion-track establishment time constant. The time constants ôá and ôâ are dependent on process technology and can be taken as 0.1 ns and 0.05 ns, respectively.

Indeed, any combinatorial block has also to be hardened to mitigate SET propagation (Sohan Purohit *et al*., 2010). There is an additional sensitivity issue for asynchronous circuits since the input events drive the circuit and not a clock signal. The state changes occur in direct response to signal changes on the input lines, and different memory elements can change state at different times. To counter the effects of SETs, several technological and by design techniques exist. This brief focuses on radiation hardening by design (RHBD) techniques. Many conventional RHBD techniques exist for different abstraction levels. For example, for a transistor level, exist the transistor sizing and transistor folding techniques exist. For a combinatorial level,

logical masking is used. On a system level, three main redundancy techniques exist, i.e., hardware, temporal, and information redundancy. Those techniques focus on hardening the system either by hardening the transistors or the output of the system without changing the system itself. The extra hardware used for hardening brings important power and area overheads. This brief proposes a system that acts as an SET temporal filter and a strengthening technique which acts as a checkpoint with self-healing properties to prevent SET propagation and SET mitigation at the sensitive node.

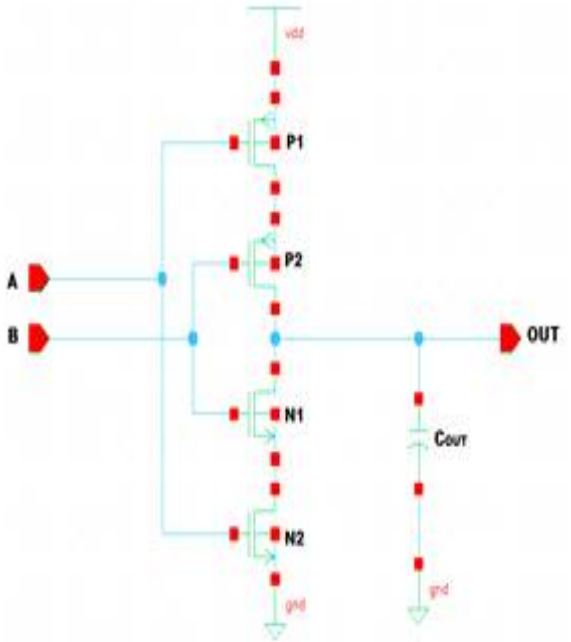
PROPOSED SET TOLERANT DESIGN TECHNIQUE

A. Hardening By Using C – Element

The function of a C-element [1] is basically to compare the logic states of its inputs. When the inputs are identical, the state of its output will be updated to reflect the inputs' state. The C element in this condition works as a buffer. In the case when its inputs are not identical, the output state will be preserved. In this case, the C-element works like a memory element. The idea of temporal filtering is to stop the SETs coming from previous stages, considering them as glitches. A simple approach is to add a downsized latch at the input of a sequential element to slow down the data transitions and as a result to filter out SET (Rodrigo Possamai Bastos *et al.*, 2010) pulses that are faster than its delay. The main advantage of using a C-element is that it is very simple to design. The C-element keeps the last output if the inputs are not the same, as a memory, or acts as a buffer when the inputs are equal.

The C-element may be used as a filter between two functions. This SET filter can feed

Figure 1: Basic C-element Structure



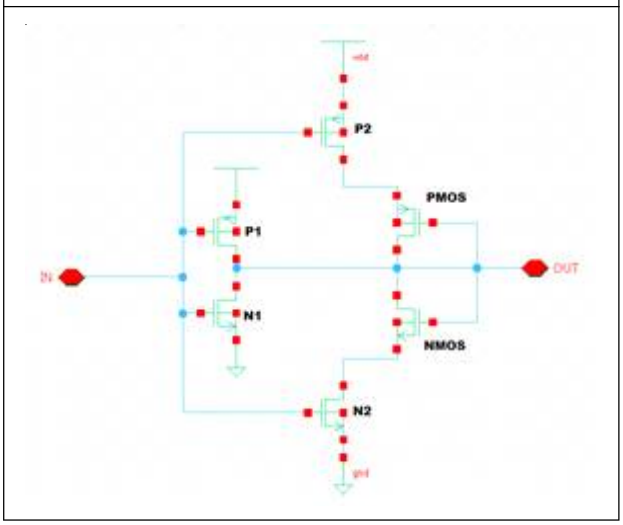
a hardened latch so that combinatorial and sequential units are both radiation hardened. If a glitch appears at the output of the combinational function and lasts less than the delay on input A, then inputs A and B will differ and the glitch will be filtered by the C-element. If the inputs A and B are different then the output gives the previous value. In recent, the authors also mentioned that values of SET pulse widths can reach values as large as a few nanoseconds and depend not only on the linear energy transfer of the striking ions but also on the considered technology (180 nm versus 90 nm, for instance). Moreover, SET pulse widths depend also on the circuit temperature. Therefore, a maximal SET pulse width has to be considered depending on the operating conditions and the targeted robustness to design the C element. Some design solutions exist in the literature to harden gates. The C-

element is a small and simple gate and those hardening strategies can be easily applied to it. The critical charge of the output can be also increased by using strengthening technique at the sensitive output node. So the C element itself can be made hardened by using strengthening technique.

B. Hardening By Using Strengthening Technique

A static logic gate is composed of two networks: (i) a pull-up network responsible for setting the high logic value to the output, and (ii) a pull-down network, responsible for transmitting the logic low to the output. If either network receive an impact or noise, and the effect reaches the gate output node, an incorrect value can be propagated up to a

Figure 2: Inverter Design with Strengthening Concept



memory element. The concept of strengthening (Calomarde *et al.*, 2013) is to make the logic gates more robust to the SET at the sensitive nodes.

The concept of strengthening is to make the logic system more robust to soft errors. The circuit is composed of pull-up and pull-down networks and a replica of both the networks. The replica networks are called as strengthening networks used to strengthen the sensitive node. The replica pull-up network is connected to the output through a PMOS transistor and the replica pull-down network is connected to output through a NMOS transistor. The PMOS is used to monitor the high level output and if the output goes low due to any SET then the PMOS connects the strengthening pull-up network to the stroked node such that the node can recover its original value. On the other hand, the operation of NMOS is similar but it monitors low level output and if it goes high due to any SET the NMOS connects the strengthening pull-down network to the stroked node and the original value is recovered at the node.

C. Proposed Hardened Circuit Using C-element and Strengthening Technique

There are different implementations of static C-element based on storing the previous logic state when the inputs are different. There is a memory circuit at the output of the basic C-element to store the previous logic state exactly without any drop in the voltage level. The figure shows the Sutherland pull up and pull down implementation of the C-element. The Sutherland implementation is more robust to load variations and suitable for low power designs. It has higher propagation delay only for high input slopes. The figure also shows the strengthening concept used with the C-element design.

The SEU tolerant design style proposed in this paper is based on the DCVSL design methodology, but modified to incorporate SEU inhibiting properties. The proposed scheme

looks very similar to the original DCVSL topology. A major difference is however that this technique relies on the use of duplicating the pull down networks as opposed to conventional DCVSL which uses complementary pull down networks. The two pull up devices are connected in a feedback style fashion and thus combine differential logic and positive feedback. As a result both the output nodes provide the same logic function OUT_BAR.

Figure 3: Proposed Hardened NAND Gate Using C-element and Strengthening

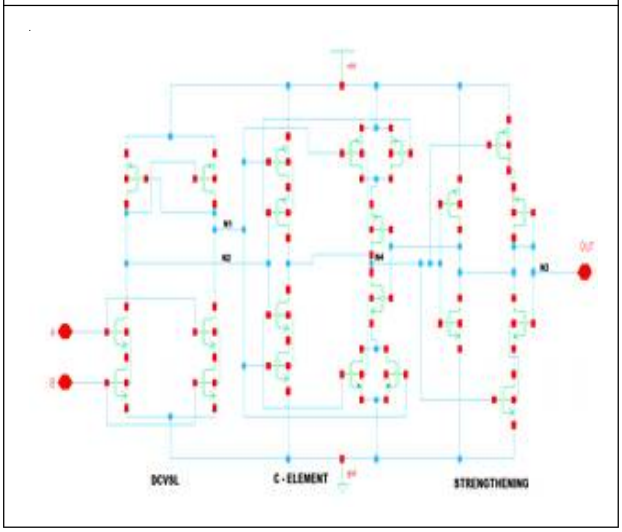


Figure 3 shows a 2 input NAND gate implementation using the proposed style. It should be noted that although intuitively for the basic NAND, NOR, XOR gates, this topology seems to just duplicate the pull down networks, the technique allows for using shared transistors while implementing larger logic functions. Similar to DCVSL, this approach allows the designer to limit the overhead while implementing large logic functions. Another important advantage offered by this design style comes through the reduction of a full PMOS pull up network. The two PMOS transistors shown in the figure act as keeper transistors for each of the individual pull down networks. The elimination of a dual PMOS pull up network provides significant advantages in terms of area and overall transistor density of the circuit. The C element along with strengthening technique is applied at the outputs of the DCVSL logic to remove the SET at the inputs and output of the logic gate.

SET HARDENING EVALUATION

In order to explain how the proposed technique achieves SET hardening we consider the NAND gate implementation of the proposed technique. The basic idea is to duplicate the pull down networks in the DCVSL configuration to achieve SET hardening. The inputs to the C-element are the outputs of the DCVSL logic which are same when there is no SET on the pull down networks. If any SET occurs in any one of the pull down network then either the node N1 or node N2 is affected but this does not affect the output of the C- element as the

Figure 4: SET at N1 and N2 in the proposed style NAND gate

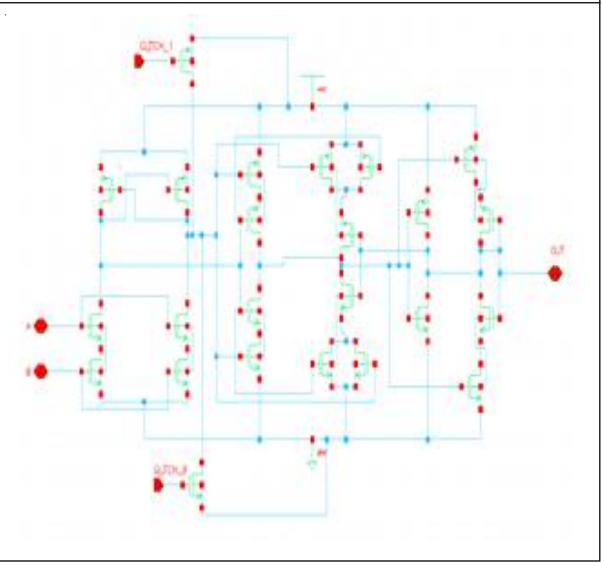
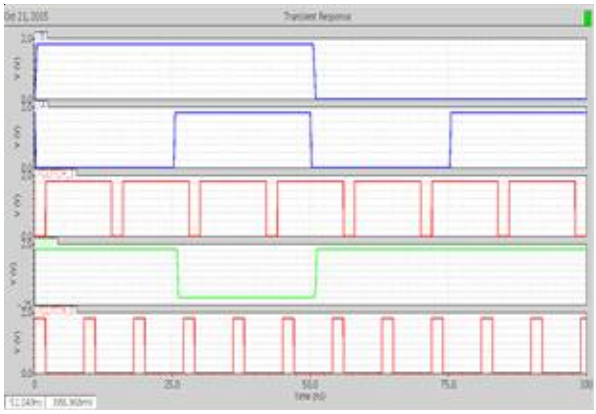


Figure 5: Output Waveform of NAND gate with SET at N1 and N2



output remains in high impedance state when the inputs of C-element differ. Thus any error on the node N1 or N2 is removed by the C-element.

If the node N3 is affected by SET then the feedback transistors in the strengthening network will attempt to regain the correct logic value. Hence the output of the NAND gate is hardened with the help of the strengthening technique. By proper sizing of the strengthening network the output voltage swing can be increased. The node N4 is hardened

Figure 6: SET at N3 in the Proposed NAND Gate

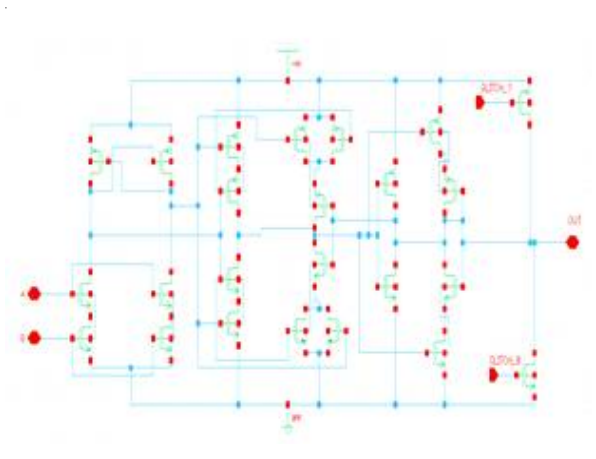
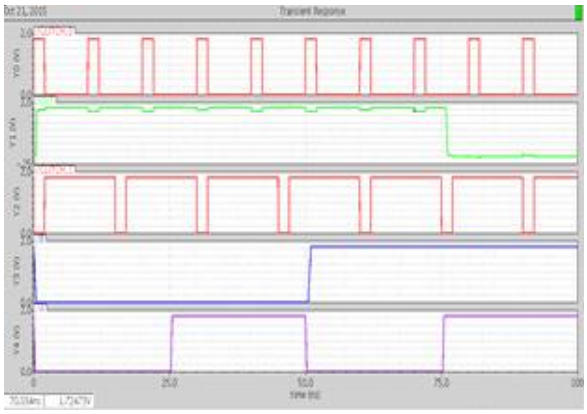


Figure 7: Output Waveform of NAND Gate with SET at N3



such the logic at node N4 is provided by two different paths. So if one of the path is affected by SET the other path can provide the correct logic value. Thus the node N4 is also hardened for any SET.

The performance of the proposed circuit was evaluated by simulation with CADENCE virtuso. To determine the practical power dissipation and propagation delay a much complex circuit is designed with the hardened gates designed by the proposed style.

SIMULATION RESULTS

To further quantify the characteristics and performance of the proposed circuit we have designed different logic gates such as NOR, AND, OR, XOR and calculated the power dissipation and delay of these gates. In order to evaluate the effective performance of the proposed style of logic design we have implemented standard circuits such as 4-bit multiplier, 8x1 multiplexer and 4-bit parallel adder and carry look-ahead adder using the logic gates designed by the proposed style. We observed that there is an area saving by

Figure 8: 8-bit Multiplexer Designed by Using Proposed NAND Gate

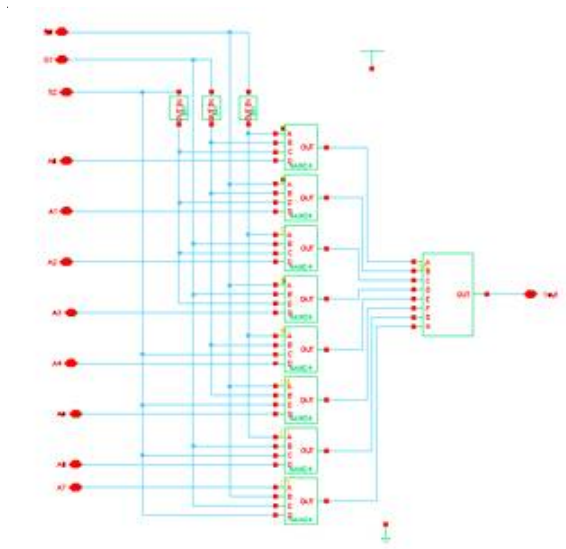


Table 1: Simulation Results for Proposed Design Style

Circuit Using Proposed Style	Power Dissipation	Delay
NAND Gate	37.9 µW	366.6 ps
4-bit multiplier	3.31 mW	1.72 ns
8x1 multiplexer	0.4 mW	1.8 ns
4-bit parallel adder	1.1 mW	1.7 ns
4-bit carry look ahead adder	1.1 mW	1.0 ns

Table 2: Comparison of Proposed Style with Previous Hardened Designs

Parameter	CDC [1]	Proposed style
Power dissipation	1.58 µW	1.12 µW
Delay	0.95 ns	0.15 ns

using the DCVSL style of logic design. The power dissipation and delay can be further reduced by selective hardening of critical elements in the circuits using standard algorithms.

The next step of evaluation the proposed circuit involved the testing for the single event effects. We tested the circuit for SETs of different pulse-widths which are mostly comparable to the modern day digital clock pulses. The proposed circuit provides high tolerance to SETs of all pulse widths. An interesting point to be noted is that most of the circuit level hardening techniques and some of the architectural level will work effectively only when the custom designed for specific current profiles, for example it presents two sets of simulation results for two different charge values and rise and delay times of the SET pulse (error pulse). As a result even though 100% SET tolerance is claimed, it will be valid only over a limited range of specific expected current profiles. Such circuits therefore will have limited portability and need to be re-designed when migrating from one environment to another. The advantage with our proposed style of design is that the circuit design process remains relatively similar to the standard CMOS logic design while still maintaining SET robustness (Véronique Ferlet-Cavrois *et al*., 2013) over a high range of possible charges. Due to the relatively low delay overhead introduced by the proposed technique and especially the significant area savings involved by using DCVSL, it is possible to introduce a second level of hardening structure at the architectural level.

CONCLUSION

This paper proposes a new design style that effectively reduces the impact of radiation induced single event transients on the logic

circuits. The proposed style derives its structure from the DCVSL design topology. The proposed style can be used in both static and dynamic CMOS logic circuit designs. The style allows higher integration density than that of conventional static CMOS designs while maintaining a comparable delay and power profiles compared to other SET mitigation techniques. The area, power, and speed penalties for the proposed technique are comparable to the other SET mitigation techniques in use by the community. The simplicity of this design approach makes it highly suitable for wide range of practical applications of digital circuits. In space environment SET and SEU are the main particle effects, so the design style protects against real space applications with minimum area overhead and latency overhead. The future work involves developing complex logic circuits using the proposed style and enhancing modifications in the style to reduce the area overhead and delay overhead.

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