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*Research Paper*

# HIGH PERFORMANCE AND LOW POWER SRAM CELL DESIGN USING POWER GATING TECHNIQUE

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In this paper the stable and power-efficient method is presented to design and implement Static-RAM Cell. Static-RAM is one of the essential building block for the VLSI design. Due to their higher speed Static-RAM based Cache memories and System-on-chips are commonly used. Due to device scaling there are several design challenges for Static-RAM design in nanometer technology. The Static-RAM implementation is based on 45 nm CMOS submicron technology. The transmission gates are used in the access path of the SRAM Cell and the Sleep transistors power gating technique is used for low leakage power and high performance. The transient and dc analysis of the proposed ST13T Static-RAM cell has been obtained for high performance. It can be observed from the results that the percentage reduction of 33.66% in power dissipation, 62.18% in noise, 10.20% in delay and 38.14% in PDP is obtained for the proposed ST13T circuit with power gating technique are that shows the high performance for Static-RAM Cell.

Keywords: CMOS integrated circuit, Integration VLSI, Layout, Logic design, Nanometers, Static-RAM chips

## INTRODUCTION

Fabrication of thousands of transistors into a single chip in an Integrated Circuit (IC) is known as the Very-Large-Scale Integration (VLSI). In the year 1970s, VLSI technology started when upgraded semiconductor electronics technologies were being developed. Before the invention of VLSI technology, most ICs had a limited set of functions which these could perform. An electronic circuit design might consist of a CPU, ROM, RAM and other glue logic. The first semiconductor chips held two transistors each but, the subsequent advancements added many more transistors, and as a result, more versatile functions were integrated over time. The first few integrated circuits placed only a few electronics devices, i.e., as many as tens of diodes, transistors, resistors and capacitors, fabrication of one or more logic gates on a single device is made possible (Yanan Sun *et al.*, 2015).

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For nearly past 40 years CMOS devices have been scaled down to nanometer scale in order to achieve higher speed, better performance and low power consumption. Due to the higher speed requirements, the Static-RAM based Cache memories and System-On-Chips (SOCs) are commonly used in most of the applications. Due to device down-scaling there are several design challenges for nanometer Static-RAM design. Now the devices with very low threshold voltages and ultra-thin gate oxide are used due to which leakage-energy consumption is getting increased. Moreover, the data storage capacity of the read and write operation is also getting affected. The intrinsic parameter fluctuation effects viz., line-edge roughness, Random Dopant Fluctuation (RDF) and gate-oxide-thickness fluctuation also reduces the stability of Static-RAM cell. In order to achieve higher noise-margin along with better performance new Static-RAM cells (Jiajing Wang and Benton Calhoun, 2011; Rajiv Joshi *et al.*, 2011; Micheal Turi and Jose Delgado-Frias, 2014; and Ghasem Pasandi and Sied Mehdi Fakhraie, 2015) have been introduced. In most of these cells read and write operations are isolated to achieve higher noise-margin. In this paper the detailed analysis of 13T Static-RAM cell has been carried out. All the simulations have been carried on 45 nm CMOS submicron-technology using Cadence Virtuoso tool.

In the recent years, the sub-threshold design for low power application is thought to be as a low energy solution. However, the memory circuits operating successfully at such low voltage are more challenging since the performance of the Static-RAM decreases at the low voltages to a large extent. Many other effects such as process-variation (PVT), bitline-leakage problem and transistors mismatches challenge the proper operation of Static-RAMs that need a precise design. In the practical sub threshold region the Static-RAM unit cell plays a important role. A robust cell design that resists to the process-variation and bit-line leakage increases the total Static-RAM performance.

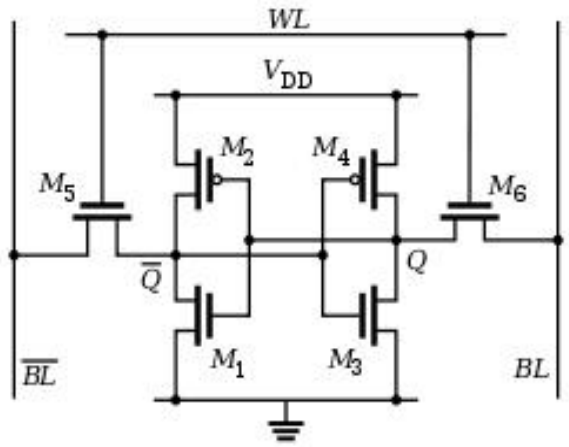
## STATIC-RAM CELLS

The overall performance of the system is dominated most of the time, by the SRAM that makes up a large portion of a system-on-chip area. Moreover, the rapid growth and the popularity of mobile, hand-held devices and other emerging applications, such as WSNs (wireless body sensing networks) implanted medical instruments, necessitates the requirement of low-power SRAMs. Hence, there exist a requirement of a robust low-power SRAM circuit design and has become important (Gahsem Pasandi and Sied Mehdi Fakhraie, 2014; Yanan Sun *et al.*, 2015; and Shairfe Muhammad Salahuddin and Mansun Chan, 2015).

However, a design of robust low-power SRAM faces many process and performance related challenges. This is because, in deep sub micrometer technology, near/sub threshold operation is very challenging due to increased device variations and reduced design margins.

In addition, with each technology node, the share of leakage power in the total power dissipated by a circuit is increasing (Balwinder Raj *et al.*, 2011; and Micheal Turi and Jose Delgado-Frias, 2014). Since, most of the time,

Figure 1: Conventional 6T SRAM Cell (Balwinder Raj et al., 2011)




SRAM cells stay in the standby mode, thus, leakage power is very important.

The increasing leakage current along with process variations leads to large spread in Read Static Noise Margin (RSNM) and causes read failures at the tail of the distribution (Balwinder Raj *et al.*, 2011). The short-channel effect and sub threshold leakage currents of conventional silicon MOSFETs (Si-MOSFETs) are exacerbated with the miniaturization of device dimensions in each new CMOS technology generation (Balwinder Raj *et al.*, 2011; Micheal Turi and Jose Delgado-Frias, 2014; Gahsem Pasandi and Sied Mehdi Fakhraie, 2014; Yanan Sun *et al.*, 2015; Shairfe Muhammad Salahuddin and Mansun Chan, 2015; and Ghasem Pasandi and Sied Mehdi Fakhraie, 2015). Alternative materials and devices are needed to be able to continue scaling the CMOS technology.

The conventional 6T SRAM as shown in Figure 1, suffers from read-current disturbance-induced SNM degradation with Vdd scaling. Moreover, due to increased variations at low supply voltages in advanced CMOS processes, caused by global and local process variations, the read stability and the write stability of 6T SRAM cell degrade to unacceptable level. This is further exacerbated by the half-select disturb and conflicting read/write requirements. To overcome these challenges, different configurations of SRAM cells, such as 7T (Jiajing Wang and Benton Calhoun, 2011; and Rajiv Joshi *et al.*, 2011), 8T (Khare *et al.*, 2014), 9T (Vandana Sikarwar *et al.*, 2013; and Joshika Sharma *et al.*, 2015), and 10T (Shyam Akashe *et al.*, 2012; Basavaraj Madiwalar and Kariyappa, 2013; Prathamesh Chodankar *et al.*, 2014; and Deeksha Anandani *et al.*, 2015) cells, have been proposed. In these circuits, data storing nodes are fully decoupled from read-access path to overcome the conflicting read/write requirements. This approach offers an RSNM that is almost the same as hold SNM (HSNM), therefore, resulting in better read stability. The conventional 8T (Khare *et al.*, 2014) uses two extra transistors in the read path and one extra Bit Line (BL) for reading. However, it suffers from leakage introduced in read path, which further increases with scaling.

Liu and Kursun proposed a differential 9T bit cell with read-disturb-free operation. It uses the same BLs for both reading and writing; however, doubling the number of transistors connected to BL increases read-access time. Another 9T SRAM cell proposed in and 10T SRAM cells proposed, independently, in use the modified versions of buffered read path that reduces the leakage of read access path, while simultaneously improving RSNM. Chang *et al.* have proposed a read-disturb-free differential 10T bit cell (hereafter called Chang 10T), which is suitable for bit interleaved

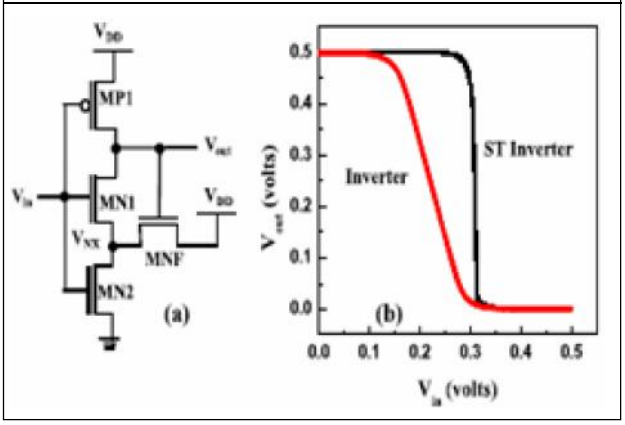
architecture. However, it incorporates two series connected transistors in its write path, which degrade the write ability of the bit cell. The word line boosting is required to work as the write-assist circuit, for a successful write operation, and so the dynamic power of the cell is increased. These bit cells address the read-disturb problem; nevertheless, having cross coupled inverter pair topology, similar to conventional 6T cell, offers little immunity to process variations at low supply voltages. The stability of the cross-coupled inverter is very important for the successful SRAM operation under Process, Voltage, and Temperature (PVT) variations (Dinesh Kumar and Noor Mahammad, 2015). Hence, in this paper, a new single-ended Schmitt-Trigger (ST)-based robust low-power SRAM cell (hereafter referred to as ST13T) is proposed, which offers lower delay, reduced power consumption along with high robustness to PVT variations.

## PROPOSED ST13T SRAM CELL DESIGN

### Schmitt-Trigger-Based SRAM Cell Design

The stability of cross-coupled inverter pair in SRAM cell operating at very low supply voltage is not very promising. Furthermore, power consumption is high due to degraded inverter characteristic. Therefore, an ST inverter is used to exploit the improved inverter characteristic. The basic element for the data storage in an ST-based SRAM cell uses a crosscoupled ST-based inverter pair shown in Figure 2a (Zhang Turi and Delgado-Frias, 2012). ST is like a comparator, which includes positive feedback. Considering the switching

Figure 2: (a) Basic ST Inverter Used for this Design, (b) Characteristics of Inverter and ST Inverter for 0 ì 1 Transition at the Input (Vdd = 0.5 V)



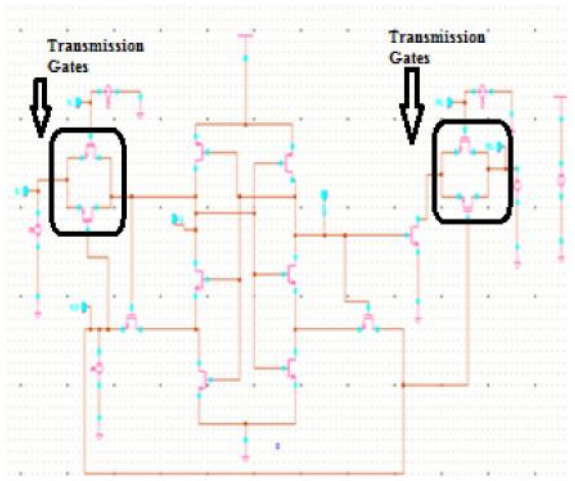

of output voltage, Vout from 1 to 0, in the case of inverter, the transition starts as soon as the input voltage reaches the Vt (threshold voltage) of the Pull down transistor, Vthn. On the other hand, in case of ST-based inverter, for Vout = 1, the feedback transistor MNF is ON and the voltage at node VNX is Vdd – Vthn. In this case, for switching at the input the minimum voltage required will be much higher than Vthn. The inverter characteristics and ST is shown in Figure 2b. Due to the improved inverter characteristic, the ST-based SRAM offers higher SNM.

### Proposed ST13T SRAM Cell

The proposed work envisages design and simulation of an schematic and layout of SRAM Cell using Schmitt-trigger based 13T configuration to study its behavior in nano scale technology node (45 nm) using simulation software Cadence Virtuoso (Virtuoso V.6.1). The schematic of the proposed design will be based on modifying the existing SRAM Cell configurations.

The various parameters for the design of SRAM Cell like read and write stability, low

Figure 3: Proposed ST13T SRAM Cell Circuit with Transmission Gates



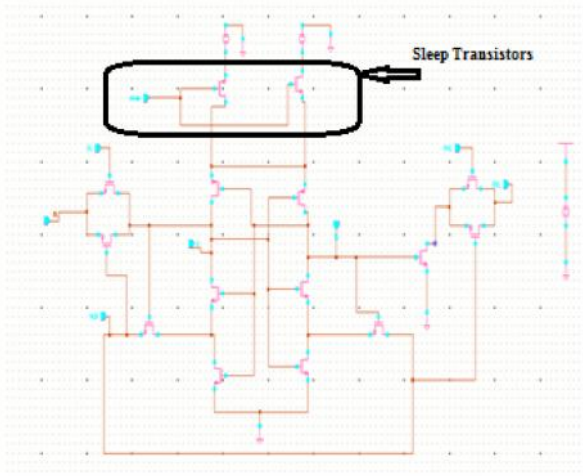

leakage power and performance metric based on SNM and power delay product will be considered for developing the proposed SRAM Cell schematic and Layout. The gate leakage current based power dissipation, multiple threshold voltage and effect of temperature on performance metric will be analyzed by making use of simulated model. The optimization of the designed SRAM Cell will also be carried out for low power low delay design.

Figure 3 shows schematic of the proposed ST13T SRAM cell. The ST13T Static-RAM cell consists of a cell core (cross-coupled ST inverter), a read path consists the two transistors, and a Write-Access (WA) transistor. The architectural change in the proposed schematic is the use of transmission gates in the access path. The transmission gate passes over the entire voltage range, i.e., strong '0' and strong '1' which improves the circuit performance. The write-access transistor is controlled by row-based Word Line (WL), and the read-access transistor is controlled by row-based Read Word Line (RWL). The feedback transistors of ST, MNFL, and MNFR are controlled by internal storage nodes Q and QB, respectively, with their drains connected with a control signal Wordline_bar (WLB) (inverted version of write enable signal).

The virtual ground (VGND) is row based, and WLB and BLs (BL and RBL) are column-based. The VGND signal can be easily shared over a row, if the memory is floor planned, such that all the cells of a word are adjacent to each other. However, for a bit-interleaved architecture, a hard-coding technique can be used to generate VGND signal for the cells of a selected word. The use of WLB and VGND control signals significantly mitigates the half-select disturb issue in the proposed cell. The main reasons of the leakage current in a CMOS design are-i) Reverse-biased junction leakage current, ii) Gate induced drain leakage, iii) Gate direct-tunnelling leakage, and iv) Sub threshold (weak inversion) leakage current.

The sub threshold leakage current is the most predominant of all the leakage current sources becomes very challenging for research in current and future silicon technologies. For the reduction of the leakage power in the SRAM Cell, the Sleep transistors power gating technique is used which minimizes the power dissipation during the data retention phase as shown in Figure 4. The Pull-up network is connected to reduced power supply (Vdd/2) during the data retention phase as the sleep signal is activated that thereby reduces the power dissipation of the circuit. The power gating techniques are used to reduce the power consumption of the circuit by reducing the power wastage during the

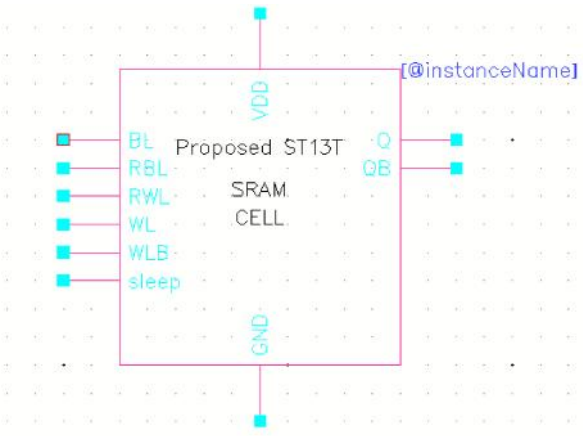
Figure 4: Proposed ST13T SRAM Cell Circuit with Power Gating Sleep Transistors




undesired phases of the circuit operation. In this paper, the sleep transistor technique is implemented for the power gating as shown in Figure 4.

The proposed ST13T SRAM Cell symbol is shown in Figure 5. The symbol can be used for the testing of the SRAM Circuit for proper working and the SRAM Cell Array is obtained by using the symbol for SRAM to avoid complexity.

Figure 5: Proposed ST13T SRAM Cell Circuit Symbol

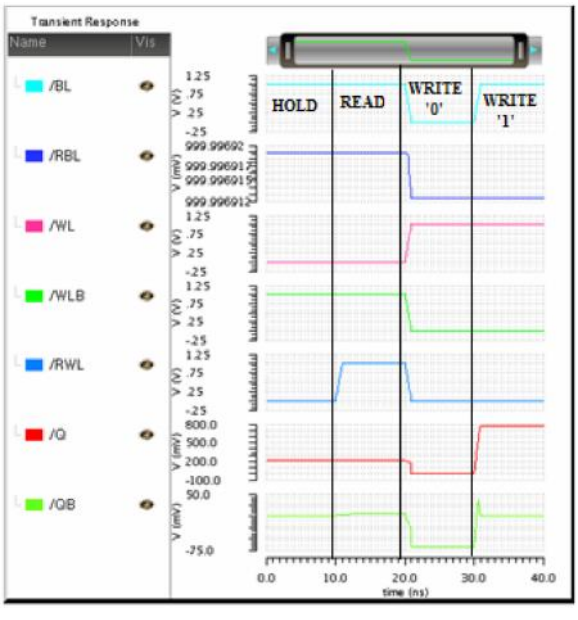



## PROPOSED ST13T SRAM CELL SIMULATION

Figure 6 shows timing diagrams for the control signals in different modes of operation of the proposed ST13T SRAM cell. During the hold mode, both Word Line (WL) and Read Word Line (RWL) are disabled and VGND is kept grounded. Therefore, the cross-coupled Schmitt Trigger inverter is isolated from both the Bit Lines (BLs), and the data-holding capability is increased due to the feedback mechanism. The four different cycles are represented in the fig. viz. HOLD, READ, WRITE '0', WRITE '1'.

In the read operation, Word Line (WL) is disabled, whereas Read Word Line (RWL) is enabled, which provides discharging path for Read Bit Line (RBL) through transistors MAR1 and MAR2 depending on the data stored at QB. The disabled Word Line (WL) makes data storage nodes (Q and QB) decoupled from

Figure 6: Proposed ST13T SRAM Cell Transient Analysis Waveforms



bitline (BL) during the read access. Due to this isolation, the RSNM is almost the same as the HSNM. Since the HSNM is very high in Schmitt-trigger based cell, read stability is remarkably improved.

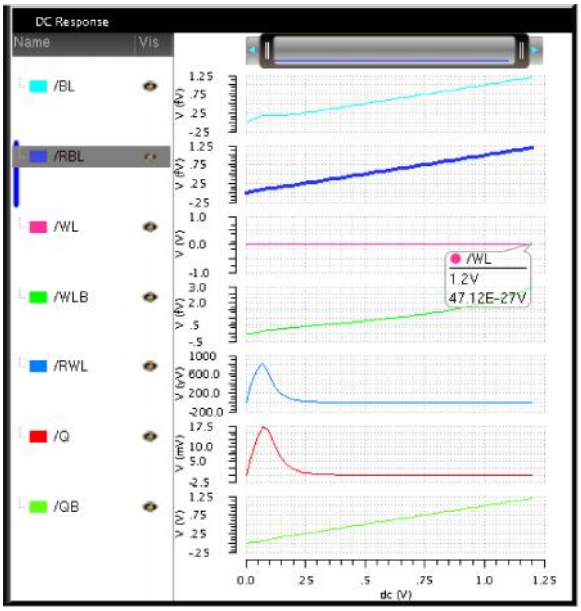
The VGND is again kept at ground, so that storage node may not get disturbed during read operation. It is to be noted that in both read and hold mode, WLB is at *V*dd (because write enable signal is disabled), which helps the feedback transistors MNFL and MNFR to provide a feedback mechanism and to exploit the feature of ST inverter to have a good inverter characteristic.

For writing data into the cell, WL is activated to transfer the data to storage node from BL, which is set/reset according to the data to be written. RWL is disabled, whereas the node VGND is kept floating. The floating VGND helps to overcome significantly write 1 problem of a single BL structure.

The WLB signal, which is inverted version of write enable signal, is disabled (i.e., WLB = 0 V) during the write operation. Consequently, there is no feedback action from any of the feedback transistors MNFL and MNFR as the voltage at nodes NL and NR does not rise. Subsequently, the writing speed is significantly increased.

The data retention phase is when the data bit is held in the cross-coupled inverter pair. During this phase the power requirement of the circuit is very less therefore, the SLEEP signal is activated during this phase for the leakage power reduction. This technique is known as the power gating technique. There are many possible choices for the power gating techniques but in this paper the sleep transistor technique is used.

Figure 7: Proposed ST13T SRAM Cell DC Analysis Waveforms




The dc analysis for the proposed ST13T SRAM Cell is shown in Figure 7. It is used to calculate the dc power consumption and the dc operating point calculation. The different phases of SRAM Cell operation, HOLD, READ, WRITE can be seen from the fig.

There are many leakage power reduction techniques based on various modes of operation of systems. The two operational modes are a) active mode and b) standby (or) idle mode. Most of the techniques aim at power reduction by shutting down the power supply to the system or circuit during standby mode.

The sleep transistors are turned ON during the active mode, in such a way that the normal operation is not affected as there exist a path between the supply and the ground rails. The sleep transistors are turned off in standby mode, thereby, shutting down the power supply to the circuit creating virtual supply and ground

rails. This technique is popularly known as SLEEP TRANSISTOR.

The Figures 8 and 9 gives the transient and dc analysis waveforms of the power gated ST13T SRAM Cell. As seen from the fig. that even after using the power gated sleep transistors, the SRAM cell is operation is same, i.e., the waveforms are nearly similar for both the circuits.

Figure 8: Proposed ST13T SRAM Cell with Power Gating Transient Analysis Waveforms

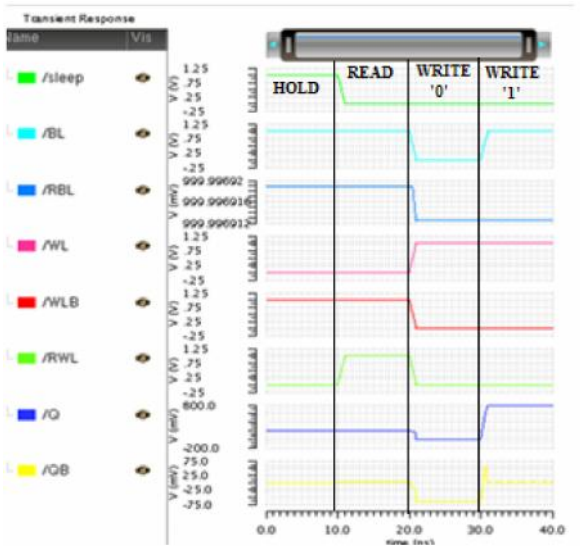



Figure 9: Proposed ST13T SRAM Cell with Power Gating DC Analysis Waveforms

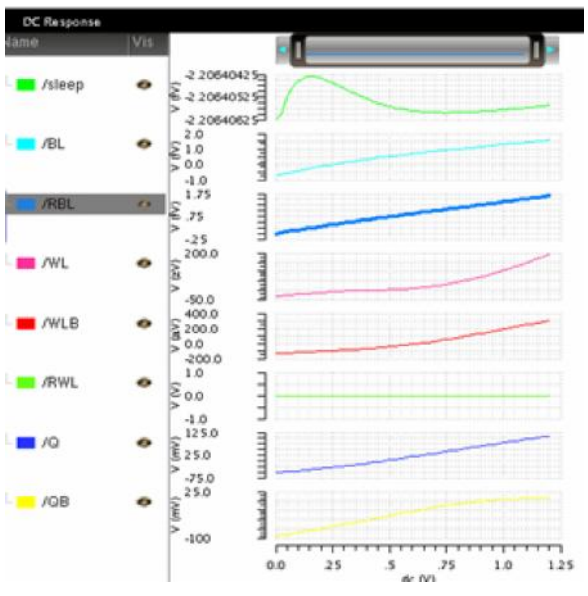



Figure 9 shows the dc analysis of the proposed SRAM Cell with power gating technique. The power is obtained using the dc analysis of the schematic outputs Q and QB.

The noise analysis is performed for the Proposed SRAM Cell and circuit with power gating technique and the noise voltage waveform is obtained as shown in the Figures 10-11. The noise summary is given later in this paper in result discussion section.

The area is also a important parameter while designing the VLSI circuit. In this circuit the numbers of transistors are increased as compared from the conventional 6T SRAM circuit but the performance is many times increased. The area overhead can be calculated from the cell Layout. When the

Figure 10: Proposed ST13T SRAM Cell Noise Response Waveforms

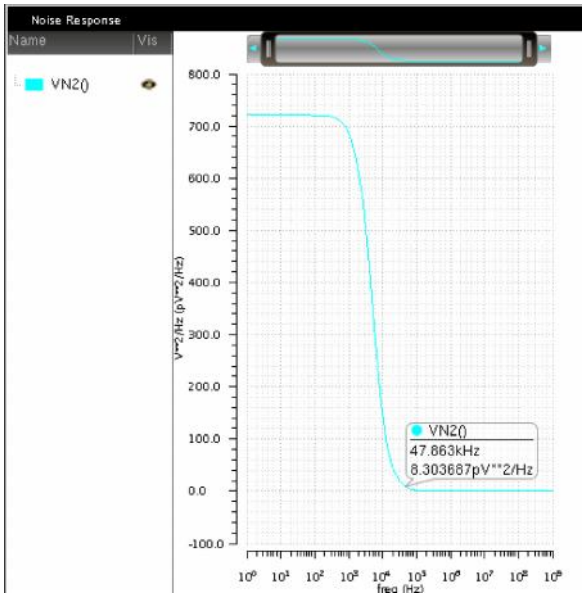
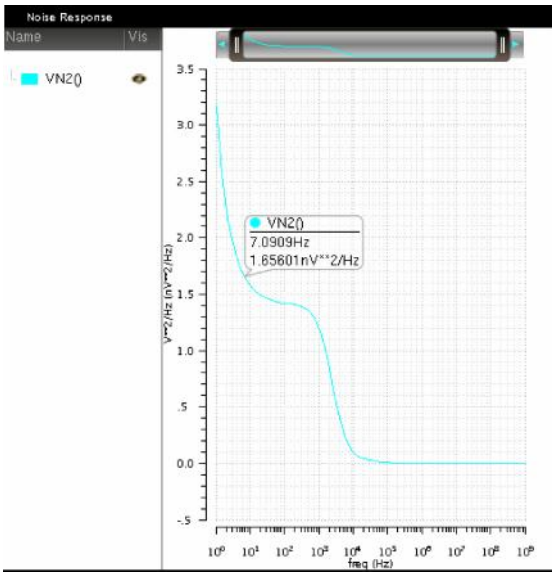


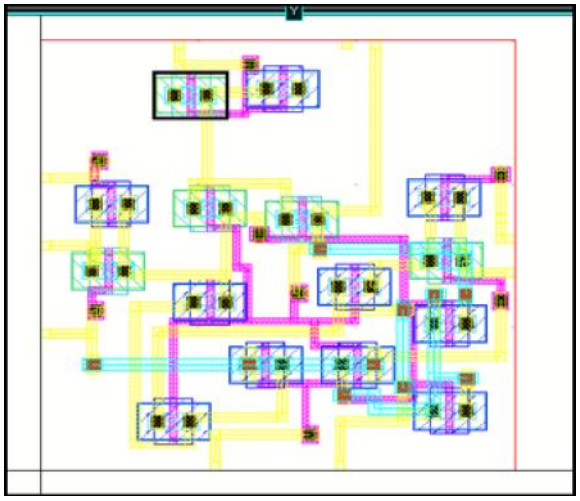
Figure 11: Proposed ST13T SRAM Cell with Power Gating Noise Response Waveforms




SRAM Cell array is formed the overall area overhead would be insignificant as compared to the performance improvement in the SRAM Cell design.

The autogenerated layout of the ST13T proposed SRAM Layout is shown in Figure 12.

Figure 12: Proposed ST13T SRAM Cell with Power Gating Layout



## RESULT ANALYSIS

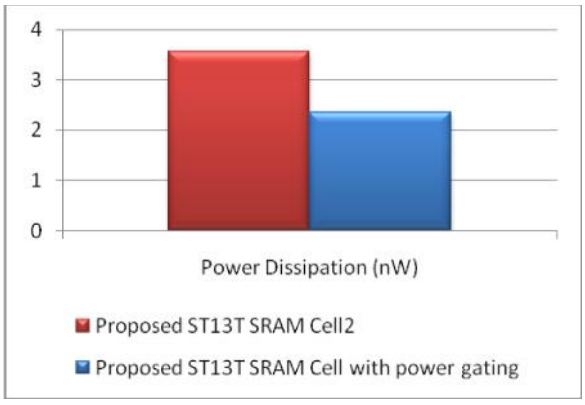
As seen from the transient and dc analysis of the proposed SRAM cell configuration that the proposed layout provides low power dissipation, Noise, Delay and Power-Delay Product values. Table 1 shows the performance analysis of the proposed ST13T SRAM Cell on the basis on Power dissipation, Noise analysis, Delay and the Power- Delay Product.

The Figure 13, shows the trend for the power dissipation for the designed ST13T SRAM Cell and then with the implementation of the power gating technique. As seen from the graph, the power dissipation is greatly reduced with the use of the sleep transistors. As during the data retention phase much power is not needed therefore the sleep transistor is activated during

Table 1: Proposed ST13T SRAM Cell Analysis

| Parameters | Proposed ST13T SRAM Cell | Proposed ST13T SRAM Cell with Power Gating |
|---|---|---|
| Power dissipation | 3.568nW | 2.367 nW |
| Noise | 8.68392e^-10 | 1.2115e^-09 |
| Delay | 10.80ns | 9.8ns |
| PDP | $38.534 X 10^{-18} J$ | $11.872 X 10^{-18} J$ |

Figure 13: Trend for Power Dissipation



this phase. The 33.66% power reduction is achieved with the use of sleep transistors.

Figure 14 shows the trend for the noise analysis for bothe the configurations of the SRAM Cell. As observed from the graph that the noise is also reduced by the use of the power gating technique. The 62.18% noise reduction is achieved by the use of the power gated sleep transistors.

The Figure 15 shows the trend for the delay for the ST13T and with the use of the power gated sleep transistors. The delay has to be reduced for the high speed memory design.

Figure 14: Trend for Noise Analysis

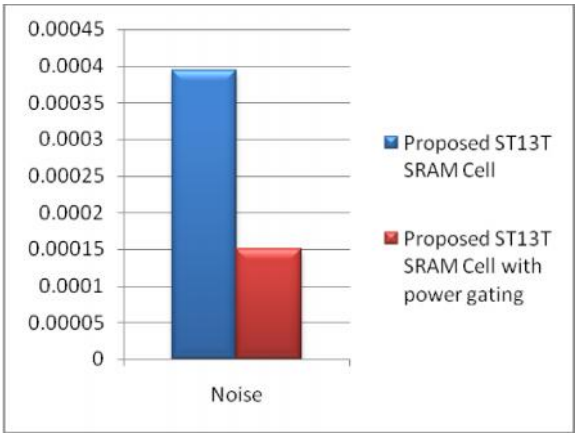
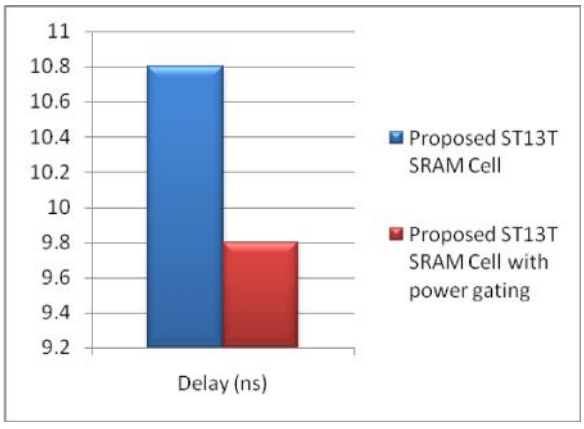



Figure 15: Trend for Delay




The delay is reduced for the power gated configuration to a small extent but as compared from the conventional SRAM circuit the delay is reduced considerably. The 10.20% delay reduction is obtained by the use of power gating configuration.

The power delay product trend is shown in the Figure 16, there exist a trade-off between the power delay product and it is expected that it should be reduced for the high performance of the circuit. The 38.14% reduction is obtained in the power delay product by the use of power gating technique.

As observed from the table, the proposed circuit gives the good results with use of the transmission gates in the access path of the SRAM Cell and the power gating technique, i.e., the use of the sleep transistors. The use

Figure 16: Trend for Power Delay Product

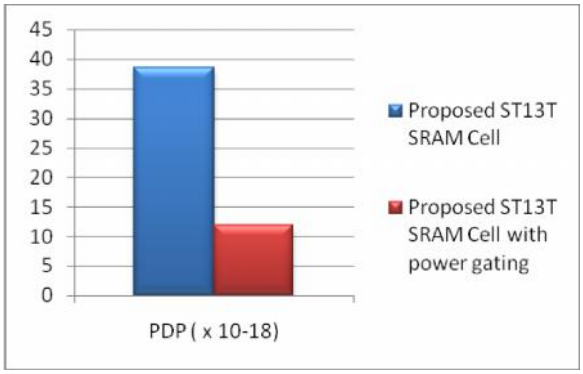



Table 2: Results Analysis for the Proposed Design

| Parameters | % Reduction in ST 13T with Power Gating Technique |
|---|---|
| Power dissipation | 0.3366 |
| Noise | 0.6218 |
| Delay | 0.102 |
| PDP | 0.3814 |

of the power gating technique greatly reduces the total power dissipation as during the data retention mode the sleep input is activated, thereby, saving the power flowing through the circuit as the pull-up network is connected to the VDD/2 supply input. Hence, this proposed circuit gives the satisfactory read write cycles and also saves the power dissipation during the standby condition and therefore, the SNR improves for the ST13T SRAM Cell.

As observed from the Table 2, the proposed circuit gives the good results with use of the transmission gates in the access path of the SRAM Cell and the power gating technique, i.e., the use of the sleep transistors. The use of the power gating technique greatly reduces the total power dissipation as during the data retention mode the sleep input is activated, thereby, saving the power flowing through the circuit as the pull-up network is connected to the VDD/2 supply input. Hence, this proposed circuit gives the satisfactory read write cycles and also saves the power dissipation during the standby condition and therefore, the SNR improves for the ST13T SRAM Cell.

Figure 17: Performance Improvement Trend of the Proposed Circuit

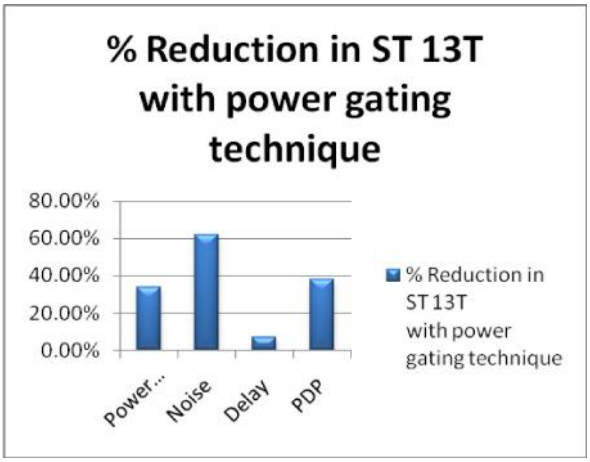



Figure 17 shows the trend of the percentage reduction in the various performance parameters viz. power, noise, delay, PDP. As seen from the fig. that the proposed circuit ST13T SRAM Cell with power gating techniques provides good results.

## CONCLUSION

This paper includes the design of Static-RAM cell. Performance analysis of the proposed ST13T SRAM Cell is done in this paper. The leakage power dissipation has become one of the most challenging issues in low power VLSI circuit designs especially with on-chip devices as it doubles for every two years. The scaling down of threshold voltage has contributed enormously towards increase in sub threshold leakage current thereby making the static (leakage) power dissipation very high. The proposed design aims at the power reduction and SNR improvement for the Static-RAM cell configurations. From the result it is clear that optimized proposed ST13T Static-RAM Cell is more power efficient with the use of power gating technique, i.e., Sleep transistors approach. During active mode the sleep transistors are turned ON, so that the normal operation is not affected as there is a path between the supply and the ground. In standby mode the sleep transistors are turned off thereby shutting down the power supply to the circuit creating virtual supply and ground rails.

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