International Journal of Electrical and Electronic Engineering & Telecommunications

ISSN 2319 – 2518 www.ijeetc.com
Vol. 5, No. 3, July 2016

Research Paper

DESIGN OF CMOS RING VCO FOR PLL BASED FREQUENCY SYNTHESIZER

Poonam Sachdeva[1]* and Ankita Aggarwal[2]

*Corresponding Author: Poonam Sachdeva, ✉ mspoonamsachdeva@rediffmail.com

The voltage controlled oscillator is one of the most important building block of the PLL based frequency synthesizer. This paper presents two design of three stage CMOS Ring VCO for PLL based Frequency Synthesizer. Ring VCO simply consists of cascaded inverters. The performance comparison is done in terms of output frequency, power dissipation and supply voltage for two different technologies. First design comprises of three stage ring VCO designed in 18 µm CMOS technology and achieves a high frequency of 5.2 GHz with a power dissipation of 152 µW under the supply voltage of 1.8 V. In the second design, a three stage ring VCO is designed in 90 nm CMOS technology and achieves a frequency of 32 GHz with a power dissipation of 132 W under the supply voltage of 1.2 V.

Keywords: VCO, Ring oscillator, CMOS, PLL, Inverter, Power dissipation, Time delay, Frequency

INTRODUCTION

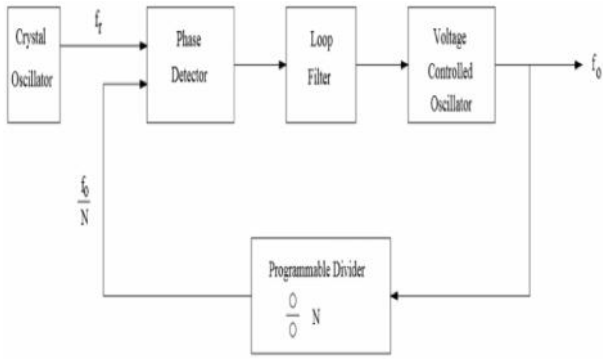
A frequency synthesizer is a circuit design that generates a new frequency from a single stable reference frequency. A crystal oscillator is often used for the reference frequency. The main objective of frequency synthesizer is to recover the signal without phase and frequency error and this process is completed after many iterations inside the system. The fundamental functional blocks of any frequency synthesizer in general are

- Phase Frequency Detector (PFD)
- Charge Pump (CP)
- Low Pass Filer (LPF)
- Voltage Controlled Oscillator (VCO)
- Loop Divider

The block diagram for Frequency Synthesizer is shown in Figure 1. The basic Phase Locked Loop (PLL) consists of a phase detector, charge pump, low pass filter and a voltage controlled oscillator. The phase detector compares the phase of an incoming reference signal with that of the VCO, and produces an output that is some function of the phase difference. The output PFD consists of a dc component superimposed with an ac

[1] M.Tech Student, Galaxy Global Group of Institute, Dinarpur, Ambala, Haryana, India.
[2] Asst. Prof. & HOD, Galaxy Global Group of Institute, Dinarpur, Ambala, Haryana, India.

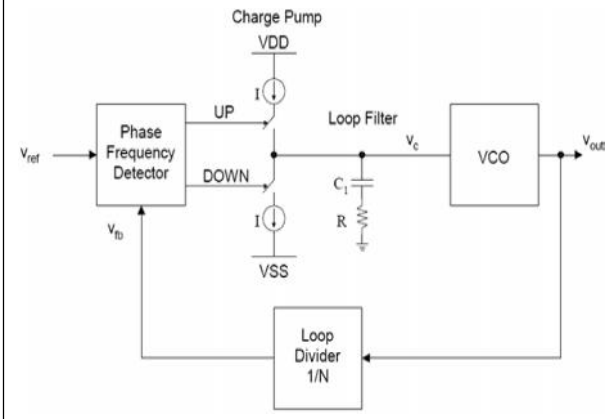
Figure 1: Frequency Synthesizer Block Diagram



component. The ac part is undesired as an input to the VCO, hence low pass filter is used to filter out the ac component. The VCO generates a signal whose frequency is some function of the control voltage. It is a negative feedback system as the output of the phase detector drives the VCO frequency in a direction that reduces the phase difference. Two widely used VCO's types are CMOS ring and LC tank based circuits. The on chip combination of inductor and capacitor consumes large layout area in LC tank based oscillators (Craninckx and Steyaert, 1995; Catli and Haskell, 2008; and Lee and Hsieh, 2008). CMOS based ring inverter oscillators have advantages over other oscillators design due to ease of controlling the tuning range and no requirement for on chip inductors (Paula *et al.*, 2008; and Cao *et al.*, 2008). CMOS based ring oscillators have a wide tuning range and are easier to integrate in CMOS process. Different types of ring VCO's have been reported using different types of delay cells including multiple feedback loops, single ended delay cells and dual delay paths (Jeong *et al.*, 1997; Lee *et al.*, 1997; Park and Kim, 1999; Eken and Uyemura, 2004; and Kim *et al.*, 2004). Voltage controlled ring oscillators consists of series of delay stages, which are more important in comparison to other monolithic oscillators (Shrivastava *et al.*, 2013). On the performance point of view, ring oscillators have provided better result than relaxation oscillators, but not as that of sinusoidal oscillators (Shrivastava *et al.*, 2013). Multi stage ring oscillator provide less oscillation frequency range and high level of phase noise. To improve the oscillation frequency, the delay elements should be reduced. So to overcome these problem a three stage voltage controlled ring oscillator is presented. The main objective of this paper is to enhance the performance (delay, oscillation frequency, power dissipation) of ring VCO using different CMOS technology and provide a comparison between them.

Figure 2 shows the integration of PFD, CP and loop filter. As shown in Figure 2, the reference input is given to the one of the input of PFD while VCO output is given to another input. This implementation senses the transition at the input and output detects phase or frequency difference and activates the charge pump accordingly**.**

Figure 2: Simple Charge Pump PLL



Source: Razavi (2000)

FREQUENCY SYNTHESIZER ARCHITECTURE

The description of various blocks of Frequency Synthesizer are as follows:

Phase Frequency Detector

It consists of two edge triggered D flip flops with their D inputs tied together to logical one. Inputs A and B serve as clock of flip flops. If $Q_A = Q_B = 0$ and A goes high, Q_A rises. If this event is followed by a rising transition on B, Q_B also goes high and the AND gate resets both flip flops. In other words, Q_A and Q_B are simultaneously high for a short time but the difference between their average values still represents the input phase or frequency difference correctly.

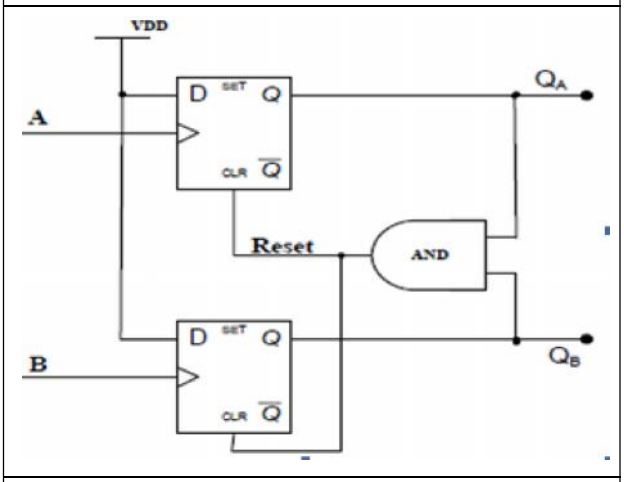
The Charge Pump

A charge pump is a three position electronic device switch which is controlled by the three states of a PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm V_P$ or a pump current $\pm I_P$ to the loop filter. When both UP and DOWN of PFD are off, the switch is open thus isolating the loop filter from the charge pump and PFD. The current sources I_{up} and I_{dn} are identical. Two outputs of PFD are given to the UP and DOWN inputs of charge pump respectively. If $Q_A = Q_B = 0$, then S1 and S2 are off and V_{out} or V_{cont} remains constant. If Q_A is high and Q_B is low, then I_{up} charges Cp. Conversely if Q_A is low and if Q_B is high, then I_{dn} discharges Cp.

Loop Filter

The output of PFD consists of dc component superimposed with an ac component. The ac part is undesired as an input to VCO. Hence low pass filter is used to filter out ac component. Both passive filter and active filter can be used

Figure 3: Phase Frequency Detector



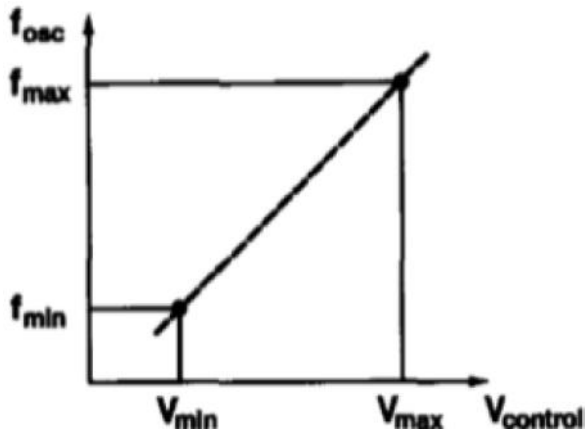
Source: Young et al. (1992)

but a passive filter is usually preferred than an active filter because an active filter results in higher complexity, cost and noise.

VCO

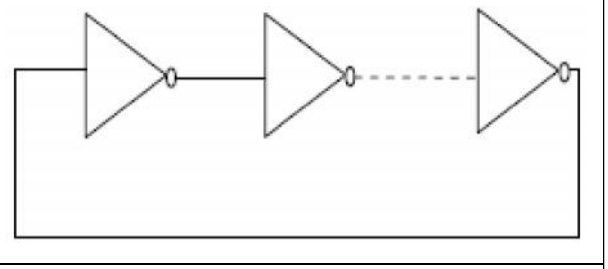
A VCO is a voltage controlled oscillator whose output frequency is linearly proportional to the control voltage generated by the PFD and Loop Filter. There are two methods which are used to design CMOS VCOs – by the use of Ring oscillator and by the use of Schmitt Trigger. Here the Ring Oscillator technique has been used. Ring oscillator is a closed-loop cascade connection of any odd number of inverters where the output node of the last inverter is connected to the input node of the first inverter. Thus the circuit forms a voltage feedback loop. When choosing a VCO circuit approach it is important to consider the control voltage versus frequency (V-f) characteristic. A linear characteristic will minimize the VCO sensitivity (i.e., characteristic slope) variation as a function of control voltage or operating frequency, providing PLL stability over the widest possible frequency range. Also, it is desirable for the V-f characteristic to have a

Figure 4: Oscillator Frequency verses Control Voltage



Source: Young et al. (1992)

Figure 5: Block Diagram of Single Ended Ring VCO



Source: Kumar et al. (2012)

positive slope as shown in Figure 5. This means that the maximum operating frequency is achieved at maximum control voltage, which is only limited by the maximum VCC applied (Young *et al.*, 1992).

PROPOSED WORK

In this work a three stage CMOS Ring VCO for PLL based Frequency Synthesizer has been designed. A single ended inverter based ring VCO block diagram is shown in figure 6. For oscillation occurrence, the ring must provide a phase shift of 2π and should have unity voltage gain. Each delay stage should provide a phase shift of π/N where N is number of delay stages. The remaining π phase shift is provided by dc inversion. Single ended oscillator requires odd number of stages for dc inversion.

Assuming the inverters are identical, the oscillation frequency is given as follow

$$f_{osc} = 1/(2*n*(t_{phl} + t_{plh})) \quad ...(1)$$

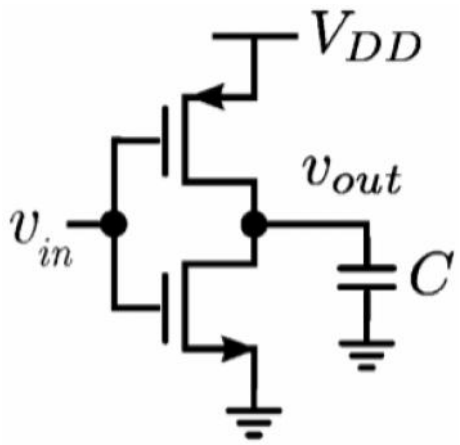
where n is the number of inverters in the ring oscillator and $(t_{phl} + t_{plh})$ is the propagation delay of each inverter. The propagation delay times t_{phl} and t_{plh} determine the input-to-output signal delay during to high-to-low and low-to-high transitions of output respectively (Kang and Leblebici, 2003).

$$t_{phl} = (C_{load}/k_n(V_{dd}-V_{tn}))*[(2*V_{tn})/(V_{dd}-V_{tn}) + \ln((4(V_{dd}-V_{tn})/V_{dd})-1)] \quad ...(2)$$

$$t_{plh} = (C_{load}/k_p(V_{dd}-V_{tp}))*[(2*V_{tp})/(V_{dd}-V_{tp}) + \ln((4(V_{dd}-V_{tp})/V_{dd})-1)] \quad ...(3)$$

The first stage CMOS inverter of ring VCO with the single lumped output load capacitance is shown in Figure 6. When the input voltage switches from low to high, the PMOS transistor in the circuit is turned off and the NMOS transistor starts conducting. During this phase, the output load capacitance is being discharged through the NMOS transistor. Thus the capacitor current equals the instantaneous drain current of the NMOS transistor. When the input voltage switches from high to low, the NMOS transistor in the circuit is turned off and the PMOS transistor starts conducting. During this phase, the output load capacitance is being charged up through the PMOS transistor therefore the capacitor current equals the instantaneous drain current of the PMOS transistor (Kang and Leblebici, 2003).

Figure 6: CMOS Inverter Driving a Capacitor Load as in a Ring VCO



Source: Abidi (2006)

The output load capacitance is given as follows (Kang and Leblebici, 2003).

$$C_L = C_{gdn} + C_{gdp} + C_{dbn} + C_{dbp} + C_{int} + C_g \quad ...(4)$$

where C_L is the Load Capacitance

C_{db} is the drain substrate junction capacitance and is given by

$$C_{db} = A*C_{j0}*K_{eq} + P*C_{jsw}*K_{eq(sw)} \quad ...(5)$$

$$C_{jsw} = C_{j0sw} * x_j \quad ...(6)$$

$$C_{j0} = (\varepsilon_{si}*q/2((N_A*N_D)/N_A+N_D)*1/\varphi_0)^{1/2}$$

$$C_{j0sw} = \varepsilon_{si}*q/2((N_{A(sw)}*N_D)/N_{A(sw)}+N_D)*1/\varphi_{0sw})^{1/2}$$

where

N_A = Substrate Doping ($2*10^{-15}$ cm^{-3})

N_D = Source/Drain (10^{19} cm^{-3})

$N_A(sw) = 4*10^{16}$ cm^{-3}

$\varphi_0 = 0.837$ V

$\varphi_{0SW} = 0.915$ V

where C_{j0} is the zero bias junction capacitance per unit area ($1.4*10^{-8}$ F/cm^2 and C_{jsw} is the zero bias side wall junction capacitance per unit length. K_{eq} is the voltage equivalence factor ($0 < K_{eq} < 1$) (Kang and Leblebici, 2003).

Here value of x_j is taken as $3.9*10^{-8}$ cm in 180nm technology and $2.8*10^{-6}$ cm in 90 nm technology. $C_{j0sw} = 6*10^{-6}$ F/cm. A is the junction bottom area and P is the junction sidewall parameter (Geiger *et al.*, 1990).

C_{gd} is gate to drain capacitance. It is actually the gate to channel capacitance seen between the gate and the drain terminals (Geiger *et al.*, 1990).

$$C_{gd} = C_{ox}*W*L_D \quad ...(7)$$

where L_D is the lateral diffusion of the source or drain under the gate. The value of L_D is taken as 0.05 μm.

The gate oxide capacitance is defined by (Geiger *et al.*, 1990)

$$C_g = W*L*C_{ox} \quad ...(8)$$

The gate oxide capacitance per unit area is given by

$$C_{ox} = \varepsilon_{ox}/t_{ox} \quad ...(9)$$

where $\varepsilon_{ox} = 3.45*10^{-11}$ F/m and is called the permittivity of the silicon oxide.

t_{ox} is called the oxide thickness. The oxide thickness is determined by the process technology used to fabricate the MOSFET. The value of t_{ox} is 4nm in 180 nm technology and 2.4 nm in 90 nm technology.

The logic threshold voltage of the CMOS inverter is given as (Kang and Leblebici, 2003)

$$V_{th} = V_{To,n} + (1/k_R)^{1/2}(V_{dd}+V_{To,p})/(1+(1/k_R)^{1/2}) \quad ...(10)$$

where ratio k_R is given by

$$k_R = (\mu_n C_{ox}(W_n/L_n))/\mu_p C_{ox}(W_p/L_p) \quad ...(11)$$

Usually the channel lengths L_n and L_p are usually fixed and equal to each other (Kang and Leblebici, 2003). The transistor aspect ratio (Kang and Leblebici, 2003) is defined as

$$R(aspectratio) = W_p/W_n \quad ...(12)$$

Average power dissipation of the CMOS inverter is

$$P_{avg} = C_{load} * V_{dd}^2 * f \quad ...(13)$$

RESULTS AND DISCUSSION

In the tabulation the performance comparison of three stage Ring VCO in terms of frequency, power dissipation and supply voltage in 180 nm technology and 90 nm CMOS technology.

Table 1: Results for Three Stage CMOS Ring VCO in Different Technology

Parameters	180 nm	90 nm
Power Supply Voltage (V)	1.8	1.2
Frequency Range (GHz)	5.2	32
Power Dissipation (μw)	152	132
No. of stages	3	3
Time delay (ps)	32.2	5.28

CONCLUSION

In this paper the design of three stage ring VCO for PLL based frequency synthesizer has been proposed. The output frequency comes out to be 5.2 GHz in case of three stage ring VCO designed in 180 nm technology with power dissipation of 152 μw. In the design of 3 stage ring VCO designed in 90 nm technology, the output frequency comes out to be 32 GHz with power dissipation of 132 μw.

REFERENCES

1. Abidi A A (2006), "Phase Noise and Jitter in CMOS Ring Oscillators", *IEEE Journal of Solid State Circuits*, Vol. 41, No. 8.
2. Cao T, Wisland D T, Lande T S and Moradi F (2008), "Low-Voltage, Low-Power, and Wide-Tuning Range VCO for Frequency Modulator", IEEE Conference NORCHIP.
3. Catli B and Haskell M M (2008), "A 0.5 V 3.6/5.2 GHz CMOS Multi-Band VCO for Ultra Low-Voltage Wireless Applications", *IEEE International Symposium on Circuits and Systems*.
4. Craninckx J and Steyaert M S J (1995), "A 1.8 Ghz CMOS Low-Phase-Noise Voltage-Controlled Oscillator with Prescaler", *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 12.
5. Eken Y A and Uyemura J P (2004), "A 5.9 GHz Voltage Controlled Ring Oscillator in 0.18 m CMOS", *IEEE Journal of Solid State Circuits*, Vol. 39, No. 1.
6. Geiger R L, Allen P E and Strader N (1990), "VLSI Design Techniques for Analog and Digital Circuits", Mc Grall Hill, New York.
7. Jeong D Y, Chai S H, Song W C and Cho G H (1997), "CMOS Current Controlled Oscillators Using Multiple-Feedback Loop Ring Architectures", IEEE International Solid-State Circuits Conference.
8. Kang S M and Leblebici Y (2003), "CMOS Digital Integrated Circuits: Analysis and Design", 3rd Edition, Tata McGraw Hill Publication.
9. Kim H R, Cha C Y, Min Oh S, Yang M S and Lee S G (2004), "A Very Low-Power Quadrature VCO with Back-Gate

Coupling", *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 6.

10. Kinger B, Suman S, Sharma K G and Ghosh P K (2015), "Design of Improved Performance Voltage Controlled Ring Oscillator", Fifth IEEE International Conference on Advanced Computing and Communication Technologies.
11. Kumar M, Arya S K and Pandey S (2012), "A Low Power Voltage Controlled Ring Oscillator Design with Substrate Biasing", *International Journal of Information and Electronics Engineering*, Vol. 2, No. 2.
12. Lee S J, Kim B and Lee K (1997), "A Novel High-Speed Ring Oscillator for Multiphase Clock Generation Using Negative Skewed-Delays Scheme", *IEEE J. Solid-State Circuits*, Vol. 32.
13. Lee S Y and Hsieh J Y (2008), "Analysis and Implementation of a 0.9 V Voltage-Controlled Oscillator with Low Phase Noise and Low Power Dissipation", *IEEE Transaction on Circuits and Systems II*, Vol. 55, No. 7.
14. Park C H and Kim B (1999), "A Low-Noise, 900 MHz VCO in 0.6 m CMOS", *IEEE J. Solid-State Circuits*, Vol. 34.
15. Paula L S, Banpi S, Fabris E and Susin A A (2008), "A Wide Band CMOS Differential Voltage-Controlled Ring Oscillators", *International IEEE Northeast Workshop on Circuits and System Design*.
16. Razavi B (2000), "Design of Analog CMOS Integrated Circuits", Edition, Tata McGraw-Hill.
17. Sedra A S and Smith K C (1998), "Microelectronic Circuits", Oxford University Press, New York.
18. Shrivastava A, Khandelwal S and Akashe S (2013), "Performance Evaluation of Five Stage VCO Ring Oscillator with Reverse Substrate Bias and SAL Technique Using Nanoscale CMOS Technology", 3rd IEEE International Conference on Advanced Computing and Communication Technologies.
19. Young I A, Greason J K and Wong K L (1992), "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors", *IEEE Journal of Solid State Circuits*, Vol. 27, No. 11.