

Research Paper

A POWER QUALITY IMPROVEMENT BY USING MC-UPQC

K Laxmi Priyanka^{1*} and P Prasanna Lakshmi²

*Corresponding Author: K Laxmi Priyanka, ✉ Laxmi.priyanka.k@gmail.com

This paper presents a new unified power-quality conditioning system (MC-UPQC), capable of simultaneous compensation for voltage and current in multibus/multifeeder systems. The series inverter of UPQC is controlled to perform simultaneous 1) voltage sag/swell compensation, and 2) load reactive power sharing with the shunt inverter. The active power control approach is used to compensate voltage sag/swell and is integrated with theory of Power Angle Control (PAC) of UPQC to coordinate the load reactive power between the two inverters. Since the series inverter simultaneously delivers active and reactive powers, this concept is named as UPQC. Therefore, power can be transferred from one feeder to adjacent feeders to compensate for sag/swell and interruption. The performance of the MC-UPQC as well as the adopted control algorithm is illustrated by simulation. The results obtained in MATLAB on a two-bus/two-feeder system show the effectiveness of the proposed configuration.

Keywords: Power Quality (PQ), MATLAB, Unified Power-Quality Conditioner (UPQC), Voltage-Source Converter (VSC)

INTRODUCTION

With increasing applications of nonlinear and electronically switched devices in distribution systems and industries, Power-Quality (PQ) problems, such as harmonics, flicker, and imbalance have become serious concerns. In addition, lightning strikes on transmission lines, switching of capacitor banks, and various network faults can also cause PQ problems, such as transients, voltage sag/swell, and interruption. On the other hand, an increase of

sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation (Sabin and Sundaram, 1996).

In order to meet PQ standard limits, it may be necessary to include some sort of compensation. Modern solutions can be found in the form of active rectification or active filtering (Rastogi *et al.*, 1994). A shunt active power filter is suitable for the suppression of negative load influence on the supply network,

¹ Student, Narasaraopeta Engineering College, Narasaraopet, Andhra Pradesh 522 601, India.

² Assistant Professor, Narasaraopeta Engineering College, Narasaraopet, Andhra Pradesh 522 601, India.

but if there are supply voltage imperfections, a series active power filter may be needed to provide full compensation (Peng, 1998).

In recent years, solutions based on flexible ac transmission systems (FACTS) have appeared. The application of FACTS concepts in distribution systems has resulted in a new generation of compensating devices. A Unified Power-Quality Conditioner (UPQC) (Akagi, 1996) is the extension of the Unified Power-Flow Controller (UPFC) (Gyugyi *et al.*, 1995) concept at the distribution level. It consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfections in a supply feeder (Fujita and Akagi, 1998; Aredes *et al.*, 1998; and Ghosh and Ledwich, 2001). Recently, multiconverter FACTS devices, such as an Interline Power-Flow Controller (IPFC) (Gyugyi *et al.*, 1999) and the Generalized Unified Power-Flow Controller (GUPFC) (Fardanesh *et al.*, 2000) are introduced. The aim of these devices is to control the power flow of multilines or a subnetwork rather than control the power flow of a single line by, for instance, a UPFC.

When the power flows of two lines starting in one substation need to be controlled, an Interline Power-Flow Controller (IPFC) can be used. An IPFC consists of two series VSCs whose dc capacitors are coupled. This allows active power to circulate between the VSCs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization.

The GUPFC combines three or more shunt and series converters. It extends the concept of voltage and power-flow control beyond what is achievable with the known two-converter

UPFC. The simplest GUPFC consists of three converters—one connected in shunt and the other two in series with two trans-mission lines in a substation. The basic GUPFC can control total five power system quantities, such as a bus voltage and independent active and reactive power flows of two lines. The concept of GUPFC can be extended for more lines if necessary. The device may be installed in some central substations to manage power flows of multilines or a group of lines and provide voltage support as well. By using GUPFC devices, the transfer capability of transmission lines can be increased significantly. Furthermore, by using the multiline-management capability of the GUPFC, active power flow on lines cannot only be increased, but also be decreased with respect to operating and market transaction requirements. In general, the GUPFC can be used to increase the transfer capability and relieve congestions in a flexible way.

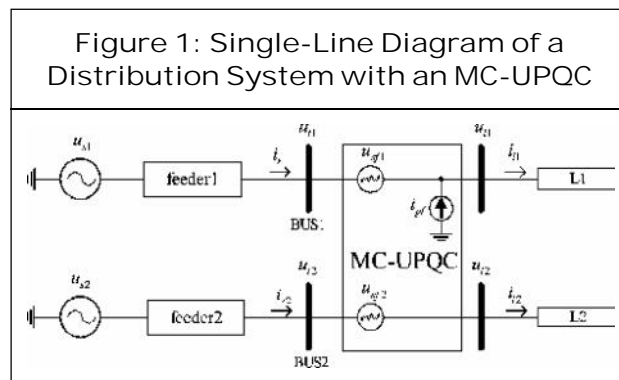
This concept can be extended to design multiconverter configurations for PQ improvement in adjacent feeders. For example, the interline unified power-quality conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in Jindal *et al.* (2007). The IUPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. In this paper, a new configuration of a UPQC called the multiconverter unified power-quality conditioner (MC-UPQC) is presented. The system is extended by adding a series-VSC in an adjacent feeder. The proposed topology

can be used for si-multaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations.

PROPOSED MC-UPQC SYSTEM

Circuit Configuration

The single-line diagram of a distribution system with an MC-UPQC is shown in Figure 1.



As shown in this figure, two feeders connected to two different substations supply the loads L1 and L2. The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of u_{t1} and u_{t2} , respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of i_{t1} . Supply voltages are denoted by u_{s1} and u_{s2} while load voltages are u_{l1} and u_{l2} finally, feeder currents are denoted by i_{s1} and i_{s2} load currents are i_{l1} and i_{l2} .

Bus voltages are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is nonsinusoidal and contains harmonics. The load L2 is a sensitive/critical

load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell, and in-terruption. These types of loads primarily include production in-dustries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe economical losses or human damages.

MC-UPQC Structure

The internal structure of the MC-UPQC is shown in Figure 3. It consists of three VSCs (VSC1, VSC2, and VSC3) which are connected back to back through a common dc-link capacitor. In the proposed configuration, VSC1 is connected in series with BUS1 and VSC2 is connected in parallel with load L1 at the end of Feeder1. VSC3 is connected in series with BUS2 at the Feeder2 end.

Figure 2: Schematic Structure of a VSC

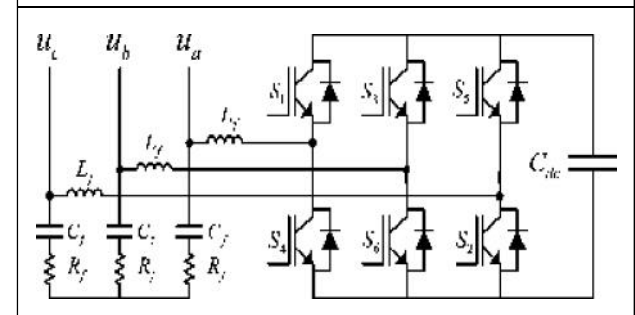
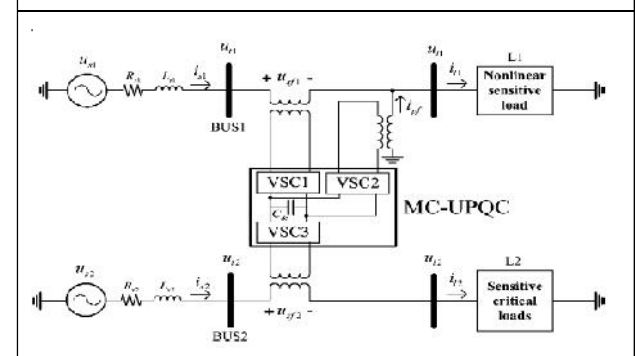


Figure 3: Typical MC-UPQC Used in Distribution System



Each of the three VSCs in Figure 3 is realized by a three-phase converter with a commutation reactor and high-pass output filter as shown in Figure 2. The commutation reactor and high-pass output filter are connected to prevent the flow of switching harmonics into the power supply.

As shown in Figure 3, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1. The aims of the MC-UPQC shown in Figure 2 are:

- To regulate the load voltage against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L1;
- To regulate the load voltage against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2;
- To compensate for the reactive and harmonic components of nonlinear load current.

In order to achieve these goals, series VSCs (i.e., VSC1 and VSC3) operate as voltage controllers while the shunt VSC (i.e., VSC2) operates as a current controller.

Control Strategy

As shown in Figure 4, the MC-UPQC consists of two series VSCs and one shunt VSC which are controlled independently. The switching control strategy for series VSCs and the shunt VSC are selected to be Sinusoidal Pulse

Width-Modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the – method (Hu and Chen, 2000), will be discussed later.

Shunt-VSC: Functions of the shunt-VSC are:

- To compensate for the reactive component of load L1 current;
- To compensate for the harmonic components of load L1 current;
- To regulate the voltage of the common dc-link capacitor.

Figure 5 shows the control block diagram for the shunt VSC. The measured load current is transformed into the synchronous reference frame by using.

Figure 4: Control Block Diagram of the Shunt VSC

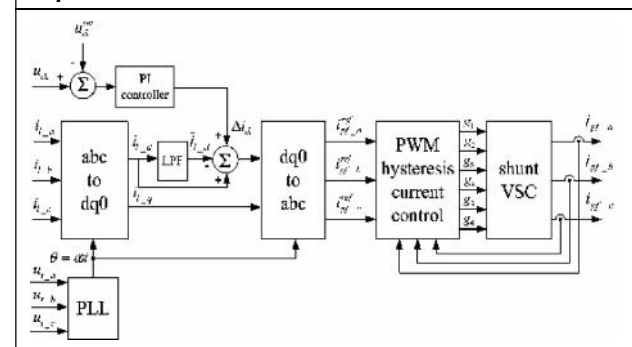
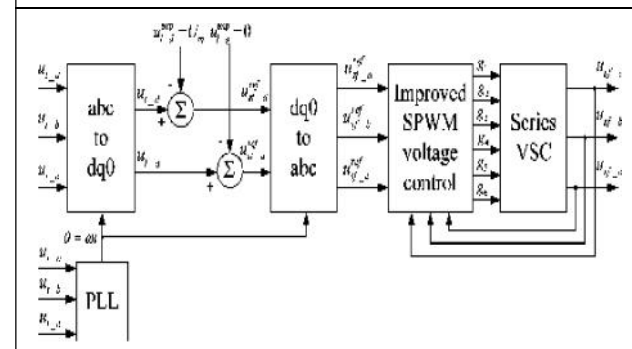


Figure 5: Control Block Diagram of the Series VSC



$$i_{L-dq0} = T_{abc}^{dq0} i_{L-abc} \quad \dots(1)$$

$$T_{abc}^{dq0} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120^\circ) & \cos(\omega t + 120^\circ) \\ -\sin(\omega t) & -\sin(\omega t - 120^\circ) & -\sin(\omega t + 120^\circ) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad \dots(2)$$

where the transformation matrix is shown in (2), at the bottom of the page.

By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the d and q axes, can be easily extracted by Low-Pass Filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift

$$i_{L-d} = \bar{i}_{L-d} + \tilde{i}_{L-d} \quad \dots(3)$$

$$i_{L-q} = \bar{i}_{L-q} + \tilde{i}_{L-q} \quad \dots(4)$$

where i_{L-d}, i_{L-q} are d-q components of load current, $\bar{i}_{L-d}, \bar{i}_{L-q}$ are dc components, and $\tilde{i}_{L-d}, \tilde{i}_{L-q}$ are the ac components of i_{L-d} and i_{L-q} .

If i_{L-d} is the feeder current and i_{L-q} is the shunt VSC current and knowing then – components of the VSC reference current are defined as follows:

$$i_{pf-d}^{\text{ref}} = \tilde{i}_{L-d} \quad \dots(5)$$

$$i_{pf-q}^{\text{ref}} = \tilde{i}_{L-q} \quad \dots(6)$$

consequently the d-q components of feeder currents are

$$i_{s-d} = \bar{i}_{L-d} \quad \dots(7)$$

$$i_{s-q} = 0 \quad \dots(8)$$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect

the dc link. In order to regulate the dc-link capacitor voltage, a Proportional-Integral (PI) controller is used as shown in Figure 5. The input of the PI controller is the error between the actual capacitor voltage and its reference value. The output of the PI controller is added to the component of the shunt-VSC reference current to form a new reference current as follows:

$$\begin{cases} i_{pf-d}^{\text{ref}} = \tilde{i}_{L-d} + \Delta i_{dc} \\ i_{pf-q}^{\text{ref}} = \tilde{i}_{L-q} \end{cases} \quad \dots(9)$$

As shown in Figure 5, the reference current in (9) is then transformed back into the abc reference frame. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained

$$i_{pf-abc}^{\text{ref}} = T_{dq0}^{abc} i_{pf-dq0}^{\text{ref}}; (T_{dq0}^{abc} = T_{abc}^{dq0})^{-1} \quad \dots(10)$$

Series-VSC: Functions of the series VSCs in each feeder are:

- To mitigate voltage sag and swell;
- To compensate for voltage distortions, such as harmonics;
- To compensate for interruptions (in Feeder2 only).

The control block diagram of each series VSC is shown in Figure 6. The bus voltage is detected and then transformed into the synchronous reference frame using

$$u_{t-dq0} = T_{abc}^{dq0} u_{t-abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{th} \quad \dots(11)$$

$$\begin{cases} u_{t1p} = [u_{t1p-d} & u_{t1p-q} & 0]^T \\ u_{t1n} = [u_{t1n-d} & u_{t1n-q} & 0]^T \\ u_{t10} = [0 & 0 & u_{t10}]^T \\ u_{th} = [u_{th-d} & u_{th-q} & u_{th-0}]^T \end{cases} \quad \dots(12)$$

u_{t1p} , u_{t1n} and u_{t10} are fundamental frequency positive-, neg ative-, and zero-sequence components, respectively, and is the harmonic component of the bus voltage.

According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with a constant amplitude even if the bus voltage is disturbed. Therefore, the expected load $dq0$ voltage in the synchronous $dq0$ reference frame ($u_{l_dq0}^{\text{exp}}$) only has one value

$$u_{l_dq0}^{\text{exp}} = T_{abc}^{dq0} u_{l_abc}^{\text{exp}} = \begin{bmatrix} U_m \\ 0 \\ 0 \end{bmatrix} \quad \dots(13)$$

where the load voltage in the abc reference frame ($u_{l_abc}^{\text{exp}}$) is

$$u_{l_abc}^{\text{exp}} = \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t - 120^\circ) \\ U_m \cos(\omega t + 120^\circ) \end{bmatrix} \quad \dots(14)$$

$$u_{sf_dq0}^{\text{ref}} = u_{t_dq0} - u_{l_dq0}^{\text{exp}} \quad \dots(15)$$

This means u_{t1p_d} in (12) should be maintained at while all other unwanted components must be eliminated. The compensating reference voltage in (15) is then transformed back into the abc reference frame. By using an improved SPWM voltage control technique (sine PWM control with minor loop feedback), the output compensation voltage of the series VSC can be obtained.

POWER-RATING ANALYSIS OF THE MC-UPQC

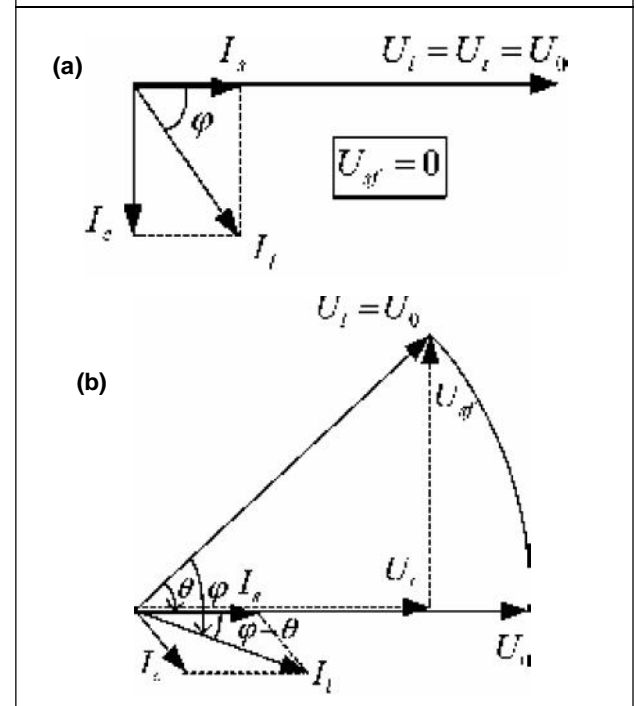
The power rating of the MC-UPQC is an important factor in terms of cost. Before calculation of the power rating of each VSC in the MC UPQC structure, two models of a UPQC are analyzed and the best model which requires the minimum power rating is

considered. All voltage and current phasors used in this section are phase quantities at the fundamental frequency.

There are two models for a UPQC-quadrature compensation (UPQC-Q) and inphase compensation (UPQC-P). In the quadrature compensation scheme, the injected voltage by the series-VSC maintains a quadrature advance relationship with the supply current so that no real power is consumed by the series VSC at steady state. This is a significant advantage when UPQC mitigates sag conditions. The series VSC also shares the Volt-Ampere Reactive (VAR) of the load along with the shunt-VSC, reducing the power rating of the shunt-VSC.

Figure 6 shows the phasor diagram of this scheme under a typical load power factor condition with and without a voltage sag. When

Figure 6: Phasor Diagram of Quadrature Compensation (a) Without Voltage Sag, (b) With Voltage Sag



the bus voltage is at the desired value, the series-injected voltage U_{sf} is zero (Figure 6a). The shunt VSC injects the reactive component of load current, resulting in unity input-power factor. Furthermore, the shunt VSC compensates for not only the reactive component, but also the harmonic components of the load current. For sag compensation in this model, the quadrature series voltage injection is needed as shown in Figure 6b. The shunt VSC injects in such a way that the active power requirement of the load is only drawn from the utility which results in a unity input-power factor.

In an inphase compensation scheme, the injected voltage is inphase with the supply voltage when the supply is balanced. By virtue of inphase injection, series VSC will mitigate the voltage sag condition by minimum injected voltage. The phasor dia-gram of Figure 7 explains the operation of this scheme in case of a voltage sag.

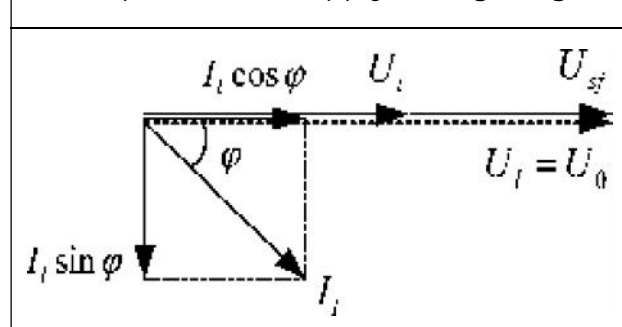
A comparison between inphase (UPQC-P) and quadrature (UPQC-Q) models is made for different sag conditions and load power factors in Basu *et al.* (2007). It is shown that the power rating of the shunt-VSC in the UPQC-Q model is lower than that of the UPQC-P, and the power rating of the series-VSC in the UPQC-P model

is lower than that of the UPQC-Q for a power factor of less than or equal to 0.9. Also, it is shown that the total power rating of UPQC-Q is lower than that of UPQC-P where the VAR demand of the load is high.

As discussed in Section II, the power needed for interruption compensation in Feeder2 must be supplied through the shunt VSC in Feeder1 and the series VSC in Feeder2. This implies that power ratings of these VSCs are greater than that of the se-ries one in Feeder1. If quadrature compensation in Feeder1 and inphase compensation in Feeder2 are selected, then the power rating of the shunt VSC and the series VSC (in Feeder2) will be reduced. This is an important criterion for practical applications.

Based on the aforementioned discussion, the power-rating calculation for the MC-UPQC is carried out on the basis of the linear load at the fundamental frequency. The parameters in Figure 6 are corrected by adding suffix "1", indicating Feeder1, and the parameters in Figure 7 are corrected by adding suffix "2", indicating Feeder2. As shown in Figures 6 and 7, load voltages in both feeders are kept constant at regardless of bus voltages variation, and the load currents in both feeders are assumed to

Figure 7: Phasor Diagram of Inphase Compensation (Supply Voltage Sag)



$$U_{l1} = U_{l2} = U_0 \quad \dots(16)$$

$$\begin{cases} I_{l1} = I_{01} \\ I_{l2} = I_{02} \end{cases} \quad \dots(17)$$

The load power factors in Feeder1 and Feeder2 are assumed to be and and the per-unit sags, which must be compensated in Feeder1 and Feeder2, are supposed to be and, respectively.

If the MC-UPQC is lossless, the active power demand supplied by Feeder1 consists of two parts:

- The active power demand of load in Feeder1;
- The active power demand for sag and interruption compensation in Feeder2.

Thus, Feeder1 current can be found as

$$U_{t1} I_{s1} = U_{t1} I_{l1} \cos \varphi_1 + U_{sf2} I_{t2} \cos \varphi_2 \quad \dots(18)$$

$$(1 - x_1) U_0 I_{s1} = U_0 I_{01} \cos \varphi_1 + x_2 U_0 I_{02} \cos \varphi_2 \quad \dots(19)$$

$$(1 - x_1) I_{s1} = I_{01} \cos \varphi_1 + x_2 I_{02} \cos \varphi_2 \quad \dots(20)$$

$$I_{s1} = \frac{I_{01} \cos \varphi_1}{(1 - x_1)} + \frac{x_2 I_{02} \cos \varphi_2}{(1 - x_1)} \quad \dots(21)$$

From Figure 6, the voltage injected by the series VSC in Feeder1 can be written as in (22) and, thus, the power rating of this converter can be calculated as

$$U_{sf1} = U_{t1} \tan \theta = U_0 (1 - x_1) \tan \theta \quad \dots(22)$$

$$S_{VSC1} = 3U_{sf1} I_{s1} = 3U_0 (1 - x_1) \tan \theta \times \left(\frac{I_{01} \cos \varphi_1}{1 - x_1} + \frac{x_2 I_{02} \cos \varphi_2}{1 - x_1} \right) \quad \dots(23)$$

The shunt VSC current is divided into two parts 1) The first part compensates for the reactive component (and harmonic components) of Feeder1 current and can be calculated from Figure 6 as

$$I_{c1} = \sqrt{I_{l1}^2 + I_{s1}^2 - 2I_{l1} I_{s1} \cos(\varphi_1 - \theta)} \quad \dots(24)$$

$$= \sqrt{I_{01}^2 + I_{s1}^2 - 2I_{01} I_{s1} \cos(\varphi_1 - \theta)}$$

where is calculated in (21). This part of the shunt VSC current only exchanges reactive power (Q) with the system.

$$S_{VSC2} = 3U_{l1} I_{pf} = 3\sqrt{Q^2 + P^2}$$

$$= 3\sqrt{(U_{l1} I_{c1})^2 + (U_{s12} I_{t2} \cos \varphi_2)^2} \quad \dots(25)$$

$$= 3U_0 \sqrt{I_{c1}^2 + (x_2 I_{02} \cos \varphi_2)^2}$$

The second part provides the real power (P), which is needed for a sag or interruption compensation in Feeder2. Therefore, the power rating of the shunt VSC can be calculated as

$$S_{VSC3} = 3U_{sf2} I_{t2} = 3x_2 U_0 I_{02} \quad \dots(26)$$

SIMULATION RESULTS

Figure 8: Circuit Diagram

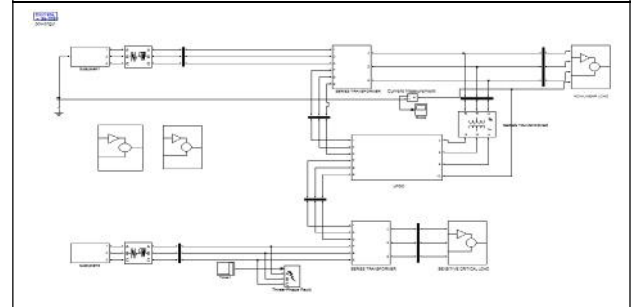


Figure 9: Bus1 Voltage, Series Compensating Voltage, and Load Voltage I feeder1

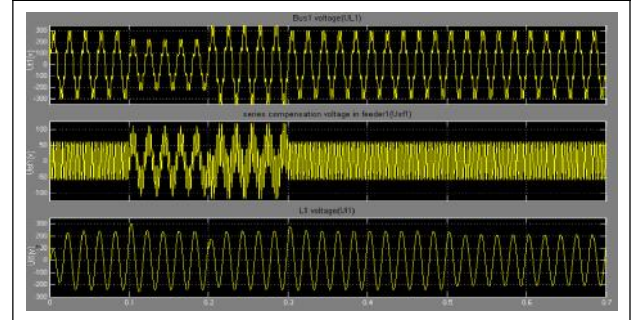


Figure 10: Bus2 Voltage, Series Compensating Voltage, and Load Voltage I feeder2

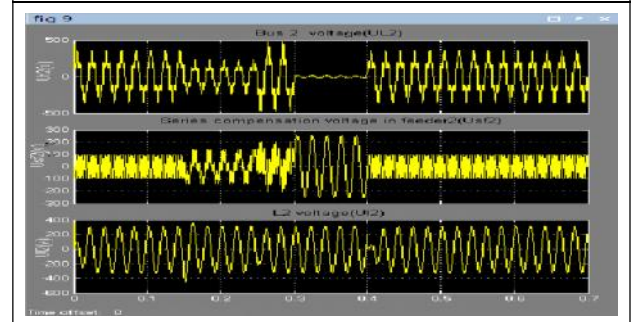


Figure 11: Nonlinear Load Current, Compensating Current, Feeder1 Current, and Capacitor Voltage

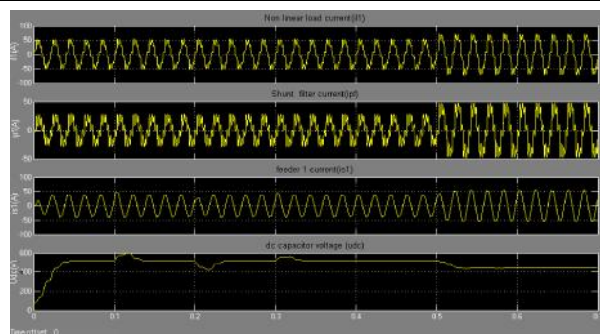
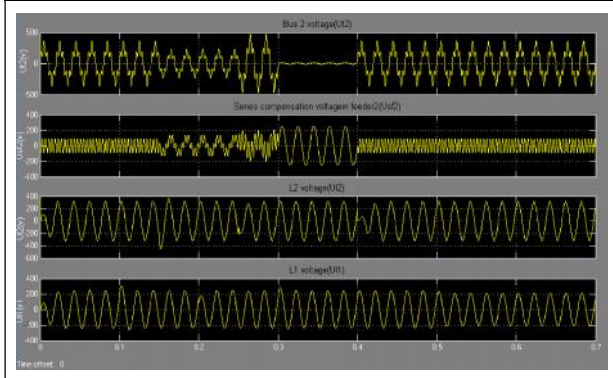


Figure 12: Simulation Results for an Upstream Fault on Feeder2: Bus2 Voltage, Compensating Voltage, and Loads L1 and L2 Voltages



Distortion and Sag/Swell on the Bus Voltage

Let us consider that the power system in Figure 2 consists of two three-phase three-wire 380(v) (rms, L-L), 50-Hz utilities. The BUS1 voltage contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage contains the fifth-order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between $0.1s < t < 0.2$ and 20% swell between $0.2s < t < 0.3$. The BUS2 voltage contains 35% sag between $0.1s < t < 0.25$ and 30% swell between $0.25s < t < 0.3$. The nonlinear/sensitive load L1 is a three-phase rectifier load which supplies an RC load of 10 and 30 F. Finally,

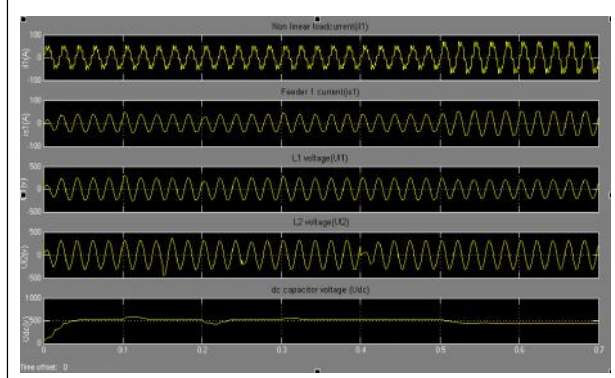
the critical load L2 contains a balanced RL load of 10 and 100 mH.

The MC-UPQC is switched on at $t=0.02$ s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage are shown in Figure 8. In all figures, only the phase waveform is shown for simplicity.

Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in Figure 9. As shown in these figures, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response.

The nonlinear load current, its corresponding compensation current injected by VSC2, compensated Feeder1 current, and, finally, the dc-link capacitor voltage are shown in Figure 11. The distorted non linear load current is compensated very well and the total harmonic distortion of the feeder current is reduced from 28.5% to less than 5%.

Figure 13: Simulation Results for Load Change: Nonlinear Load Current, Feeder1 Current, LoadL1 Voltage, LoadL2 Voltage, and dc-link Capacitor Voltage



CONCLUSION

The simulation studies demonstrate the effectiveness of the proposed concept of simultaneous voltage sag/swell and load reactive power sharing feature of series part of MC-UPQC. The significant advantages of MC-UPQC over general UPQC applications are: 1) the multifunction ability of series supporting load reactive power; 2) better utilization of series inverter rating of UPQC; and 3) reduction in the shunt inverter rating due to the reactive power sharing by both the inverters.

REFERENCES

1. Akagi H (1996), "New Trends in Active Filters for Power Conditioning", *IEEE Trans. Ind. Appl.*, Vol. 32, No. 6, pp. 1312-1322.
2. Aredes M, Heumann K and Watanabe E H (1998), "An Universal Active Power Line Conditioner", *IEEE Trans. Power Del.*, Vol. 13, No. 2, pp. 545-551.
3. Basu M, Das S P and Dubey G K (2007), "Comparative Evaluation of Two Models of UPQC for Suitable Interface to Enhance Power Quality", *Elect. Power Syst. Res.*, pp. 821-830.
4. Fardanesh B, Shperling B, Uzunovic E and Zelingher S (2000), "Multi-Converter FACTS Devices: The Generalized Unified Power Flow Controller (GUPFC)", in *Proc. IEEE Power Eng. Soc. Summer Meeting*, Vol. 4, pp. 2511-2517.
5. Fujita H and Akagi H (1998), "The Unified Power Quality Conditioner: The Integration of Series and Shunt Active Filters", *IEEE Trans. Power Electron.*, Vol. 13, No. 2, pp. 315-322.
6. Ghosh A and Ledwich G (2001), "A Unified Power Quality Conditioner (UPQC) for Simultaneous Voltage and Current Compensation", *Elect. Power Syst. Res.*, pp. 55-63.
7. Gyugyi L, Schauder C D, Williams S L, Rietman T R, Torjerson D R and Edris A (1995), "The Unified Power Flow Controller: A New Approach to Power Transmission Control", *IEEE Trans. Power Del.*, Vol. 10, No. 2, pp. 1085-1097.
8. Gyugyi L, Sen K K and Schauder C D (1999), "Interline Power Flow Controller Concept: A New Approach to Power Flow Management in Transmission Systems", *IEEE Trans. Power Del.*, Vol. 14, No. 3, pp. 1115-1123.
9. Hamid Reza Mohammadi and Ali Yazdian Varjan M (2014), "Multiconverter Unified Power-Quality Conditioning", *IEEE Transactions on Power Delivery*, Vol. 24, No. 3, MC-UPQC.
10. Hu M and Chen H (2000), "Modeling and Controlling of Unified Power Quality Compensator", in *Proc. 5th Int. Conf. Advances in Power System Control, Operation and Management*, pp. 431-435, Hong Kong, China.
11. Jindal A K, Ghosh A and Joshi A (2007), "Interline Unified Power Quality Conditioner", *IEEE Trans. Power Del.*, Vol. 22, No. 1, pp. 364-372.
12. Peng F Z (1998), "Application Issues of Active Power Filters", *IEEE Ind. Appl. Mag.*, Vol. 4, No. 5, pp. 21-30.

13. Rastogi M, Naik R and Mohan N (1994), "A Comparative Evaluation of Harmonic Reduction Techniques in Three-Phase Utility Interface of Power Electronic Loads", *IEEE Trans. Ind. Appl.*, Vol. 30, No. 5, pp. 1149-1155.
14. Sabin D D and Sundaram A (1996), "Quality Enhances Reliability", *IEEE Spectr.*, Vol. 33, No. 2, pp. 34-41.