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Research Paper

SIMULATION OF A VOLTAGE-CONTROLLED STATCOM IN POWERSYSTEM

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A Power quality problem is an occurrence manifested as a nonstandard voltage, current or frequency that results in a failure or a mis-operation of end user equipments. Utility distribution networks, sensitive industrial loads and critical commercial operations suffer from various types of outages and service interruptions which can cost significant financial losses. With the restructuring of power systems and with shifting trend towards distributed and dispersed generation, the issue of power quality is going to take newer dimensions. In developing countries like India, where the variation of power frequency and many such other determinants of power quality are themselves a serious question, it is very vital to take positive steps in this direction. The present work is to identify the prominent concerns in this area and hence the measures that can enhance the quality of the power are recommended. This work describes the techniques of correcting the supply voltage sag, swell and interruption in a distributed system. At present, a wide range of very flexible controllers, which capitalize on newly available power electronics components, are emerging for custom power applications. Among these, the distribution static compensator and the dynamic voltage restorer are most effective devices, both of them based on the VSC principle. A D-STATCOM injects a current into the system to correct the voltage sag, swell and interruption.

Keywords: Power quality problem, Power frequency, STATCOM

INTRODUCTION

Distribution system suffers from current as well as voltage-related Power-Quality (PQ) problems, which in-clude poor power factor, distorted source current, and voltage disturbances (Bollen, 2000; and Fujita and Akagi, 2007). A DSTATCOM, connected at the Point of Common Coupling (PCC), has been utilized to mitigate both types of PQ problems (Ghosh and Ledwich, 2003; Mishra *et al.*, 2003 and 2007; Elnady and Salama, 2005; Fujita and Akagi, 2007; Jain *et al.*, 2006; Gupta *et al.*, 2008; Mishra and Karthikeyan, 2009; Yazdani *et al.*, 2009; Mitra and

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Venayagamoorthy, 2010; and Rahmani *et al.*, 2012). When operating in Current Control Mode (CCM), it injects reactive and harmonic components of load currents to make source currents balanced, sinusoidal, and in phase with the PCC voltages (Ghosh and Ledwich, 2003; Elnady and Salama, 2005; Mishra *et al.*, 2007; Mishra and Karthikeyan, 2009; and Rahmani *et al.*, 2012). In Voltage-Control Mode (VCM) (Mishra *et al.*, 2003; Jain *et al.*, 2006; Gupta *et al.*, 2008; Yazdani *et al.*, 2009; and Mitra and Venayagamoorthy, 2010), the DSTATCOM regulates PCC voltage at a reference value to protect critical loads from voltage disturbances, such as sag, swell, and unbalances. However, the advantages of CCM and VCM cannot be achieved simultane-ously with one active filter device, since two modes are inde-pendent of each other.

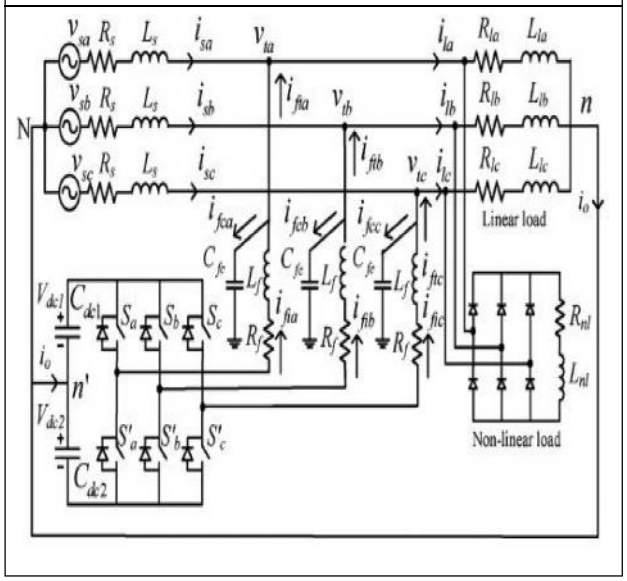
In CCM operation, the DSTATCOM cannot compensate for voltage disturbances. Hence, CCM operation of DSTATCOM is not useful under voltage disturbances, which is a major disad-vantage of this mode of operation (Ko *et al.*, 2006). Traditionally, in VCM operation, the DSTATCOM regulates the PCC voltage at 1.0 p.u. However, a load works satisfactorily for a permis-sible voltage range (Moradlou and Karshenas, 2011). Hence, it is not necessary to regulate the PCC voltage at 1.0 p.u. While maintaining 1.0 p.u. voltage, DSTATCOM compensates for the voltage drop in feeder. For this, the compensator has to supply additional reactive currents which increases the source currents. This increases losses in the Voltage-Source Inverter (VSI) and feeder. Another important as-pect is the rating of the VSI. Due to increased current injection, the VSI is de-rated in steady-state condition. Consequently, its capability to mitigate deep voltage sag decreases. Also, UPF cannot be achieved when the PCC voltage is 1 p.u. In the litera-ture, so far, the operation of DSTATCOM is not reported where the advantages of both modes are achieved based on load re-quirements while overcoming their demerits.

This paper considers the operation of DSTATCOM in VCM and proposes a control algorithm to obtain the reference load terminal voltage. This algorithm provides the combined advan-tages of CCM and VCM. The UPF operation at the PCC is achieved at nominal load, whereas fast voltage regulation is pro-vided during voltage disturbances. Also, the reactive and har-monic component of load current is supplied by the compen-sator at any time of operation. The deadbeat predictive con-troller (Kukrer, 1996; Rodriguez *et al.*, 2007; and Barros and Silva, 2010) is used to generate switching pulses. The con-trol strategy is tested with a three-phase four-wire distribution system. The effectiveness of the proposed algorithm is validated through detailed simulation and experimental results.

PROPOSED CONTROL SCHEME

Circuit diagram of a DSTATCOM-compensated distribution system is shown in Figure 1. It uses a three-phase, four-wire, two-level, neutral-point-clamped VSI. This structure allows independent control to each leg of the VSI (Mishra *et al.*, 2007). Figure 2 shows the single-phase equivalent representation of Figure 1. Variable is a switching function, and can be either or depending upon switching state. Filter inductance and resistance are and,

Figure 1: Circuit Diagram of the DSTATCOM-Compensated Distribution System



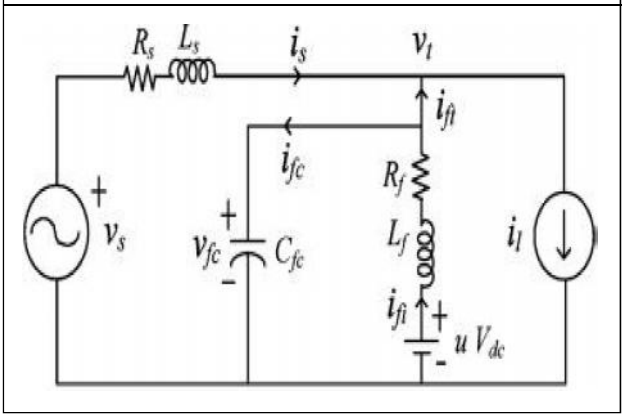
respectively. Shunt capacitor eliminates high-switching frequency components.

First, discrete modeling of the system is presented to obtain a discrete voltage control law, and it is shown that the PCC voltage can be regulated to the desired value with properly chosen pa-rameters of the VSI. Then, a procedure to design VSI parame-ters is presented. A Proportional-Integral (PI) controller is used to regulate the dc capacitor voltage at a reference value. Based on instantaneous symmetrical component theory and complex Fourier transform, a reference voltage magnitude generation scheme is proposed that provides the advantages of CCM at nominal load. The overall controller block diagram is shown in Figure 3. These steps are explained as follows.

System Modeling and Generation of the Voltage-Control Law

The state-space equations for the circuit shown in Figure 2 are given by

Figure 2: Single-Phase Equivalent Circuit of DSTATCOM



$$\dot{x} = A\,x + B\,z \qquad ...(1)$$

where

$$A = \begin{bmatrix} 0 & \frac{1}{C_{fc}} & 0 \\ -\frac{1}{L_f} & -\frac{R_f}{L_f} & 0 \\ -\frac{1}{L_s} & 0 & -\frac{R_s}{L_s} \end{bmatrix},$$

$$B = \begin{bmatrix} 0 & -\frac{1}{C_{fc}} & 0 \\ \frac{V_{dc}}{L_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_s} \end{bmatrix},$$

$$x = [v_{fc} \quad i_{fi} \quad i_s]^t, \quad z = [u \quad i_{ft} \quad v_s]^t.$$

The general time-domain solution of (1) to compute the state vector x(t) with known initial value $x(t_0)$, is given as follows:

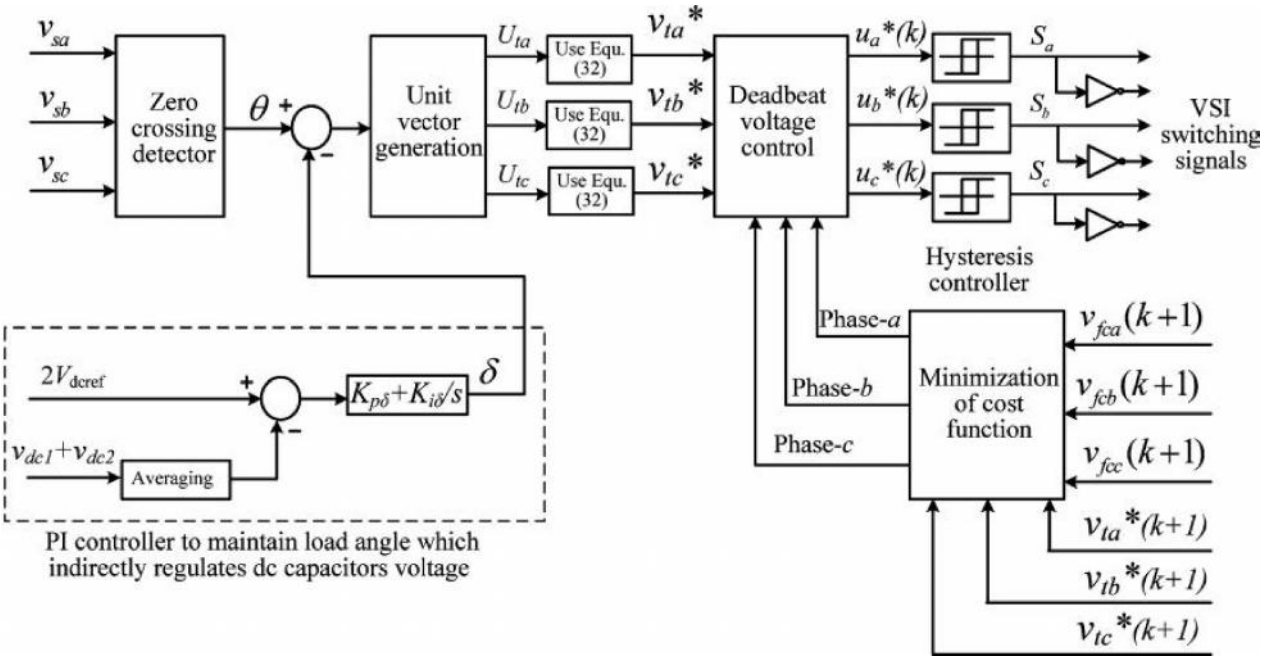
$$x(t) = e^{A(t-t_0)}\,x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)} B\,z(\tau)\,d\tau \qquad ...(2)$$

The equivalent discrete solution of the continuous state is obtained by replacing $t_0 = kT_d$ and $t = (k + 1)T_d$ as follows:

$$x(k+1) = e^{AT_d}\,x(k) + \int_{kT_d}^{T_d+kT_d} e^{A(T_d+kT_d-\tau)} B\,z(\tau)\,d\tau \qquad ...(3)$$

In (3), z(t) and z(k) represent the th sample and sampling period, respectively. During the

Figure 3: Overall Block Diagram of the Controller to Control DSTATCOM in a Distribution System



consecutive sampling period, the value of is held constant, and can be taken as. After simplification and changing the integration variable, (3) is written as (Nagrath and Gopal, 1982)

$$x(k+1) = e^{AT_d}\, x(k) + \int_0^{T_d} e^{A\lambda} B\, d\lambda\, z(k) \qquad ...(4)$$

Equation (4) is rewritten as follows:

$$x(k+1) = G\, x(k) + H\, z(k) \qquad ...(5)$$

Where G and H are sampled matrices, with a sampling time of Td. For small sampling time, matrices G and H are calculated as follows:

$$G = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} = e^{AT_d} \approx I + AT_d + \frac{A^2 T_d^2}{2} \qquad ...(6)$$

$$H = \begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_0^{T_d} e^{A\lambda} B\, d\lambda \approx \int_0^{T_d} (I + A\lambda)\, B\, d\lambda. \qquad ...(7)$$

From (6) and (7), $G_{11} = 1 - T_d^2/2L_fC_{fc}, G_{12} = T_d/C_{fc} - T_d^2 R_f/2L_fC_{fc}, G_{13} = 0, H_{11} = T_d^2 V_{dc}/2L_fC_{fc}, H_{12} = -T_d/C_{fc}$, and $H_{13} = 0$. Hence, the capacitor voltage using (5) is given as

$$v_{fc}(k+1) = G_{11} v_{fc}(k) + G_{12} i_{fi}(k) + H_{11} u(k) + H_{12} i_{ft}(k) \qquad ...(8)$$

As seen from (8), the terminal voltage can be maintained at a reference value depending upon the VSI parameters and sampling time. Therefore, VSI parameters must be chosen carefully. Let be the reference load terminal voltage. A cost function is chosen as follows (Mishra *et al.*, 2003):

$$J = \left[v_{fc}(k+1) - v_t^*(k+1)\right]^2 \qquad ...(9)$$

The cost function is differentiated with respect u(k) to and its minimum is obtained at

$$v_{fc}(k+1) = v_t^*(k+1) \qquad ...(10)$$

The deadbeat voltage-control law, from (8) and (10), is given as

$$u^*(k) = \frac{v_t^*(k+1) - G_{11}v_{fc}(k) - G_{12}i_{fi}(k) - H_{12}i_{ft}(k)}{H_{11}}$$

...(11)

In (11), $V_t(k+1)$ is the future reference voltage which is unknown. One-step-ahead prediction of this voltage is done using a second-order Lagrange extrapolation formula as follows:

$$v_t^*(k+1) = 3\,v_t^*(k) - 3\,v_t^*(k-1) + v_t^*(k-2).$$

...(12)

The term $v_t^*(k+1)$ is valid for a wide frequency range and when substituted in (11), yields to a one-step-ahead deadbeat voltage-control law. Finally, is converted into the ON/OFF switching command to the corresponding VSI switches using a deadbeat hysteresis controller (Kukrer, 1996).

Design of VSI Parameters

DSTATCOM regulates terminal voltage satisfactorily, de-pending upon the properly chosen VSI parameters. The design procedure of these parameters is presented as follows.

Voltage Across DC Bus (Vdc): The dc bus voltage is taken twice the peak of the phase voltage of the source for satisfactory performance [19]. Therefore, for a line voltage of 400 V, the dc bus voltage is maintained at 650 V.

DC Capacitance (Cdc): Values of dc capacitors are chosen based on a period of sag/swell and change in dc bus voltage during transients. Let the total load rating be kVA. In the worst case, the load power may vary from minimum to maximum that is, from 0 to kVA. The compensator needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in the deviation of capacitor voltage from its reference value. The voltage continues to decrease until the capacitor voltage controller comes into action. Consider that the voltage controller takes cycles, that is, seconds to act, where is the system time period. Hence, maximum energy exchange by the compensator during transient will be pST. This energy will be equal to the change in the capacitor stored energy.

Therefore

$$\frac{1}{2}C_{\mathrm{dc}}\left(V_{\mathrm{dcref}}^2 - V_{\mathrm{dc}}^2\right) = p\,S\,T$$

...(13)

where V_{dcref} and V_{dc} are the reference dc bus voltage and maximum-allowed voltage during transients, respectively. Hence

$$C_{\mathrm{dc}} = \frac{2\,p\,S\,T}{V_{\mathrm{dcref}}^2 - V_{\mathrm{dc}}^2}$$

...(14)

Here, S = 10 kVA, V_{dcref} = 650 V, p= 1, and V_{dc} = 0.8 V_{dcref} or 1.2 V_{dcref}. Using (14), capacitor values are found to be 2630 and 2152 uf. The capacitor value 2600 uf is chosen to achieve satisfactory performance during all operating conditions.

Filter Inductance (Lf): Filter inductance should provide reasonably high switching frequency and a sufficient rate of change of current such that VSI currents follow desired currents. The following equation represents inductor dynamics:

$$L_f\frac{di_{fi}}{dt} = -v_{fc} - R_f i_{fi} + V_{\mathrm{dc}}.$$

...(15)

The inductance is designed to provide good tracking performance at a maximum switching frequency (f_{max}) which is achieved at the zero of the source voltage in the hysteresis controller. Neglecting R_f, L_f is given by

$$L_f = \frac{2\,V_m}{(2\,h_c)\,(2\,f_{\max})} = \frac{0.5\,V_m}{h_c\,f_{\max}} \quad ...(16)$$

Where 2 hc is the ripple in the current. With f_{max} = 10 kHz and 0.75 A (5% of rated current), the value of L_f using (16) is found to be 21.8 mH, and 22 mH is used in realizing the filter.

Shunt Capacitor: The shunt capacitor should not resonate with feeder inductance at the fundamental frequency (C_f). Capacitance, at which resonance will occur, is given as

$$C_{fcr} = \frac{1}{\omega_o^2\,L_s} \quad ...(17)$$

For proper operation, C_{fc} must be chosen very small compared to C_{fcr}. Here, a value of 5 F is chosen which provides an impedance of 637 at. This does not allow the capacitor to draw significant fundamental reactive current.

Controller for DC Bus Capacitor Voltage

Average real power balance at the PCC will be

$$P_{\rm pcc} = P_{lavg} + P_{\rm loss} \quad ...(18)$$

where P_{pcc}, P_{lavg}, and P_{loss} are the average PCC power, load power, and losses in the VSI, respectively. The power available at the PCC, which is taken from the source, depends upon the angle between source and PCC voltages, that is, load angle.

Hence, must be maintained constant to keep constant. The voltage of the dc bus of DSTATCOM can be maintained at its reference value by taking inverter losses from the source. If the capacitor voltage is regulated to a constant reference value, is a constant value. Consequently, is also a constant value. Thus, it is evident that dc-link voltage can be regulated by generating a suitable value of this includes the effect of losses in the VSI and, therefore, it takes care of the term in its action. To calculate load angle, the averaged dc-link voltage (V_{dc1} + V_{dc2}) is compared with a reference voltage, and error is passed through a PI controller. The output of the PI controller, which is load angle, is given as follows:

$$\delta = K_{p\delta}\,e_{\rm vdc} + K_{i\delta}\int e_{\rm vdc}\,dt \quad ...(19)$$

where $e_{vdc} = 2\,V_{\rm dcref} - (V_{\rm dc1} + V_{\rm dc2})$ is the voltage error. Terms $K_{p\delta}$ and $K_{i\delta}$ are proportional and integral gains, respectively must lie between 0 to 90 for the power flow from the source to PCC. Hence, controller gains must be chosen carefully

Proposed Method to Generate Reference Terminal Voltages

Reference terminal voltages are generated such that, at nom-inal load, all advantages of CCM operation are achieved while DSTATCOM is operating in VCM. Hence, the DSTATCOM will inject reactive and harmonic components of load current. To achieve this, first the fundamental positive-sequence component of load currents is computed. Then, it is assumed that these currents come from the source and considered as reference source currents at nominal load. With these source currents and for UPF at the PCC, the magnitude of the PCC voltage is calcu-lated.

Let three-phase load currents $i_{la}(t)$ $i_{lb}(t)$ and $i_{lc}(t)$ be represented by the following equations:

The fundamental positive-sequence component of load current, calculated by finding the complex Fourier coefficient, is expressed as follows:

$$i_{lj}(t) = \sum_{n=1}^{m} \sqrt{2}\, I_{lj\,n} \sin\left(n\,\omega t + \phi_{lj\,n}\right)$$

...(20)

Where j = a b c represent three phases, n is the harmonic number, and is the maximum harmonic order represents the phase angle of the th harmonic with respect to reference in phase- and is similar to other phases. Using instantaneous symmetrical component theory, instantaneous zero-sequence, positive-sequence, and negative-sequence current components are calculated as follows:

$$\begin{bmatrix} i_{la}^{0}(t) \\ i_{la}^{+}(t) \\ i_{la}^{-}(t) \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} i_{la}(t) \\ i_{lb}(t) \\ i_{lc}(t) \end{bmatrix}$$

...(21)

where is a complex operator and defined by $e^{j\,2\,\pi/3}$.

The fundamental positive-sequence component of load current $\bar{I}_{la1}^{+}$, calculated by finding the complex Fourier coefficient, is expressed as follows

$$\bar{I}_{la1}^{+} = \frac{\sqrt{2}}{T} \int_{0}^{T} i_{la}^{+}(t)\, e^{-j(\omega\, t - 90^{\circ}}$$

...(22)

$\bar{I}_{la1}^{+}$ is a complex quantity, contains magnitude and phase angle information, and can be expressed in phasor form as follows:

$$\bar{I}_{la1}^{+} = \left|\bar{I}_{la1}^{+}\right| \angle \bar{I}_{la1}^{+}$$

...(23)

Hence, the instantaneous fundamental positive-sequence component of load current in phase-a $i_{la1}^{+}(t)$, is expressed as

$$i_{la1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t + \angle \bar{I}_{la1}^{+}\right)$$

...(24)

The fundamental positive-sequence component of load currents must be supplied by the source at nominal load. Hence, it will be treated as reference source currents. For UPF at nominal operation, the nominal load angle δ_0 is used. By knowing, $i_{la1}^{+}(t)$ fundamental positive-sequence currents in phases b and c can be easily computed by providing a phase displacement of -2pi/3 and 2pi/3, respectively, and are given as

$$\begin{aligned} i_{sa}^{*} &= i_{la1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t - \delta_0\right) \\ i_{sb}^{*} &= i_{lb1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t - \frac{2\pi}{3} - \delta_0\right) \\ i_{sc}^{*} &= i_{lc1}^{+}(t) = \sqrt{2}\, \left|\bar{I}_{la1}^{+}\right| \sin\left(\omega t + \frac{2\pi}{3} - \delta_0\right) \end{aligned}$$

...(25)

When reference source currents derived in (25) are supplied by the source, three-phase terminal voltages can be computed using the following equations:

$$v_{tj}(t) = v_{sj}(t) - L_s \frac{di_{sj}^{*}}{dt} - R_s i_{sj}^{*}$$

...(26)

Let the rms value of reference terminal and source voltages be and, respectively. For UPF, the source current and terminal voltage will be in phase. However, to obtain the expression of independent of, we assume the PCC voltage as a reference phasor for the time-

being. Hence, phase-quantities, by considering UPF at the PCC, will be

$$v_{ta}(t) = \sqrt{2}\, V_t^* \sin \omega t$$
$$i_{sa}^* = \sqrt{2}\, \left| \bar{I}_{la1}^+ \right| \sin \omega t$$
$$v_{sa}(t) = \sqrt{2}\, V \sin (\omega t + \delta_0)$$

...(27)

Substituting (27) into (26), the phasor equation will be

$$V_t^* \angle 0 = V \angle \delta_0 - (R_s + jX_s) \left| \bar{I}_{la1}^+ \right|$$

...(28)

Figure 4: Simulation Circuit

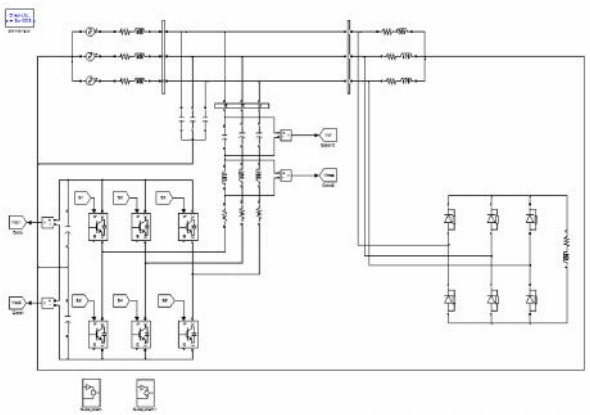


Figure 5: Control Circuit

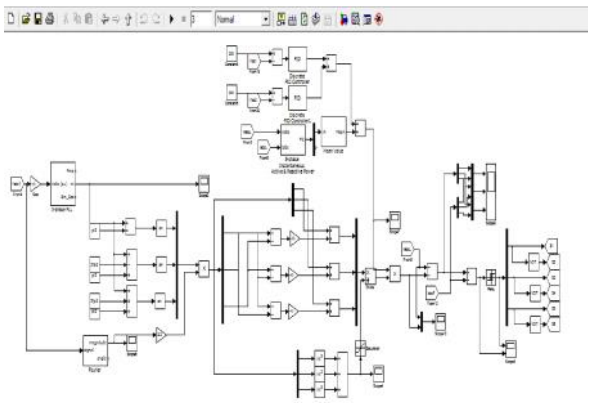


Figure 6: Input 3 Phase Currents and Voltages

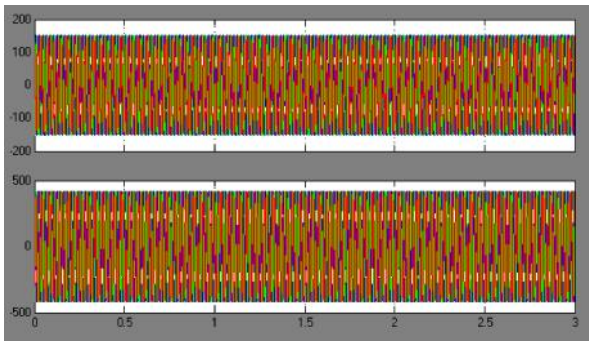


Figure 7: Dc Bus Voltages vdc1 and vdc2

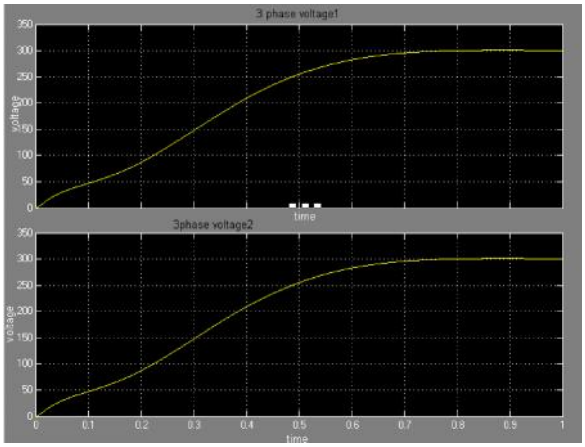


Figure 8: 3 Phase Filter Currents

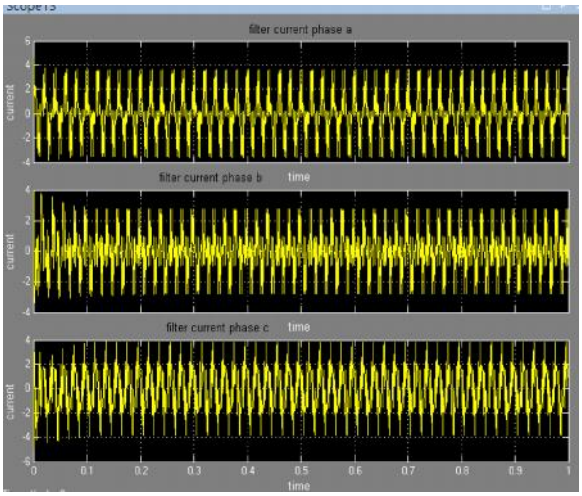
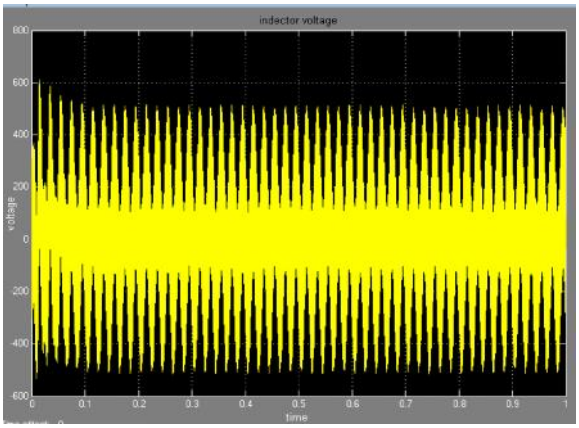


Figure 9: Inductor Voltage



Simplifying the above equation

$$V_t^* = V\cos\delta_0 + jV\sin\delta_0 - \left|\bar{I}_{la1}^+\right| R_s - j\left|\bar{I}_{la1}^+\right| X_s$$

...(29)

Equating real and imaginary parts of both sides of (29), the following equation is obtained:

$$\begin{aligned} V\cos\delta_0 &= V_t^* + \left|\bar{I}_{la1}^+\right| R_s \\ V\sin\delta_0 &= \left|\bar{I}_{la1}^+\right| X_s. \end{aligned} \quad \text{...(30)}$$

SIMULATION RESULTS

The control scheme is implemented using MATLAB software. Terminal voltages and source currents before compensation are plotted in Figure 6. Distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted.

Using the proposed method, terminal voltages and source currents in phases and are shown in Figure 6, respectively. It can be seen that the respective terminal voltages and source currents are in phase with each other, in addition to being balanced and sinusoidal. Therefore, UPF is achieved at the load terminal.

The voltage across the dc bus is shown in Figure 7. During transients, this voltage deviates from its reference voltage. However, it is brought back to the reference value once steady state is reached.

CONCLUSION

This paper has presented the power quality problems such as voltage dips, swells and interruptions, consequences, and mitigation techniques of D-STATCOM. The design and applications of D-STATCOM for voltage sags, interruptions and swells, and comprehensive results are presented.

A new PWM-based control scheme has been implemented to control the electronic valves in the two-level VSC used in the D-STATCOM. As opposed to fundamental frequency switching schemes already available in the MATLAB/SIMULINK, this PWM control scheme only requires voltage measurements. This characteristic makes it ideally suitable for low-voltage custom power applications.

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