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Research Paper

SEVEN LEVEL INVERTER WITH SINGLE DC SOURCE INTERCONNECTED PHOTOVOLTAIC SYSTEM

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In this paper, seven level inverter with single DC source interconnected Photovoltaic System (PV) is presented. The proposed system, mainly focuses on designing an efficient topology for MLI with reduced number of electronic components, improve the harmonic performance and reduce the Total Harmonic Sistortion (THD) level. A seven level inverter (+3Vdc, 2Vdc, +Vdc, 0, -Vdc, -2Vdc and -3Vdc) withsingle dc source and reduced switching power losses has been designed.Capacitor voltage balancing DC-DC isolation converter has been used to handle the dynamic varying conditions (Temperature, Irradiation) of the PV panel.A single reference multicarrier Sine Pulse Width Modulation (SPWM) with commutation logics has been used to control the bidirectional switches and Zero Cross Detector (ZCD) has been used to control the H-bridge inverter. The performance (with/without filter) of this approach based on the THD has beensimulated in MATLAB/Simulink software and developed a prototype experimental results are presented.

Keywords: Multilevel inverter, Photovoltaic systems, PI controller, DC-DC isolation converter

INTRODUCTION

Nowadays, a number of research works have focused on renewable energy based MLIs designs in grid connected power distribution system due to their potential excellence in various applications such as, chemical and oil plants, power generation, energy transmission, power quality devicesand induction motor drives (Carrasco, 2006; and Lopez *et al.*, 2006). Among the renewable energy sources, Photo Voltaic (PV) systems have been extensively utilized for diverse applications as it is pollution free and largest energy potential (Jain and Agarwal, 2007). A large number of nonlinear loads have been deployed for commercial and non-commercial purposes due to the demand of electrical utilities, where PV panel has been used as the

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input DC source.MLIs can be classified into three topologies such as diode clamped, flying capacitors and H-bridgecells with separate DC sources. Among these inverter topologies, clamped diode needs complex pulse width modulation controls because more capacitors and diodes are necessary for generating output levels and more power losses. The problems in flying capacitor MLIs are poor in switching utilization and poor efficiency in real power transmission, whereas, difficult to solve capacitor voltage balancing problems (Xiao *et al.*, 2004).

In recent years, cascaded H bridge multilevel inverter has been widely deployed in diversified applications as input separated dc sources could be easily interfaced to the MLI to deliver higher output voltages with minimum THD (Duggapu and Nulakajodu; Villanueva *et al.*, 2011 and 2012). But, the major limitation of this cascaded MLI is that more number of dc sources is required for this topology. Moreover, the topology comprises of a number of switches which would in turn result in more power losses.Therefore, Single DC supply has become an attractive research area. This single DC supply would highly influence the capacitor voltage balance in MLI. PV panel irradiance variance occurs due to the dynamic nature of the climate, light intensity, temperature, etc. The single DC supply with the PV panel would result in the irradiance variance issue which would greatly affect the supply voltage (high/low) of the system (Sepahvand *et al.*, 2013).

A sub multilevel cell is proposed and then series connections of the submultilevel cells are proposed in (Alagu Sundari and Dhinakaraj, 2014). The proposed multilevel inverter uses reduced number of switching devices. The proposed system is established to obtain optimal structures regarding different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources, etc. (Babaei *et al.*, 2007). However Harmonics produced also less with this method.A new modified cascaded H-Bridge multilevel inverter presented with reduction of switching component (Cherukuru *et al.*, 2014). In traditional CHB inverters required more number of apparatuses, it seem to more complex control circuitry and bulky. The Conduction losses are increased when the number of Switches is increased.A three phase 11 level is proposed with reduced number of switches (Rajmadhan *et al.*, 2014). An algorithm has been generated on the basis of optimized harmonic stepped waveform technique to find out firing angle for multilevel inverter to decrease harmonic content present in output. Harmonic contents present in the output could be more reduced using an efficient improved optimized harmonic stepped waveform technique.A new hybrid cascaded H-bridge multilevel inverter motor drive DTC scheme for electric vehicles where each phase of the inverter can be implemented using a single DC source (Cherukuru, 2014). Different amounts of energy are required due to the induction motor operating point fast variation.Two types of multilevel inverters, known as symmetrical and asymmetrical multilevel inverter proposed (Haiwen *et al.*, 2008; Ahmed *et al.*, 2010; Khoucha *et al.*, 2013; and Rajmadhan *et al.*, 2014). Both types are very effective and efficient for improving the quality of the inverter output voltage. Through proposed inverter topology generates a high-quality output voltage waveform and

harmonic components of output voltage and current are low.

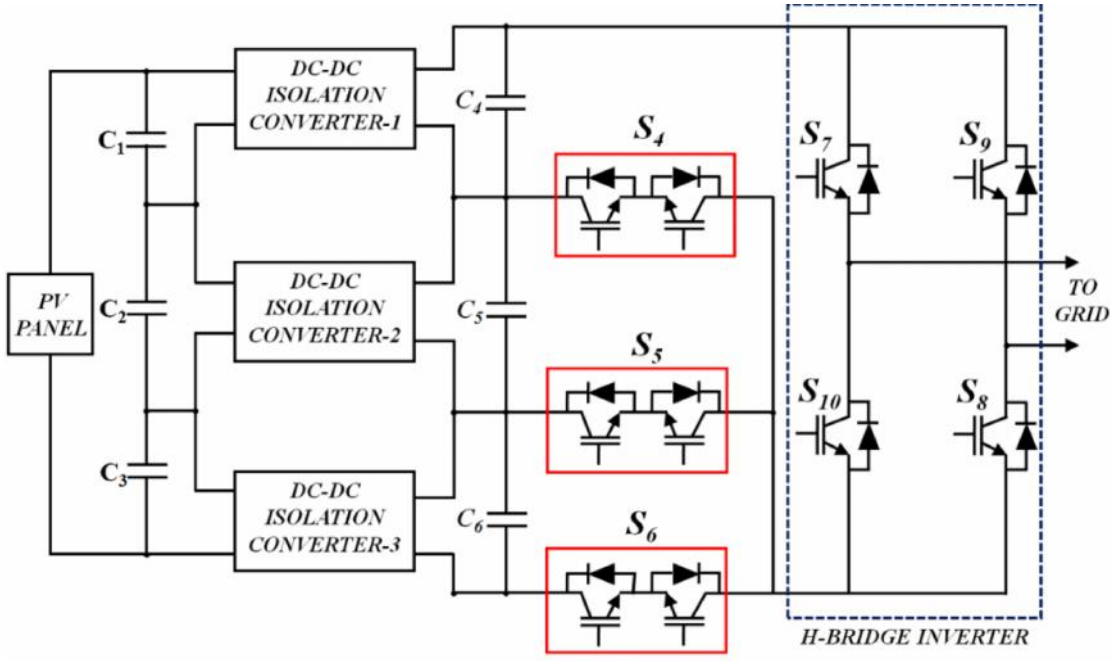
This research work uses a single DC supply MLI with capacitor voltage balancing scheme. This proposed approach would result in a constant voltage even in the presence of above mentioned dynamic natural conditions such as temperature, climate, light intensity, etc. The proposed MLI focuses on reducing the number of switches with single DC supply. This research work uses a single reference multicarrier Sine Pulse Width Modulation (SPWM) approach to control the MLI.

SYSTEM DESCRIPTION

Figure 1 shows the PV based proposed seven level inverter with grid inter connected system, which comprises of voltage balancing capacitors, DC isolation converters and MLI. Three voltage balancing capacitors c_1, c_2 and c_3 are used to balance the voltage obtained from the input PV panel. Three DC-DC isolation converters have been used for maintaining the constant voltage for input varying conditions. The proposed MLI comprises of Anti parallel switches andH-bridge inverter. Based on the switching table mode of operation, three positive voltage levels, three negative voltage levels and a zero level is generated by the proposed system in a sequence of (*+3Vdc, 2Vdc, +Vdc, 0, -Vdc, -2Vdc and -3Vdc*).

The proposed system takes the input supply voltage from the PV panel. The PV panel output would not be constant and would change due to the above mentioned dynamic natural conditions. Under these conditions, the PV output to the load would vary which would affect the performance of the load. In order to solve this issue, this research work proposes an efficient closed loop control scheme with DC-DC isolation converter. The

Figure 1: PV Based Proposed Seven Level Multilevel Inverter



attained constant voltage is applied to the MLI which converts it into a seven levels based on the switching table with SPWM. The following sections discusses in detail about the proposed system model and its mode of operation.

PHOTOVOLTAIC MODULE

Generally, Photo Voltaic (PV) cell is a semiconductor device that converter solar irradiation in to electrical energy is named as "Photo voltaic cell" and this result is called 'Photovoltaic Effect' (Rahim *et al.*, 2011). The PV panel acts as the input dc source for the inverter. The electrical power generated by a solar PV panel mainly depends on the operating conditions, solar irradiation in W/M^2, temperature in degree Celsius, number of cells, short circuit current (I_{sc}), etc. The nonlinear mathematical model of the PV array can be expressed as

$$I = I_{LG} - I_0 \left\{ exp\left[\frac{q}{AKT}(V + I_A R_S\right] - 1 \right\} \quad ...(1)$$

$$I_0 = I_{0r}\left[\frac{T}{T_r}\right]^3 exp\left[\frac{qE_{Go}}{BK}\left\{\frac{1}{T_r} - \frac{1}{T}\right\}\right] \quad ...(2)$$

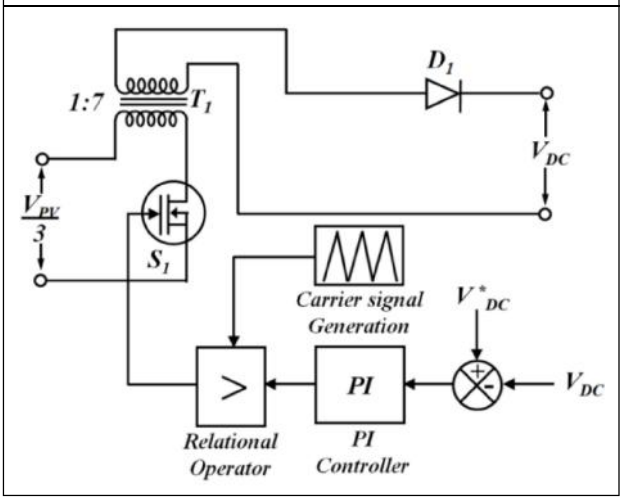
$$I_{LG} = [I_{SCR} + K_1(T_C - 28]\lambda/100 \quad ...(3)$$

where, I = cell output current; I_{LG} = Photon Current; I_0 = Cell Saturation Current of the diode; q = electron charge (1.6 x 10^{-19}); k = Boltzmann's constant; B = A = ideality factor; R_{sh}, R_{se} = Shunt and Series resistance respectively in ohm; V = Panel Voltage in volts; T = Temperature in Kelvin. T_c = Temperature in degree Celsius, T_r = Reference Temperature; I_{SCR} = cell short circuit current; E_{GO} = band gap for silicon.

DC-DC ISOLATION CONVERTER

Figure 2 shows the proposed a DC-DC isolation-1 converter model with closed loop control. It comprises of step up transformers (T_1), power diode D_1 and power switch S_1. The input variable voltage from the PV panel is 48 V and is gets divided among the three voltage balancing capacitors, and as shown in figure 1. Then, the separated voltage across each capacitor is fed into each of the DC-DC isolation convertor (Changchien *et al.*, 2010). Thus, the voltage maintained across the primary winding of the transformer is approximately 15 to 18 V.

Figure 2: Proposed DC-DC Isolation Converter-1 with Closed Loop Control



The output voltage from the isolation converter is taken as the actual voltage for the closed loop control. The peak voltage (V_{peak}) of 325 V is essential for attaining V_{rms} of 230 V based on the following equation $V_{rms} = V_{peak}/\sqrt{2}$. Thus, the voltage across the MLI V_{peak} = 325 V is shared by three isolation DC-DC convertor. Thus, even in voltage and load variation conditions, the voltage across the isolation converter, i.e., capacitors c_4, c_5 and

c_6 should be maintained constant at 108.33 V. Thus, the closed loop control of the proposed DC-DC isolation converter-1has been modeled. Similarly, the same closed loop control process is carried out for the DC-DC isolation converter-2 and 3.

Minimum Capacitance (*C*) of the DC-DC isolation is given by

$$C = \frac{I_a (V_a - V_{pv})}{V_a f_{sb} \Delta V_c} \quad ...(4)$$

$$I_a = \frac{V_{pv} * I_{pv}}{V_a} \quad ...(5)$$

where, f_{sb} = Switching frequency for Boost converter (20 kHz)

V_{pv} = PV panel Voltage (48 V)

V_a = Output Voltage across Capacitor (108 V)

I_a = Average Load Current (1.6188 A)

ΔV_c = Ripple Voltage of Capacitor (0.42 mV)

$$C = C_1 + C_2 + C_3; C_1 = C_2 = C_3;$$

$$C = C_1 + C_2 + C_3; C = 3C_1$$

Therefore, $C_1 = C/3$

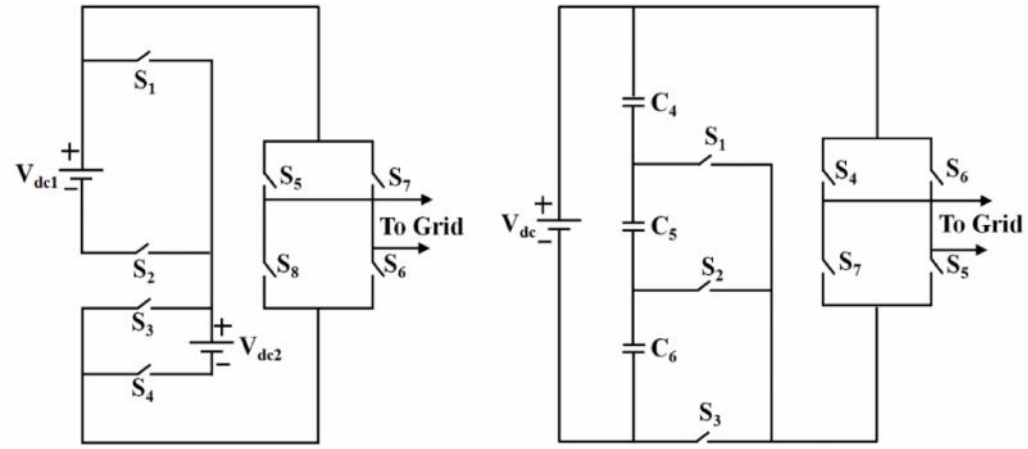
The Proportional Integral (PI) controller is its effectiveness in the control of steady state error of a control system and also its easy implementation (Mikkili and Panda, 2011). K_p and K_i are the proportional and integral gains respectively, the gains depend on the system parameters. In this work, PI controller has been used to improve the settling time, rise time and peak overshoot of the converter output voltage. This is attained through identifying the error which is the difference between the actual and reference DC-DC isolation converter voltage. This error could also be represented by the following equation as

$$y(t) = K_p * e(t) + K_i \int_0^t e(t)dt \quad ...(6)$$

PROPOSED THREE PHASE SEVEN LEVEL INVERTER TOPOLOGY

Figure 3 shows the structural comparison of the conventional seven level Inverter topology

Figure 3: Comparison of Seven Level MLI Structures (a) Conventional Seven Level Inverter Structure (b) Proposed Seven Level Inverter Structure



(a) (b)

Table 1: Switching Sequence of Conventional and Proposed System

Conventional System									Proposed System							
Voltage Rating (V)	Switching States								Voltage Rating (V)	Switching States						
	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}		S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
$+V_{dc}$	0	1	1	0	1	0	0	1	$+V_{dc}$	1	0	0	1	1	0	0
$+2V_{dc}$	1	0	0	1	1	0	0	1	$+2V_{dc}$	0	1	0	1	1	0	0
$+3V_{dc}$	0	1	0	1	1	0	0	1	$+3V_{dc}$	0	0	1	1	1	0	0
0	0	0	0	0	0/1	0	0	0/1	0	0	0	0	0	0/1	0	0/1
$-V_{dc}$	0	1	1	0	0	1	1	0	$-V_{dc}$	1	0	0	0	0	1	1
$-2V_{dc}$	1	0	0	1	0	1	1	0	$-2V_{dc}$	0	1	0	0	0	1	1
$-3V_{dc}$	0	1	0	1	0	1	1	0	$-3V_{dc}$	0	0	1	0	0	1	1

with proposed seven level Inverter topology. In the conventional MLI topology, two different DC input sources namely V_{dc1} and V_{dc2} are required. Moreover, eight switches are being used in the conventional topology which would result in higher switching losses and high initial PV panel cost. As the voltage across V_{dc1} and V_{dc2} would be maintained at 108 V and 217 V respectively (Rahim *et al.*, 2011; and Gopal *et al.*, 2013). Thus, two different PV panels with two different boost converter would be required which would obviously result in higher cost and power losses. Thus, the conventional system may not be effective under certain conditions. The proposed seven level inverter topology, only a single DC source has been used and voltage across the V_{in} would be shared equally among the capacitors c_4, c_5 and c_6. Moreover, only seven switches have been used in the proposed topology which results in minimum switching losses when compared with the conventional seven level inverter. Table 1 shows the switching sequence of conventional and proposed system in which 1 represents the ON state and 0 represent the OFF state.

MODE OF OPERATION

Figure 4 shows the different mode of operation of the proposed seven level inverter. Seven different modes (+3Vdc, 2Vdc and +Vdc, 0, -Vdc, -2Vdc and -3Vdc,) are attained for the proposed seven level inverter.

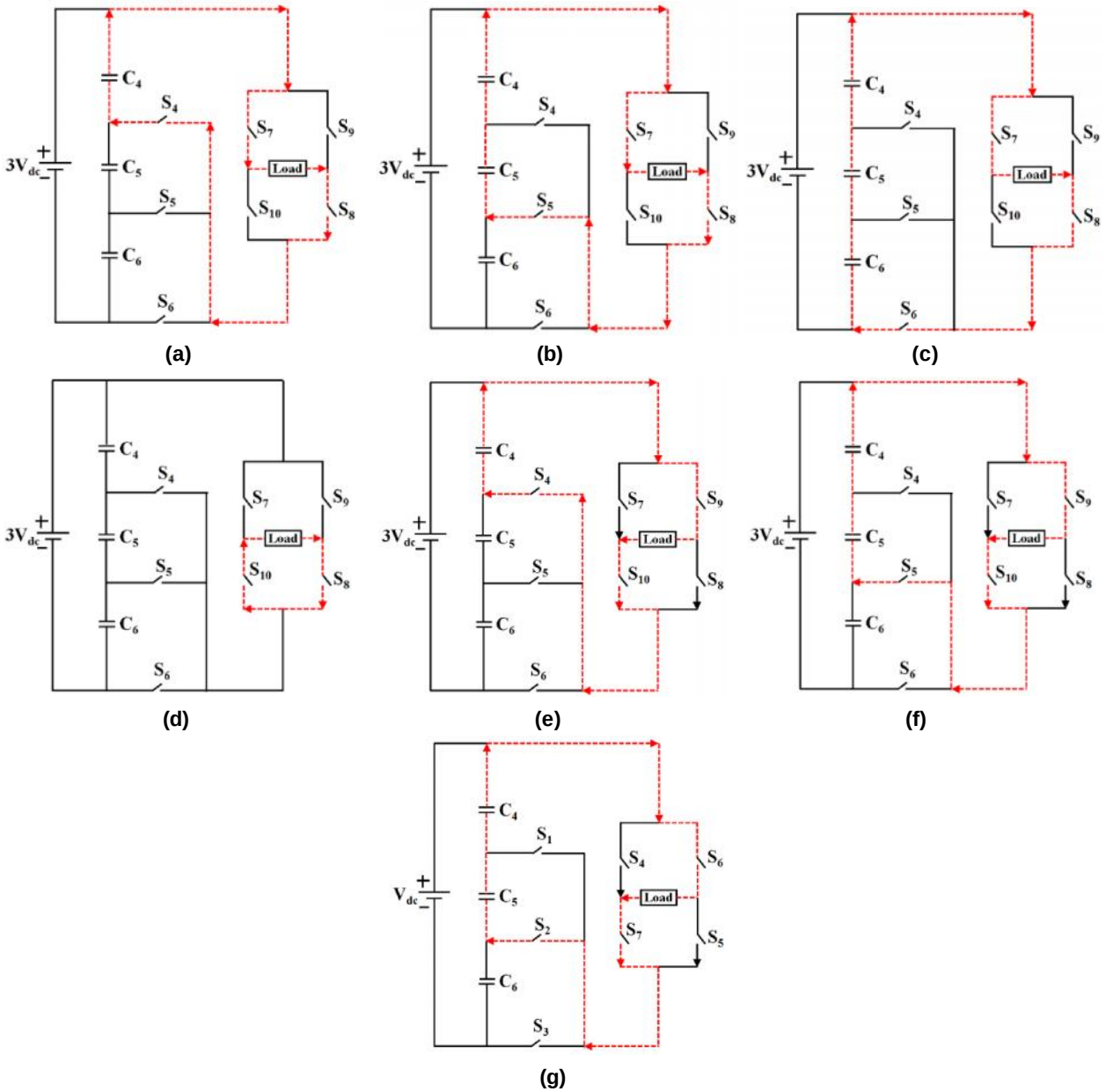
Mode 1 ($+V_{dc}$)

The output voltage of 108 V from the DC-DC isolation converter is maintained constant across the capacitors c_4, c_5 and c_6. In mode 1, initially switches S_4, S_7 and S_8 are switched ON due to the current flow from the positive of the c_4 capacitor towards the drain and source of the S_7 and S_8 switch. Then the current flows through the load and it gets grounded through the bidirectional switch S_4 and ends at the negative of the capacitor c_4. During this mode, only one capacitor c_4 gets conducted which results in $+V_{dc}$.

Mode 2 ($+2V_{dc}$)

In mode 2, initially switches S_5, S_7 and S_8 are switched ON due to the current flow from the positive of the c_4 capacitor towards the drain and source of the S_7 and S_8 switch. Then the current flows through the load and it gets

Figure 4: Mode of Operation of Proposed Seven Level Inverter



grounded through the bidirectional switch S_5 and ends at the negative of the capacitor c_5. Now, the capacitors c_4 and c_5 are in series connection and thus, two capacitors c_4 and c_5 gets conducted which results in $+2V_{dc}$.

Mode 3 ($+3V_{dc}$)

In mode 3, switches S_6, S_7 and S_8 are switched ON due to the current flow from the positive of the c_4 capacitor towards the drain and source of the S_7 and S_8 switch. Then the current flows through the load and it gets grounded through the bidirectional switch S_6 and ends at the negative of the capacitor c_6. Now, the capacitors c_4, c_5 and c_6 are in series connection

and thus, three capacitors c_4, c_5 and c_6 gets conducted which results in $+3V_{dc}$.

Mode 4 ($V_{dc} = 0$)

In mode 4, switches S_8 and S_{10} are switched ON remaining all switches are OFF condition. In this mode load is short circuited, voltage across load is zero.

Mode 5 ($-V_{dc}$)

In mode 5, initially switches S_4, S_9 and S_{10} are switched ON due to the current flow from the positive of the c_4 capacitor towards the drain and source of the S_9 and S_{10} switches. Then the current flows through the load and it gets grounded through the bidirectional switch S_4 and ends at the negative of the capacitor c_4. Now, only one capacitors c_4 gets conducted which results in $-V_{dc}$.

Mode 6 ($-2V_{dc}$)

In mode 6, initially switches S_5, S_9 and S_{10} are switched ON due to the current flow from the positive of the c_4 capacitor towards the drain and source of the S_9 and S_{10} switches. Then the current flows through the load and it gets grounded through the bidirectional switch S_5 and ends at the negative of the capacitor c_5. Now, the capacitors c_4 and c_5 are in series connection and thus, two capacitors c_4 and c_5 gets conducted which results in $-2V_{dc}$.

Mode 7($-3V_{dc}$)

In mode 7, initially switches S_6, S_9 and S_{10} are switched ON due to the current flow from the positive of the c_4 capacitor towards the drain and source of the S_9 and S_{10} switches. Then the current flows through the load and it gets grounded through the bidirectional switch S_6 and ends at the negative of the capacitor c_6. Now, the capacitors c_4, c_5 and c_6 are in series connection and thus, three capacitors c_4, c_5 and c_6 gets conducted which results in $-3V_{dc}$.

CONTROL TECHNIQUE

SPWM is the process of generating the gate pulses by comparing the reference sine wave with the triangular carrier signal. The generated pulses are manipulated using the commutation logic with the help of the modes of the switching table. Among different SPWM techniques, in this approach single reference multi carrier pulse width modulation technique is used. Initially, sine wave (pu) is generated based on $sin\mu t$.

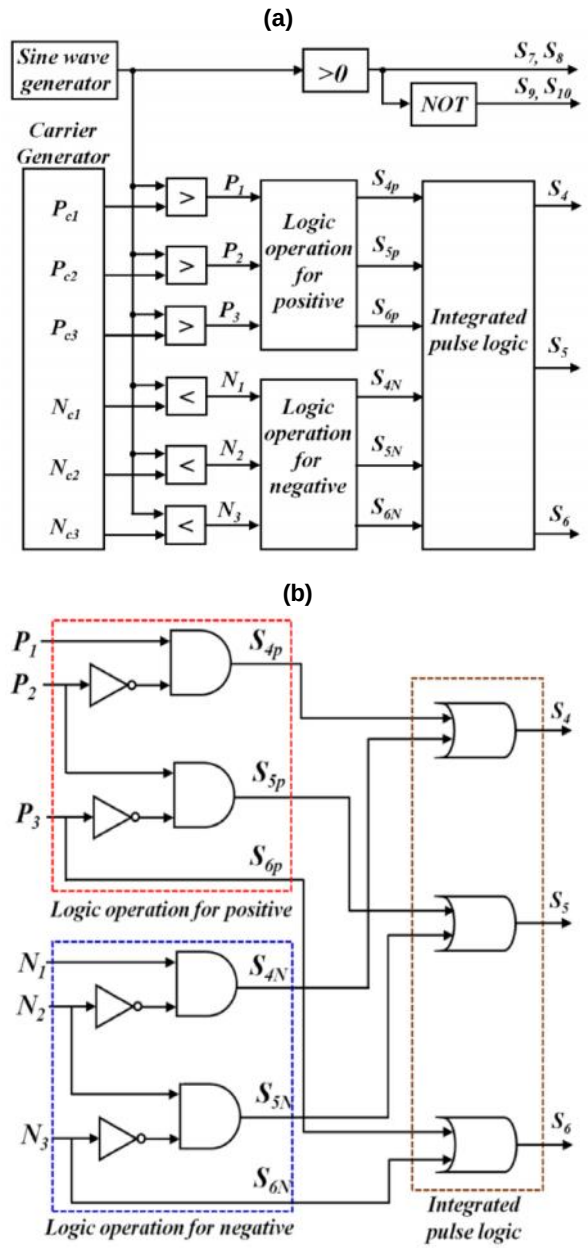
where, angular frequency $\omega = 2\pi f$ and frequency f = 50 Hz

In this proposed seven level inverter approach, three levels of positive waves and three levels of negative waves are required and thus, the (pu) sine wave is multiplied with 3 for satisfying the $+3V_{dc}$ levels of the proposed seven level inverter.

Triangular carrier signal is generated with 10 KHz switching frequency with look up table. Carrier signals with three different positive amplitudes (010, 121, 232) and three different negative amplitudes (0-10, -1-2-1, -2-3-2) are generated. Three positive pulses P_1, P_2 and P_3 and three negative pulses N_1, N_2 and N_3 are obtained from comparing a single sine reference with six carrier signals. The comparator used here is the relational operator wherein greater than '>' is used for positive pulses and lesser than '<' is used for the negative pulses as shown in Figure 5.

Now, in order to generate seven levels in the inverter, three switches S_4, S_5 and S_6 and

Figure 5: Sine Pulse Width Modulation Control Technique



a H-bridge inverter with switches S_7 to S_{10} are to be operated with a logic sequence (Cortes *et al.*, 2010). Each switch S_4, S_5 and S_6 gets conducted at the positive and negative cycles to achieve seven levels. The gate pulses of each switch are attained through the logical model.

In pulse logic Integrated sequence, the positive and negative gate pulses are added to attain the gate pulses for the switches S_4, S_5 and S_6 respectively. Switch S_4 gets conducted at the sequence of $(+V_{dc}, -V_{dc})$. Similarly, Switch S_5 gets conducted at the sequence of $(+2V_{dc}, -2V_{dc})$ and with sequence of $(+3V_{dc}, -3V_{dc})$, switch S_6 gets conducted.

SIMULATION RESULTS

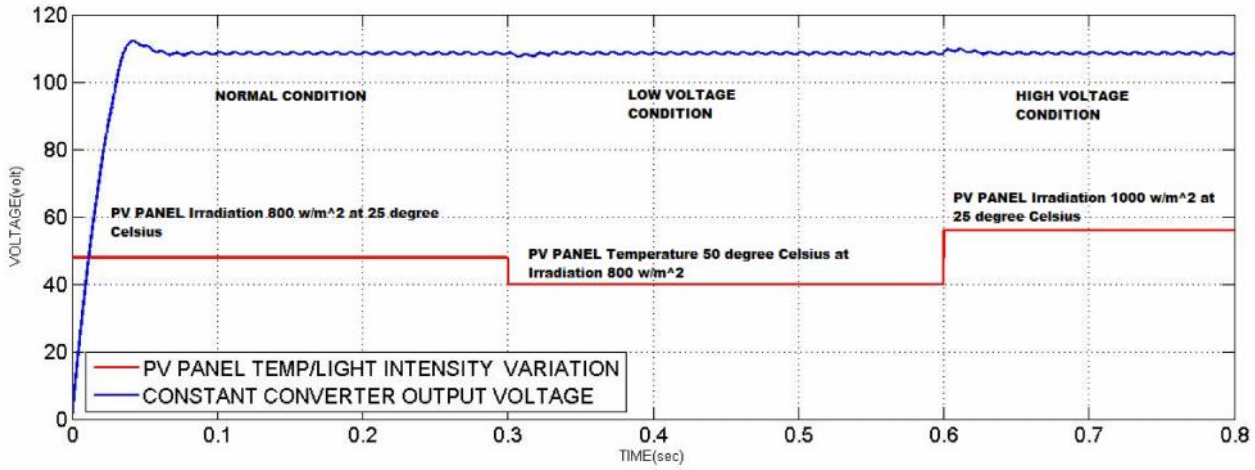
The proposed Modified seven-level inverter system based on has been simulated and verified through MATLAB/Simulink software. The parameters of simulation circuit is listed in Table 2.

Table 2: Simulation Parameters

Description	Parameter	Value
PV Array	Number of cell	120 (12 × 10)
	Nominal voltage	24
Isolation DC-DC converter	Step up transformer	1:7 V
PI controller	K_p	5
	K_i	0.1
Switching frequency		10 KHz
Capacitance	$C_1 = C_2 = C_3$	20 µF
	$C_4 = C_5 = C_6$	1000 µF
LC Filter	L	15 mH
	C	20 µF
Isolation converter output voltage		108 V
Load voltage (RMS)		230 V
Load current (RMS)		2A

Figure 6 shows the output voltage of the converter under PV panel natural variation conditions. In the figure, the normal condition is taken at a temperature of 25 with 800 W/M^2 solar irradiation. In the normal condition, the output voltage of the converter is kept constant

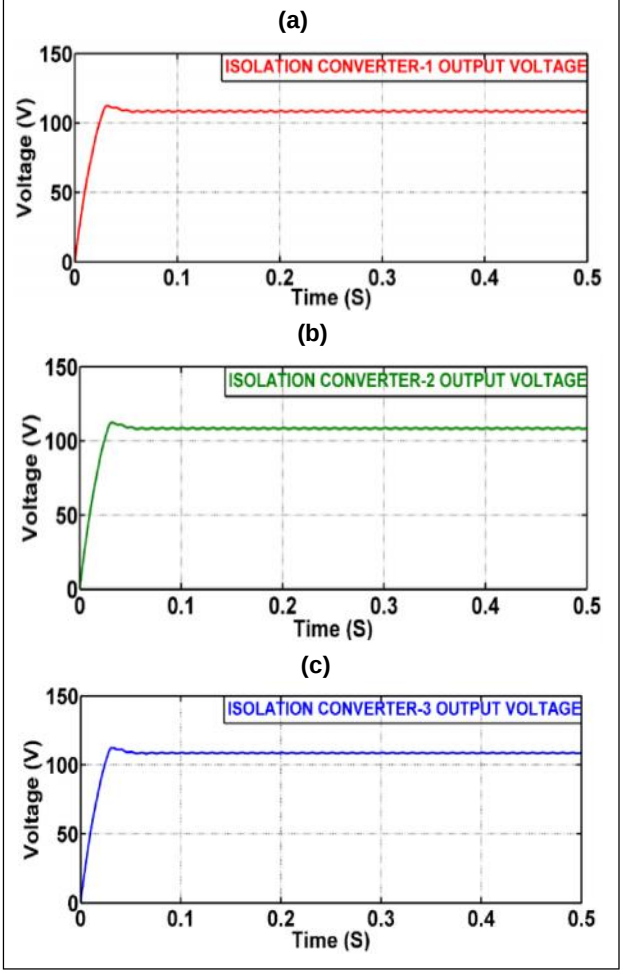
Figure 6: Simulation Result of Isolation Converter Output Voltage Under Natural Variation Conditions



at 108.33 V. The three DC-DC isolation converter output voltages are shown in Figure 7. The Figure 8 depicts switching pattern of DC-DC isolation converter. The Figure 9 represents switching pulse of H-bridge inverter.

The Figure 10 depicts simulation result of load voltage and load current without filter. The simulation waveform of load voltage with and without filter as shown in Figure 11. The Figure 12 depicts the load current with and without filter. The output voltage of DC-DC isolation converter is maintained 108 V. The PV array output voltage is 24 V. The proposed system modified seven level inverter output voltage is 230V rms value load current is 2A. System is the total harmonic distortion (THD) of the proposed system in load voltage was 16.27% and the load current was 18.92%. After filter installation the THD level of load voltage was reduced 1.11% and load current was 1.22% as shown in Figure 13.

Figure 7: Simulation Result of DC-DC Isolation Converter Output Voltage



EXPERIMENTAL RESULTS

To evaluate the performance of the proposed modified seven level inverter is using

Figure 8: Simulation Result of Switching Pulse for Isolation Converter

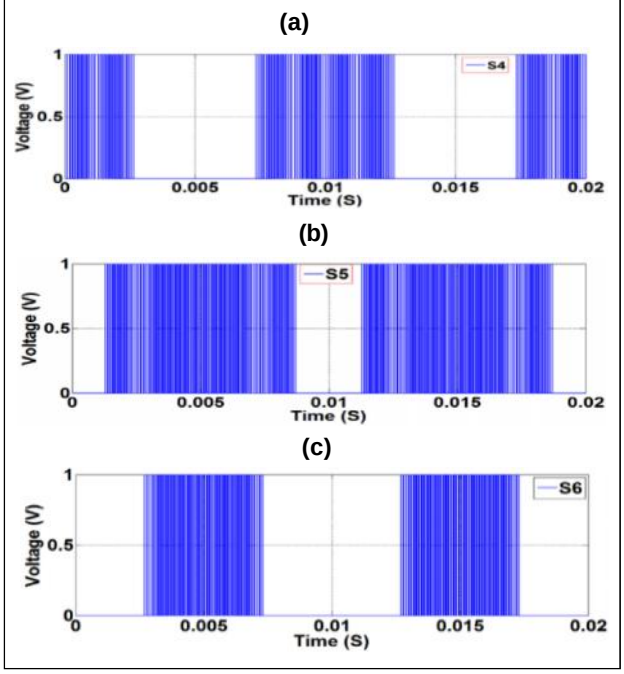


Figure 9: Simulation Result of Switching Pulse for H-Bridge Inverter

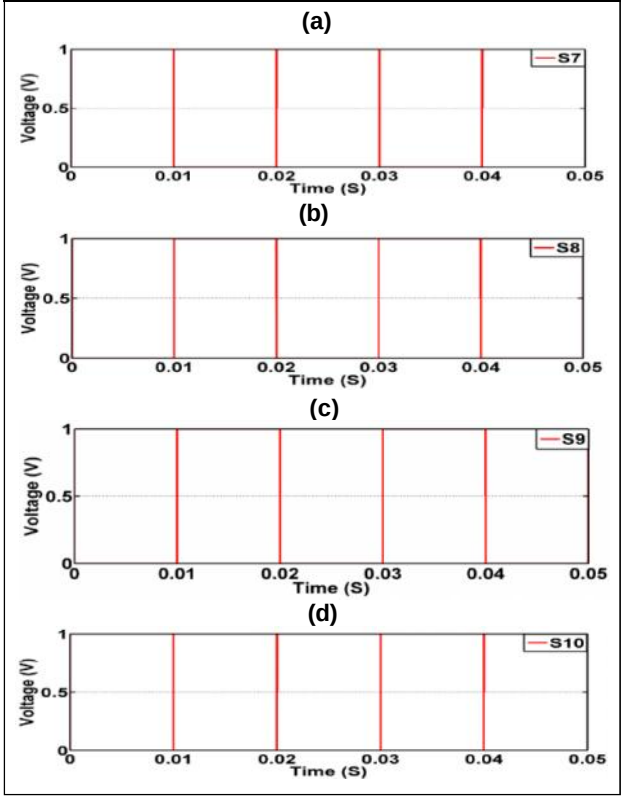


Figure 10: Simulation Result of Load Voltage and Load Current Without Filter

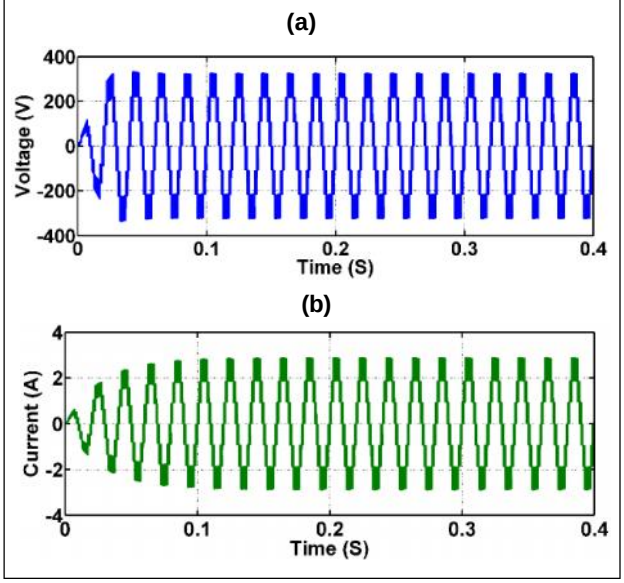


Figure 11: Simulation Result of Seven Level Output Voltage with and Without Filter

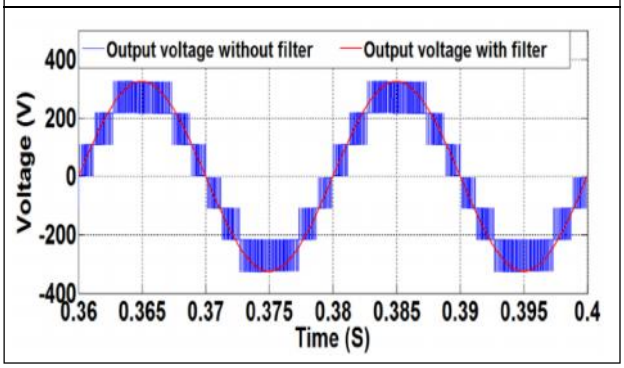


Figure 12: Simulation Result of Seven Level Output Current with and Without Filter

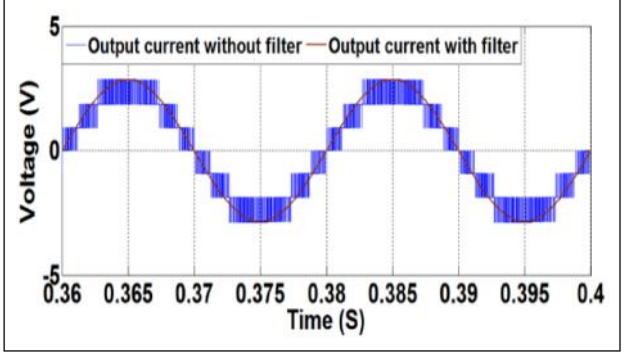


Figure 13: Harmonic Content of the Load Voltage and Load Current Without Filter

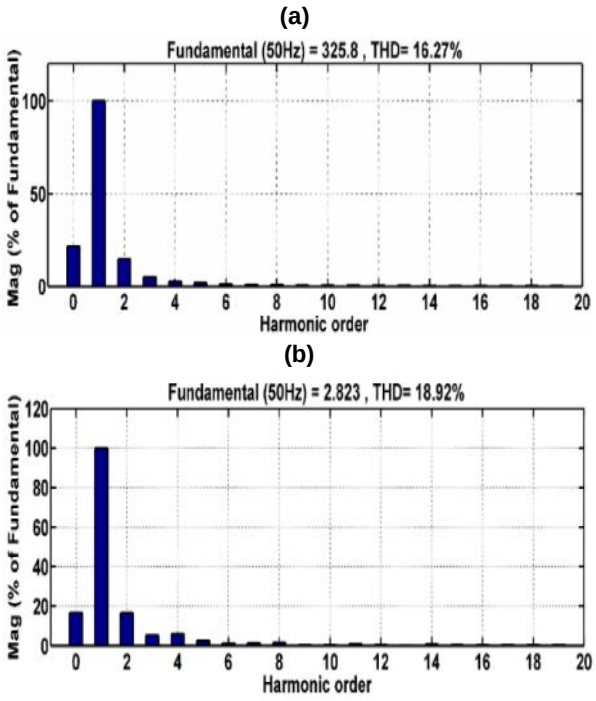


Figure 14: Harmonic Content of the Load Voltage and Load Current with Filter

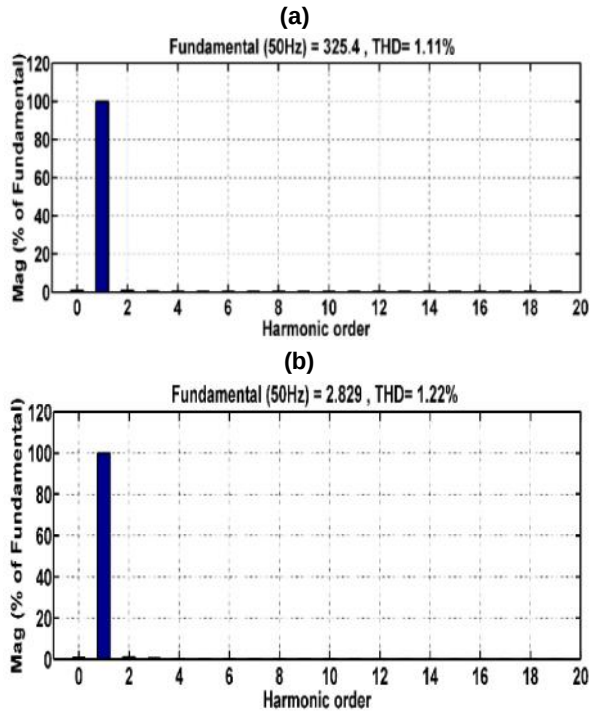


Figure 15: Experimental Result of Switching Pulse for Isolation Converters

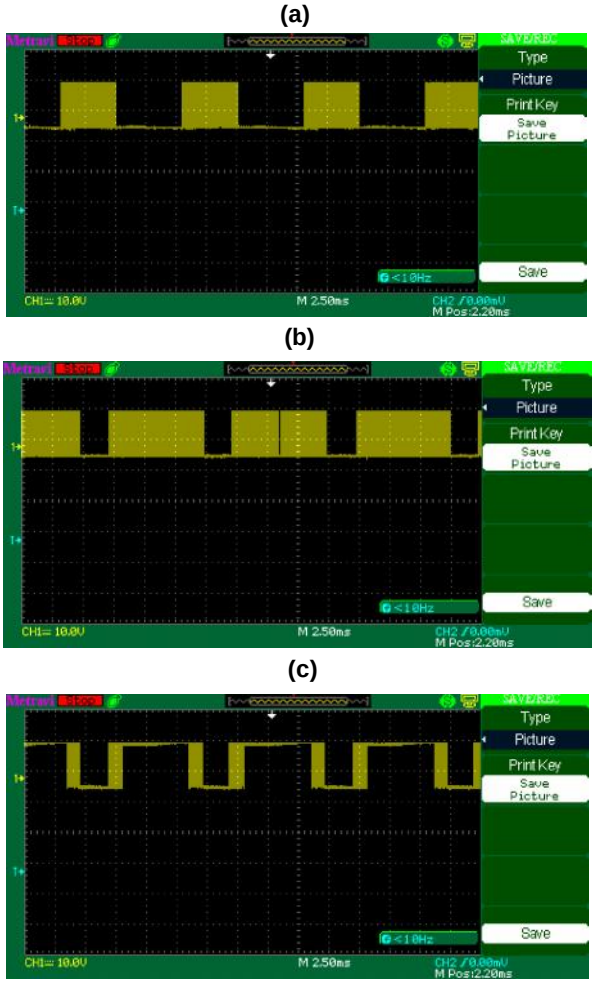


Figure 16: Experimental Result of Switching Pulse for H-Bridge Inverter

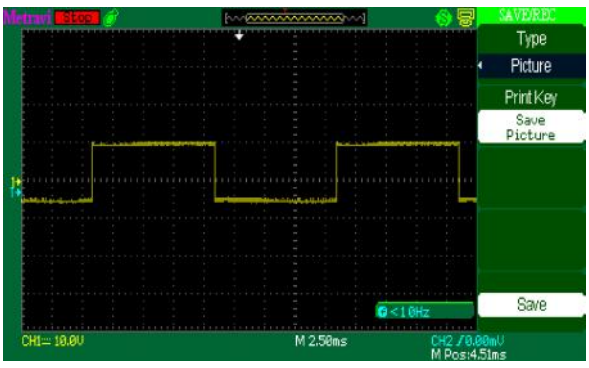


Figure 16 (Cont.)

(b)

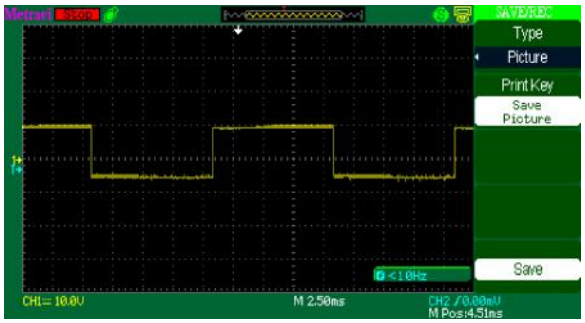
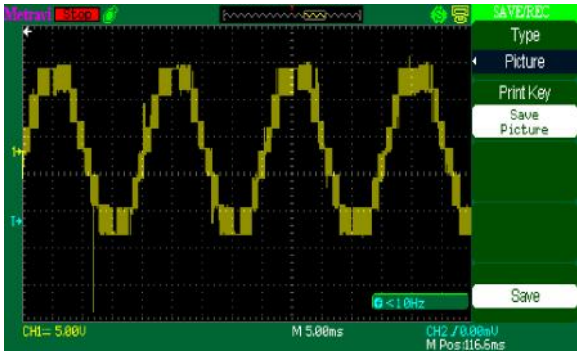


Figure 17: Experimental Result of Seven Level Inverter Output Voltage



experimental prototype is developed. The parameters of the prototype circuit are closed to simulation parameters. The switching patterns has been generated by using PIC16F877A microcontroller. The Figure 15 represents the switching pattern of isolation DC-DC converter. The H-bridge inverter switching signals are shown in Figure 16. The Figure17 depicts the load voltage of proposed system with filter.

CONCLUSION

This work proposed a seven level inverter with reduced number of power electronic components. This proposed system is observed to provide cost effective solution for renewable power generation, motor load, and grid connected system. This proposed model is adaptable to operate in varying input conditions. The main feature of this system is that voltage balancing has been achieved with a single DC source. Simulation results with V_{peak} 325 V V_{rms} 230 V has been carried out and has been compared with conventional seven level inverters such as cascaded H-bridge, diode clamped and flying capacitor. It is clearly observed that the proposed model outperforms the conventional inverters through the number of devices and the dc sources utilized. Similarly, experimental results with V_{peak} of 155 and 110 V_{rms} has been carried out to attain the desired seven level inverter result. SPWM has been done for both simulation and experimental set up to attain the desired gate pulses.

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