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Research Paper

SOFT SWITCHING CONTROL OF SYNCHRONOUS BUCK CONVERTER WITH ZCD CIRCUIT

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This paper aims to improve the efficiency of a dc-dc buck converter. It enables a synchronous rectifier buck converter to realize zero voltage switching in light load condition. The replacement of output rectifier diode by MOSFET can minimize conduction losses and increase the efficiency of the circuit. The control technique introduced in this paper enables a SR buck converter to carry out ZVS in light load condition to increase efficiency. No extra auxiliary switches or RLC passive components are required. It is of low cost and easy to control.

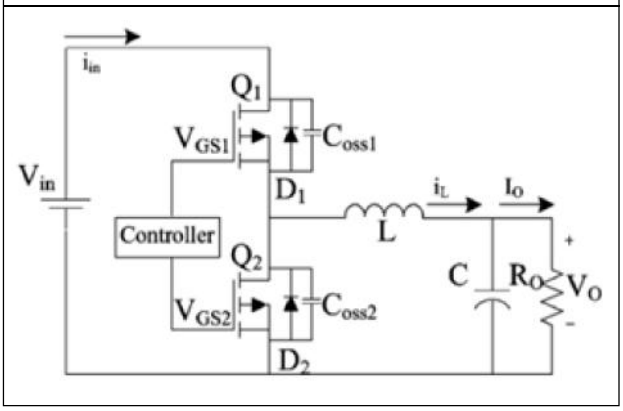
Keywords: Buck converter, Synchronous rectifier, ZVS, Light load condition

INTRODUCTION

Buck converters have already been applied to portable products which are powered by batteries. The efficiency of a buck converter should be increased to prolong the operation of portable products and minimize battery drain. The efficiency of a buck converter is affected by conduction losses. Switching loss of a buck converter must be decreased in light load condition. In order to reduce the conduction losses and raise the efficiency the SR technique is used.

In Figure 1 the basic circuit diagram of synchronous rectifier buck converter to have ZVS in light load condition is shown. A new control technique is proposed in this paper. It enables a SR buck converter to have ZVS function and increase efficiency in light load

Figure 1: Synchronous Rectifier Buck Converter



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condition without the need for extra auxiliary switches or RLC passive components. This new control technique is low cost and easy to control. Because the output rectifier diodes are replaced by MOSFET, conduction loss will be lower and the efficiency of the whole circuit will be higher. Figure 1 shows the circuit topology of a SR buck converter.

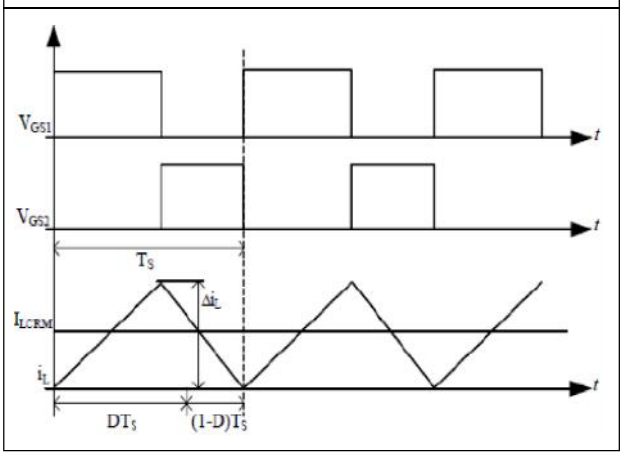
OPERATING PRINCIPLES

The oscillogram of the inductor current and switches when the SR buck converter is operated in critical-conduction mode (CRM) is shown in Figure 2. In CRM, the average inductive current IL of a SR buck converter can be represented by Equation (1), where T_S stands for switching frequency and *D.* For duty cycle.

$$I_{LCRM} = DT_s/2L(V_{in} - V_o) \quad ...(1)$$

In the equation, the SR buck converter is operated in Discontinuous Conduction Mode (DCM) if the mean value of the output current IO is lower than I_{LCRM}. However, T_S, V_{in}, V_o, L, and *D* remain unchanged. It is operated in a Continuous Conduction Mode (CCM) if the mean value of the output current IO is higher than ILCRM. Based on the descriptions above analysis, Equation (1) determines which mode the converter will be operated in, whether DCM or CCM.

Figure 2: Oscillogram of the Inductor Current and Switches



In Figure 2 the oscillogram of the inductor current and voltage across the switches are shown.

Two assumptions are made as follows to simplify the analysis:

1. The output voltage is assumed as a constant-voltage source because the output capacitance is large enough.
2. That no losses arise from any parts in the circuit is assumed. All the components are assumed to be ideal.

Modes of Operations in Light Load

State 1 (t_0 ~ t_1)

In this state, the main switch Q_1 is conducted, whereas the SR switch Q_2 is off. The input current iin flows through the inductor to the load. The conduction path is shown in Figure 3a. The inductor *L* is charged by $V_{in} - V_o$ at this time, whereas the inductor current $i_L(t)$ begins to increase linearly. The inductor current equation is:

$$i_L(t) = i_L(t_0) + \left(\frac{[V_{in} \vdash V_o]}{L}\right)(t - t_0) \quad ...(2)$$

State 2 (t_1 ~ t_2)

In State 2, the main switch Q_1 is turned off, whereas the Q_2 is conducted. The conduction path is shown in Figure 3b. As the inductor current is continuous, it flows through Q_2 to avoid the breakage of inductor current. The inductor *L* is discharged by $-V_o$ at this time,

and the inductor current iL begins to decrease linearly. The inductor current equation in this state is:

$$i_L(t) = i_L\,(t_1) + \left|-\frac{V_o}{L}(t - t_0)\right| \quad ...(3)$$

and the parasitic capacitor voltage equation is:

$$V_{Coss1}(t) = V_{in} \quad ...(4)$$

State 3 (t_2 ~ t_3)

The inductor current has already dropped to 0 at t_2. The SR switch Q_2 is turned off to avoid energy losses of the buck converter. The conduction path is shown in Figure 3c. In this state, the inductor *L* start to resonant with the parasitic capacitor *Coss* of switch Q_1 and Q_2, this enables C_{oss1} to be discharged and C_{oss2} to be charged. The $i_L(t)$ and V_{Coss2} can be calculated as follows:

$$i_L(t) = -\frac{V_0}{Z}\sin\omega(t - t_2) \quad ...(5)$$

$$v_{coss\,1}(t) = [V_{in} - V_o] + V_o\cos\omega(t - t_2) \quad ...(6)$$

State 4 (t_3 ~ t_4)

In State 4, the switch Q_1 keeps turning off, whereas the SR switch Q_2 is conducted. The conduction path is shown in Figure 3d. As a result, the inductor voltage is $V_L = -V_o$, this enables the inductor *L* to be charged and the inductor current to increase linearly in the opposite direction. The current $i_L(t)$ at this time is:

$$i_L(t) = -\frac{V_o}{L}(t - t_3) \quad ...(7)$$

The parasitic capacitor voltage $V_{Coss1(t)}$ of switch Q_1 is

$$v_{coss\,1}(t) = V_{in} \quad ...(8)$$

State 5 (t_4 ~ t_5)

State 5 is the duration for resonance. The switch Q_1 and the SR switch Q_2 are both turned off. The conduction path is shown in Figure 3e. The SR rectifying switch is turned off, whereas the inductor current must be continuous. This current will discharge to C_{oss1} and charges to C_{oss2} until the voltage of C_{oss1} is discharged to 0, and the voltage of C_{oss2} is charged from 0 to V_{in}. The $i_L(t)$ and $V_{Coss1(t)}$ of switch Q_1 are calculated as follows:

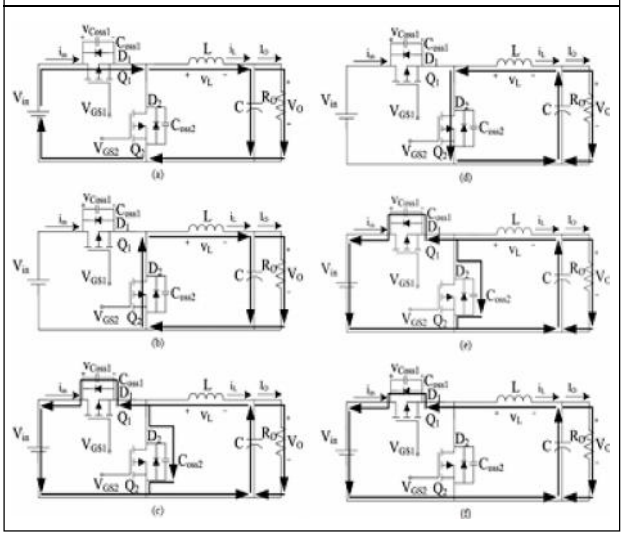
$$i_L(t) = -\frac{V_o}{Z}\sin\omega(t - t_4) \quad ...(9)$$

$$v_{coss\,1}(t) = \frac{[V_{in} - V_o]}{L}(t - t_4) \quad ...(10)$$

State 6 (t_5 ~ t_6)

In State 6, the main switch Q_1 and the SR switch Q_2 are continuously turned off. However, C_{oss1} has been discharged, and C_{oss2} has been discharged by inductor current. The body diode D_1 is then conducted. The conduction path is shown in Figure 3f. In this state, the

Figure 3a-f: The Six Operation States of the Control Technique for the Synchronous Rectifier Buck Converter Proposed in this Paper



zero voltage condition of Q_1 has been completed. The $i_L(t)$ and $V_{Coss1(t)}$ of switch Q1 are calculated as follows:

$$i_L(t) = i_L(t_5) + \frac{[V_{in} - V_o]}{L}(t - t_5) \quad ...(11)$$

$$v_{coss\,1}(t) = 0 \quad ...(12)$$

In Figure 3a-3f the six operation states of the control technique for the synchronous rectifier buck converter proposed in this paper is shown. According to the previous description, the SR buck converter is operated in DCM in light load condition. When the inductor current is lower than 0, the SR switch Q_2 remains to be turned on. That will result in the decrement in conversion efficiency of the SR buck converter. The second conduction of SR switch Q_2 in one switching cycle enables the main switch Q1 to be turned on with ZVS and increase the efficiency in light load condition. In conclusion, the control technique proposed in this paper has the following advantages. When the SR buck converter is operated in heavy load condition, the SR technique can be used to reduce conduction losses. In contrast, the ZVS technique can be adopted in light load condition to reduce switching losses.

Conditions for ZVS in Light Load Condition

To attain the ZVS of main switch Q_1 in light load condition, the inductor L must store enough energy to let the parasitic capacitor of switch Q_1 be discharged completely in State 4. Therefore, the energy E_L stored by inductor has to be higher than E_{Coss1} stored by capacitor. This can be represented by the following equation (ILP) is the peak value of inductor current:

$$(i_{Lp})^2 \times L \geq C_{oss1}(V_{in})^2 \quad ...(13)$$

The pulse duration for State 4 can be calculated using Equation (11):

$$t_{43} \geq \frac{\sqrt{LC_{oss\,1}} \times V_{in}}{V_0} \quad ...(14)$$

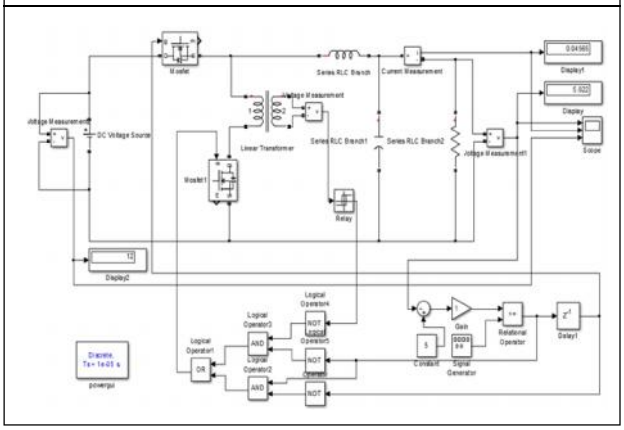
In order to attain the ZVS of switch main Q_1, the switch Q_1 in State 6 must be conducted. If the Q_1 is not conducted, the inductor current will charge to C_{oss1} again in the positive direction, thus the ZVS of main switch Q_1 may fail. The delay time from State 5 to State 6 is critical to the ZVS function of main switch Q_1. The optimal delay time is 1/4 of the resonance cycle. It is represented by the following equation:

$$T_{delay} = \frac{2\pi\sqrt{LC_{oss\,1}}}{4} = \frac{\pi}{2}\sqrt{LC_{oss\,1}} \quad ...(15)$$

SIMULATION MODEL AND RESULTS

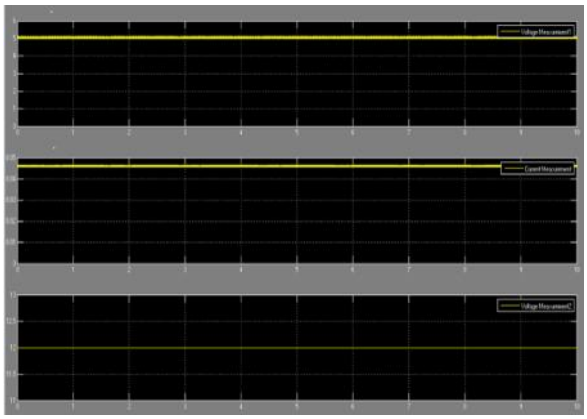
The proposed DC-DC converter is simulated using MATLAB and the results are presented here.

Figure 4: Control Circuit Structural Diagram of a Synchronous Rectifier Buck Converter



Below Figure 5 shows Output voltage, Output current and Input voltage.

Figure 5: Simulation Output Voltage, Current and Input Volltage



Disadvantages of Conventional Buck Converter

- Losses due to resistance when the transistor switch is conducting.
- Diode forward voltage drop (usually 0.7 V or 0.4 V for schottky diode)
- Loss in Inductor winding resistance.
- Loss in Capacitor equivalent series resistance.
- Noise and voltage ripple.
- Low efficiency.

Advantages of Proposed Buck Converter

- MOSFET RDSon is very less.
- Diode is replaced by MOSFET.
- Proposed control technic is simple and low cost.
- Noise and ripple are reduced.
- No extra auxillary switches and RLC passive components are used.
- ZVS is attained to reduce switching losses.
- Increased efficiency.

CONCLUSION

In this paper, the control technique applicable to a SR buck converter is proposed, and the analysis of its operating principles is discussed. The control method proposed herein has two advantages. First, due to the SR technique proposed in the paper, the diode of output rectifier can be replaced by a MOSFET. This will help to reduce conduction losses and increase the conversion efficiency of the converter. Second, when the converter is operated in light load condition, ZVS will be achieved successfully without any auxiliary switch or passive component(R, L, C). In other words, there is no need to add extra cost in the converter, and the conversion efficiency of the converter can also be increased in light load condition.

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