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*Research Paper*

# MODELING AND ANALYSIS OF 5-LEVEL H-BRIDGE INVERTER-FED SWITCHED RELUCTANCE MOTOR

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This paper presents the modeling and analysis of H-bridge Inverter-fed Switched Reluctance Motor. This project proposes the performance characteristics of 5-Level H-bridge inverters. The H-bridge inverter is triggered by multi-carrier sinusoidal pulse width modulation technique. The performance of the inverter is studied for different modulation indices. The open loop response of the switched reluctance motor is observed for varying torque conditions.

Keywords: 5-level H-bridge inverter, Multi-carrier SPWM, Switched reluctance motor, THD

## INTRODUCTION

Power electronic speed controlling devices are becoming popular in the industry due to their reliability and efficiency under working conditions. In recent years high-power and medium-voltage drive applications have been installed. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level H-bridge inverters are receiving great deal of attention in the past few years. The multilevel H-bridge inverter was brought into use so as to obtain a higher converter operating voltage for overcoming the difficulties faced by classical semiconductors. The multilevel H-bridge voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Multilevel H-bridge inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages. The principle advantage of using multilevel H-bridge inverters is the low harmonic distortion

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obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used. The performance of an inverter is based on the harmonic content in its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms. There are many techniques, which are applied to multilevel inverter topologies. Pulse Width Modulation (PWM) is a widely used technique to control the output of static power inverters. PWM inverters can control their output voltage and frequency simultaneously. The different PWM schemes are discussed in [1]. New cascade H-bridge inverter efficiency is reported in [2]. The number of switches and sources are reduced with new cascade multi-level Inverter are modified in [3]. Multilevel Strategy in SPWM Design as a reported [4]. Multi carrier PWM for multilevel inverters and strategies are discussed in detail [5].Multilevel Converters and power converter details are analysed in [6]. Multi-Phase VSI with Simple PWM Switching Techniques performance is investigated in [7]. Multilevel voltage source converter topologies for industries in medium voltage drives are detailed in [8]. Inverted Sine Carrier for fundamental fortification in PWM Inverters and FPGA based implementations are reported and implemented in [9]. The switched reluctance machine modeling and control is proposed in [10]. Switched reluctance motor drive and voltage-ampere requirements are discussed in [11]. The aim of this project is to design and analyze the performance of 5-Level H-bridge inverter fed switched reluctance motor using PWM technique.

## POWER CIRCUIT OF 5 LEVEL H-BRIDGE INVERTER

Figures 1 and 2 shows the power circuit and block diagram of n-level H-bridge voltage source inverter, The input Dc supply is observed from the AC source. The output is given to the three phase H-bridge inverter. The output of the VSI is connected to the three-phase SRM drive. The n-level inverter switches are triggered by multi carrier SPWM technique. The switches in the voltage source inverter can be turned on and off as required. In the simplest

Figure 1: Power Circuit of 5 Level H-bridge Inverter

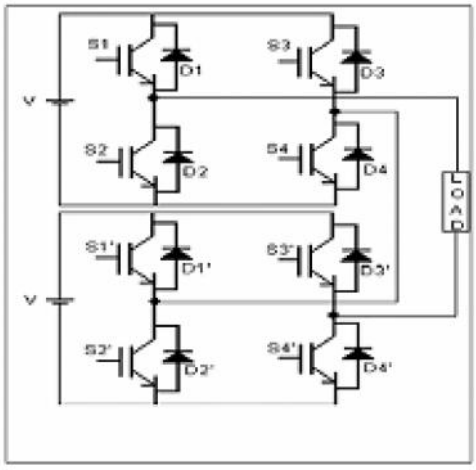
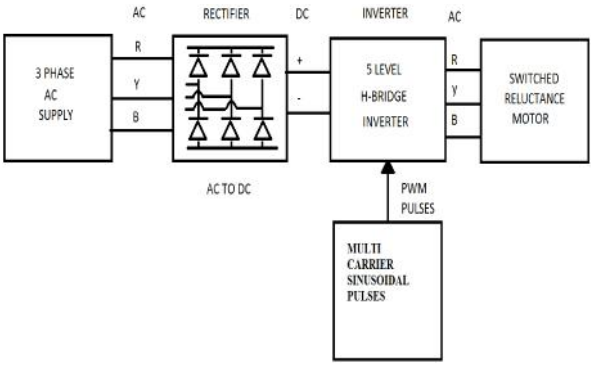
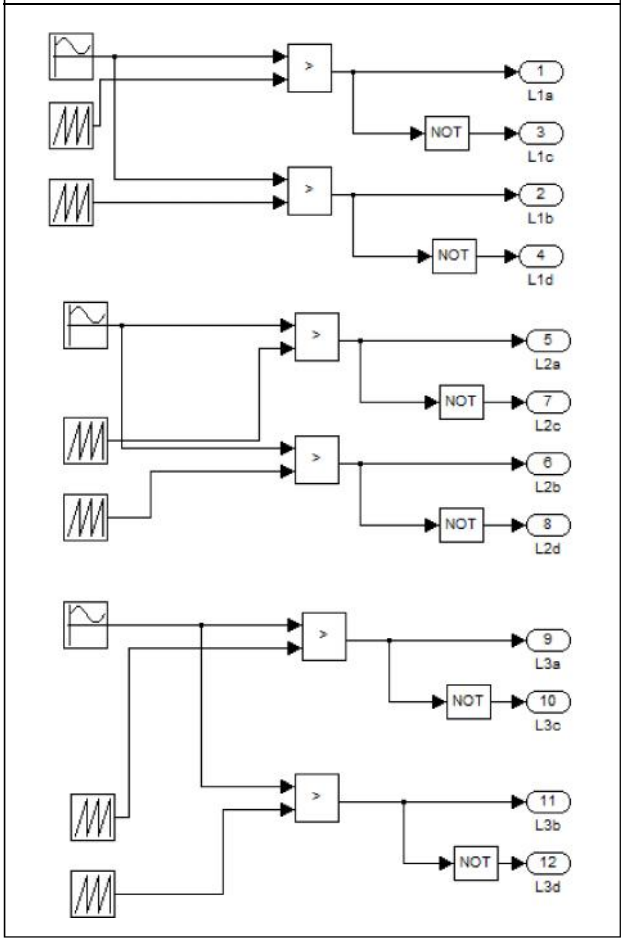



Figure 2 Block Diagram Representation of H-bridge Inverter Fed Switched Reluctance Motor



approach, the top switch is turned on and off only once in each cycle, a square wave waveform results. However, if turned on several times in a cycle an improved harmonic profile may be achieved. In the most straightforward implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as depicted schematically in Figure 3. The fundamental frequency is 50 Hz, the carrier frequency is greater than fundamental frequency. The MI is ratio of amplitude of fundamental to the amplitude of carrier waveform.

Figure 3: Multi-Carrier Sinusoidal Pulse Width Modulation




## DESCRIPTION OF H-BRIDGE INVERTER

The smallest number of voltage levels for a multilevel inverter using cascaded- inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Figure 4. The inverter circuit consists of four main switches and four freewheeling diodes

According to four-switch combination, three output voltage levels, +V, -V, and 0, can be synthesized for the voltage across A and B. During inverter operation shown in Figure 4, switch of S1 and S4 are closed at the same time to provide VAB a positive value and a current path for Io. Switch S2 and S4 are turned on to provide VAB a negative value with a path for Io. Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes. When all switches are turned off, the current will flow through the freewheeling diodes. In case of zero level, there are two possible switching patterns to synthesize zero level, for example, 1) S1 and S2 on, S3 and S4 off, and 2) S1

Figure 4: H-bridge Cell

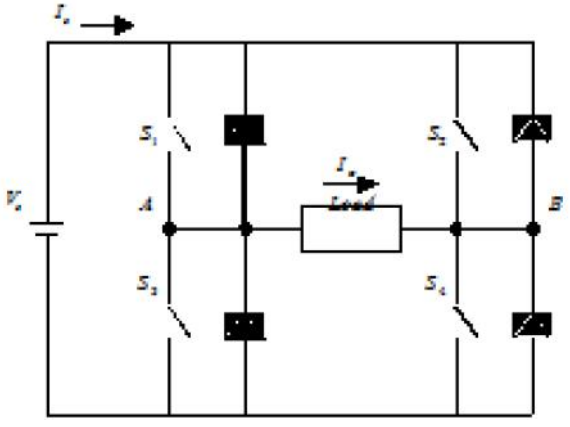
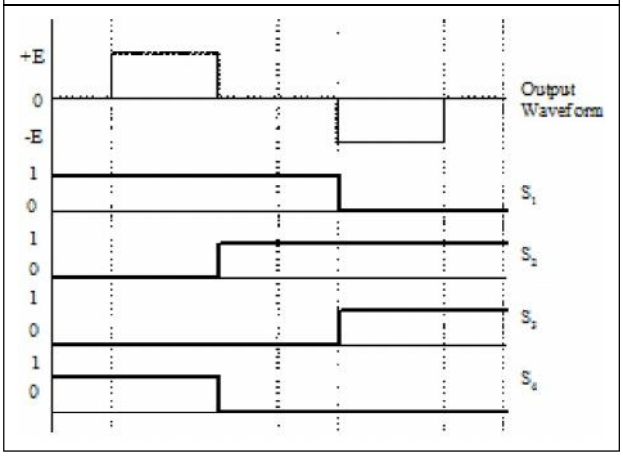


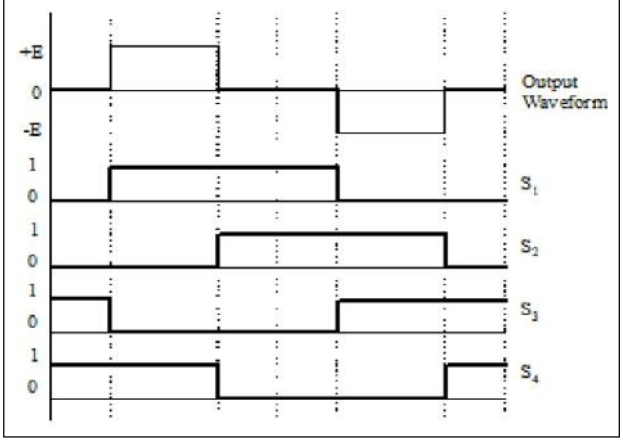
Figure 5: Repeated Zero Level Switching Pattern




and S2 off and S3 and S4 on. A simple gate signal, repeated zero-level patterns, is shown in Figure 5. All zero levels are generated by turning on S1 and S2.

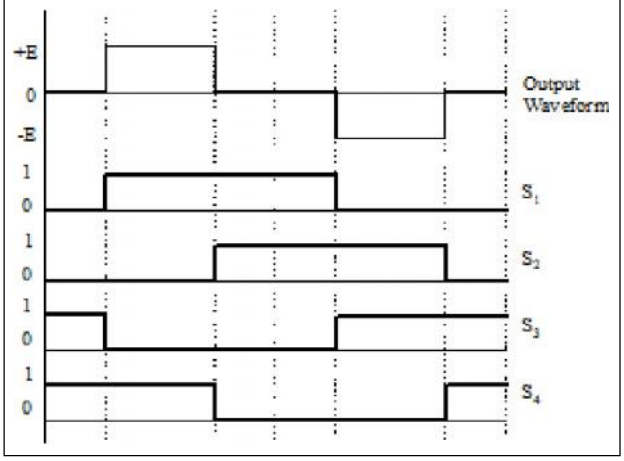
Note that level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. In Figure 6, S1 and S2 are turned on longer than S3 and S4 do in each cycle because the same zero level switching pattern is used. As a result, S1 and S2 are consuming more power and getting higher temperature than the other two switches. To avoid such a problem, a different switching pattern for zero level is applied. In the first zero stage, S1 and S2 are turned on; then, in the second zero stage, S3 and S4 are turned on in stead of S1 and S2. By applying this method, turn-on time for each switch turns out to be equal, a shown in Figure 2.3.

Figure 6: Swapped Zero Level Switching Pattern Blanking Time




Another issue that has to be concerned is providing blanking time for gate signal. In practice, switching devices are not ideal. To completely turn-off the devices, a short period, which depends on the type of the device, is needed. Usually, because of the finite turn-off and turn-on times associated with any types of switch, a switch is turned off at the switching time instant. However, the turn-on of the other switching in that inverter leg is delayed by a blanking time, *t*, which is conservatively chosen to avoid cross-conduction current through the leg. A blanking time concept is illustrated in Figure 7.

Figure 7: Blank Time to Gate Signal




## MODELLING OF SWITCHED RELUCTANCE MOTOR

A mathematical model for the switched Reluctance motor used for the design of the speed contour. The mode1 is represented by a set of differential equations which are

obtained using standard electric circuit and machine theory. In order to include all relevant dynamics, the plant is modeled as a combination of two subsystems: an electric subsystem derived from Kirchhoff s laws, which describe the dynamic behavior of the stator. and a mechanical subsystem derived from Newton's law, which accounts for the mechanical load and the rotor dynamics. The two subsystems are coupled together by energy conversion consideration. Voltage relations for a switched reluctance motor are the same as for any other electrical machine. ie., the voltage applied to the stator terminals equals the sum of a voltage drop due to resistive losses and the induced voltage due to flux Linkage variations. Therefore the voltage equation for the k phase of an SRM will be:

$$V_k = ri_k + \frac{d \cdot_k (\bar{}_k, i_k)}{dt} \qquad ...(1)$$

Since $\cdot_k$ is a function of $\bar{}_k$ and $i_k$ Equation (1) cm be expanded using the partial derivatives of $\bar{}_k$ to yield:

$$v_k = ri_k + \frac{\partial \cdot_k (\bar{}_k, i_k)}{\partial \bar{}_k} \frac{d\bar{}_k}{dt} + \frac{\partial \cdot_k (\bar{}_k, i_k)}{\partial i_k} \frac{di_k}{dt} \qquad ...(2)$$

## SIMULATION RESULTS

The H-bridge inverter-fed SRM drive is simulated with the above said switching scheme and the results are observed. The switching frequency of the VSI is chosen as 10 kHz and the fundamental frequency is set to 50 Hz. Figure 8 shows the Simulink model of 5-level H-bridge inverter-fed SRM. The Figures 9 and 10 shows the simulation results for 5-level H-bridge voltage source inverter. Figure 9 shows the phase voltage of 5 level

Figure 8: Simulink Diagram of 5-Level H-bridge Fed Switched Reluctance Motor

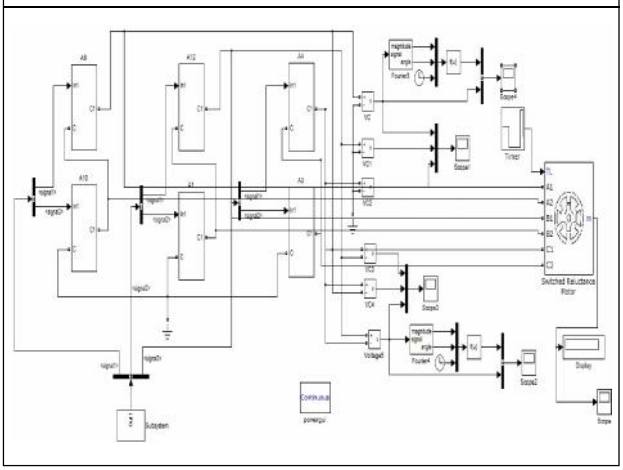


Figure 9: Phase Voltage of 5 Level Inverter at Modulation Indices 1 Condition

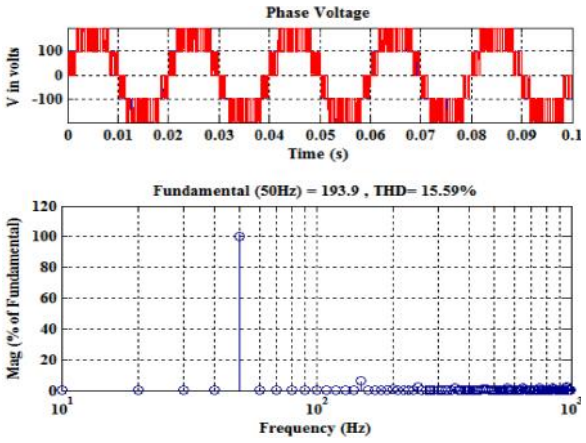
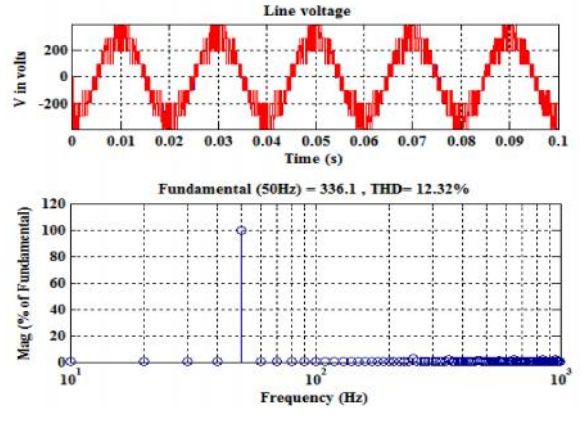



Figure 10: Line Voltage of 5 Level Inverter at Modulation Indices 1 Condition



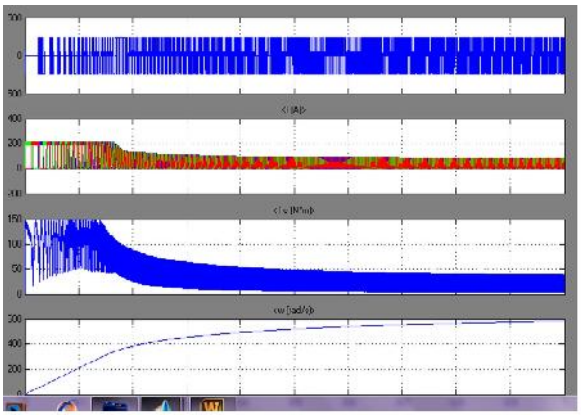
inverter at modulation indices 1 condition. It is seen that phase rms is 137 V and THD is 15.59%. Figure 10 shows the simulation results of line voltage of 5 level inverter at modulation indices 1 condition. It is seen that line voltage rms is 237.3 V and THD is 12.32%. Table 1 shows the simulation results for different 5-level H-bridge inverter. It seen that when increasing modulation Indices the THD is reduced and the fundamental voltage is increased. Figure 10 shows the 5-level voltage source inverter fed SRM drive results. It is observed that in the no load condition the corresponding stator current, speed and motor torque are found. From the simulation results the motor torque follows the load torque.

Table 1: 5-Level H-bridge Inverter Results for Different Modulation Index Condition

| MI | Vph | | Vl | |
|---|---|---|---|---|
| | rms | THD% | rms | THD% |
| 0.2 | 30.76 | 87.72 | 52.82 | 76.47 |
| 0.4 | 79.35 | 20.00 | 106.1 | 34.49 |
| 0.6 | 93.30 | 19.97 | 161.6 | 25.09 |
| 0.8 | 119.74 | 19.94 | 207.4 | 19.07 |
| 1 | 137.7 | 15.59 | 237.3 | 12.32 |

Figure 11: Open Loop Response of 5-Level Inverter Fed SRM Drive Under No Load Condition

Figure 12: Open Loop Response of 5-level Inverter Fed SRM Drive Under Rated Condition



Similarly it is repeated for rated torque condition.

## CONCLUSION

This paper discusses the modeling and analysis of 5-level H-bridge inverter fed SRM. The inverter-fed SRM is developed in matlab/ simulink environment. The performance of the inverter is found for different modulation indices. From the simulation results increase in modulation index decrease in THD increase in fundamental voltage is observed. The inverter fed SRM is developed and open loop results are analyzed for different load conditions.

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