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Research Paper

SIMPLIFIED 7 LEVEL MULTILEVEL INVERTER

Jithin Baby[1]* and Bharathi A Rao[1]

*Corresponding Author: Jithin Baby, ✉ jbstations@gmail.com

The power electronic converter which converts DC power to AC power at required voltage and frequency is known as Inverter. Inverters with different levels of output voltage and current are called Multilevel Inverter. Multilevel inverter have very high efficiency and their output waveform almost reaches sinusoidal in shape as the number of levels are increased. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and complex control circuitry. This work highlights a multilevel inverter using an H-bridge output stage with two bidirectional auxiliary switches. It also achieves a significant reduction in number of power devices used. A 7-Level Multilevel inverter is discussed in this paper. The proposed inverter circuit is simulated using Matlab/Simulink tool and the results are obtained.

Keywords: Multilevel inverter, Converter, Reduced switches, MOSFET's, H-Bridge, MATLAB/ Simulink

INTRODUCTION

In recent years, a lot of revolution has occurred in the field of power electronics. All these advancements in this field have been evolved to improve the efficiency, reduce the complexity and also to reduce the cost. One such major change that has happened in converter or inverter field is the introduction of multilevel inverter.

Early inverters had only two output voltage or current levels 0 or ±Vdc. Since only two output levels, they were called two-level inverter. But to obtain quality output voltage or current waveform, they required high switching frequency along with various Pulse Width Modulation (PWM) techniques. This disadvantage possessed a limitation to inverter to high power and high voltage application [4].

To overcome these problems multilevel inverters have evolved. The multilevel inverter have given a big boost in the power industry. They present a new set of features that are switched for use in reactive power compensation. It is also easy to obtain high power, high voltage inverter with multilevel structure. This multilevel structure allows inverter to obtain high voltages with low harmonics. As the number of voltage levels

[1] Department of Electrical and Electronics, St. Joseph Engineering College, Vamanjoor, Mangalore, India.

increases, the harmonic content of the output voltage waveform decreases significantly. The effect of the lower order harmonics can be eliminated with increase in output voltage levels. This structure of the multilevel inverter produces a near sinusoidal voltage from different levels of DC voltage, which may be obtained from the capacitor connected across the DC voltage source.

Generally the multilevel inverters were classified into [4],

- Diode clamped multilevel inverter.
- Flying capacitor multilevel inverter.
- Cascaded H-bridge multilevel inverter.

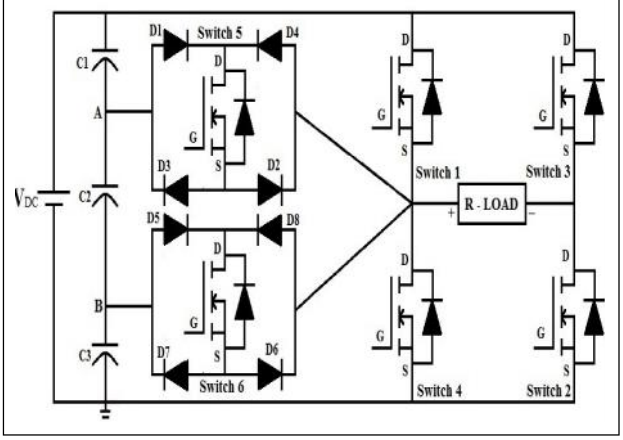
All the above introduced multilevel inverter topologies have certain limitations like complex circuits, requiring high number of power switches and high cost as lot of switches, capacitors and diodes were used.

To overcome all these limitations new topology of multilevel inverter has been presented here. This new topology can be implemented with a five-level waveform and can be extended to obtain any number of levels of output waveform. To obtain a smooth waveform with reduced lower order harmonics, a seven-level multilevel inverter is introduced in this paper. This new topology is simulated using MATLAB/Simulink simulation software and simulation results prove that, the design ideas work as expected.

CIRCUIT OF NEW PROPOSED TOPOLOGY

Figure 1 shows the complete circuit of the new Multilevel Inverter topology. The H-Bridge is formed by connecting MOSFET switches 1 to 4. Capacitor voltage divider is formed by

Figure 1: Circuit of New Topology



capacitors C1, C2 and C3 [1]. It will provide all the voltage levels required by the multilevel inverter for its operation. Two auxiliary switches 5 and are connected between positive terminal of load and nodes A and B respectively. Diodes D1 to D4 are connected to switch 5 and diodes D5 to D8 are connected to switch 6 to obtain a proper conduction path to obtain various output levels.

OPERATION OF NEW PROPOSED TOPOLOGY

The circuit works in seven different levels. All the different levels and the corresponding switching combination are shown below.

Figure 2: Output Voltage at +Vdc/3

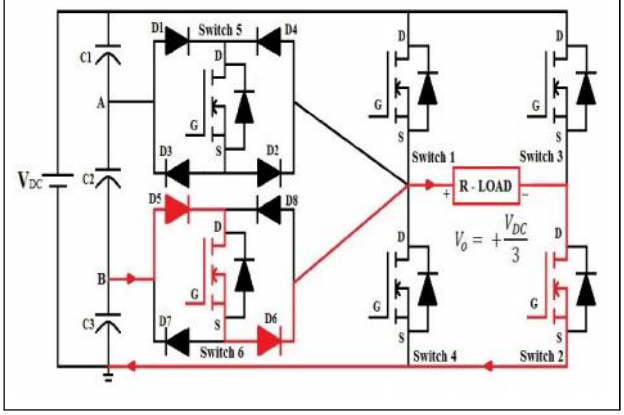


Figure 3: Output Voltage at +2Vdc/3

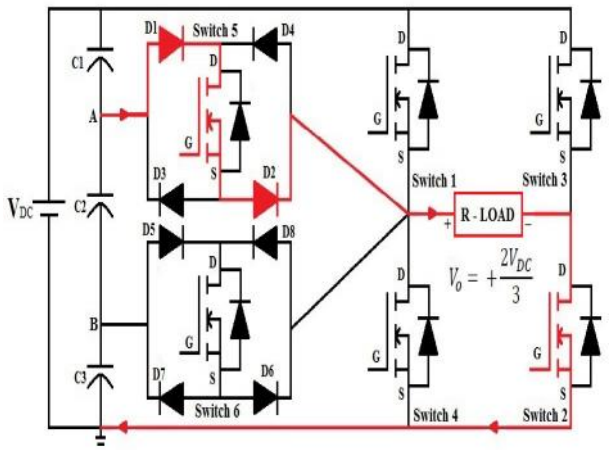


Figure 4: Output Voltage at +Vdc

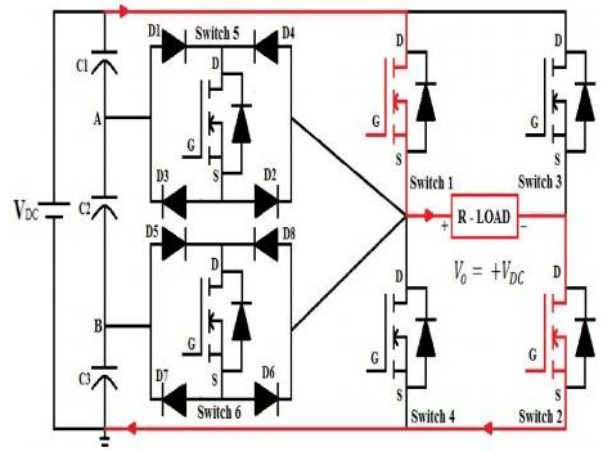
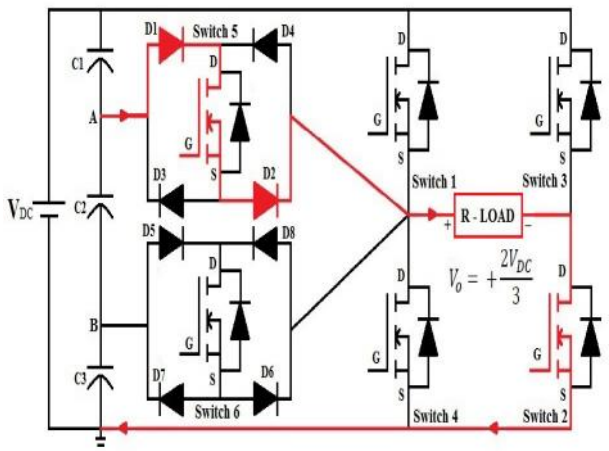


Figure 3: Output Voltage at +2Vdc/3



Output Voltage: +Vdc/3

To obtain an output voltage level of +Vdc/3, switch 2 and auxiliary switch 6 must be switched ON such that it connects the positive load terminal to node B and negative load terminal to ground as shown in Figure 2. Diodes D5 and D6 conduct during this time.

Output Voltage: +2Vdc/3

Figure 3 shows the switches which are turned ON to obtain output voltage level of +2Vdc/3. Switch 2 and auxiliary switch 5 are turned ON. Node A is connected to positive load terminal and negative load terminal is connected to ground. Diodes D1 and D2 conduct at this interval.

Output Voltage: +Vdc

Maximum positive output voltage +Vdc is obtained when switches 1 and 2 from H-Bridge are turned ON. The switching combination and current path required to obtain this voltage level is as shown in Figure 4. The positive terminal of load is connected to positive terminal of the DC Source and negative terminal is connected to the ground.

Output voltage: -Vdc/3

Figure 5 shows the switches that are turned ON to obtain output voltage level of -Vdc/3. Switch 2 and auxiliary switch 5 form the conducting path to obtain the required output voltage level. Diode D3 and Diode D4 also conduct during this time. Positive load terminal is connected to node A and negative terminal of load is connected to positive terminal of DC voltage source.

Output Voltage: -2Vdc/3

Output voltage level of -2Vdc/3 is obtained by turning ON switch 3 and auxiliary switch 6.

Figure 5: Output Voltage at -Vdc / 3

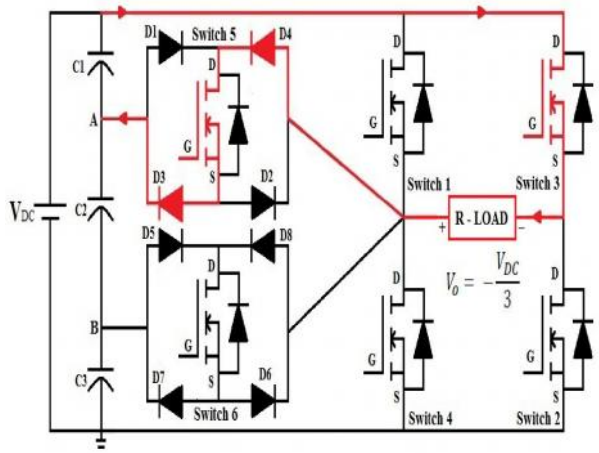


Figure 6: Output Voltage at -2Vdc / 3

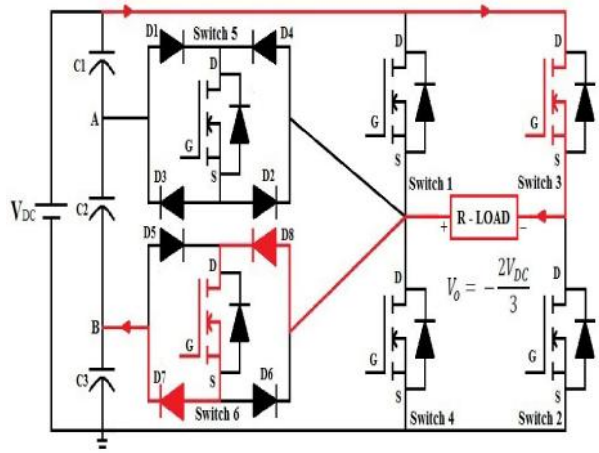


Figure 7: Output Voltage at –Vdc

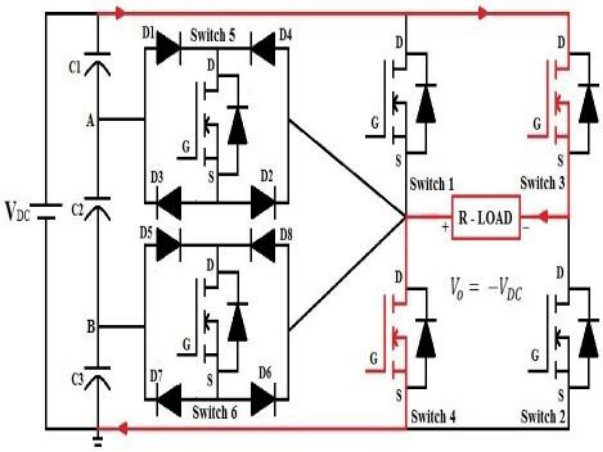


Figure 6 shows the conduction path. Diode D7 and D8 also conduct and it connects Node B to the positive terminal of the load.

Output Voltage: -Vdc

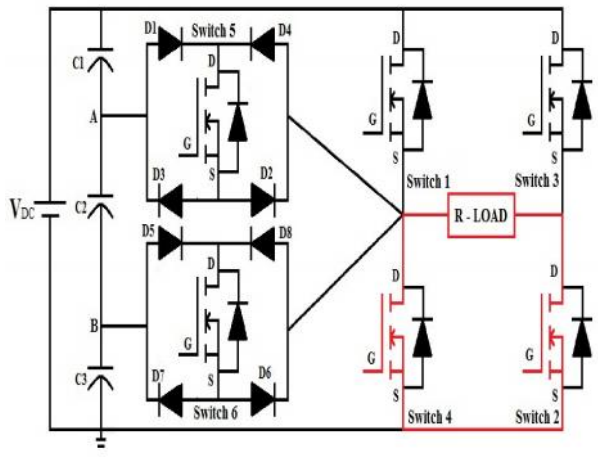
Maximum negative output voltage -Vdc is obtained when switches 3 and 4 from H-bridge are turned ON. The complete conduction path is shown in Figure 7. The positive terminal of the load is connected to ground and negative terminal is connected to the positive side of the DC source.

Output Voltage: Zero

Since this paper discusses the operation of new topology for resistive load, there will not be any inductive current flowing in the circuit. Hence by turning OFF every switch in the circuit zero output can be obtained. Further, if Inductive load is being used, then by switching ON switches 2 and 4 from H-Bridge, the load will be connected to ground and any inductive current present can be eliminated and zero output voltage can be obtained.

In this configuration the three capacitors in the capacitive voltage divider are connected

Figure 8: Zero Output Voltage Level



directly across the DC bus or voltage source, and since all switching combinations are activated in an output cycle, the dynamic voltage balance between the three capacitors is automatically restored [2].

Figure 9 shows the expected seven level output voltage. All the seven levels are marked in the waveform. One complete cycle (0 to 2ð) is divided into twelve equal parts to obtain a symmetrical output waveform. For an input DC voltage of 30 V, the seven output levels of voltages are 0, +10 V, +20 V, +30 V, -10 V, -20 V, -30 V. To obtain a 50 Hz output the total time period of one cycle is taken and it is divided into twelve halves and by using the switching sequence given in Table 1, the switches are turned ON to obtain the waveform as expected in the given Figure 8.

Figure 9: Seven Level Output Waveform

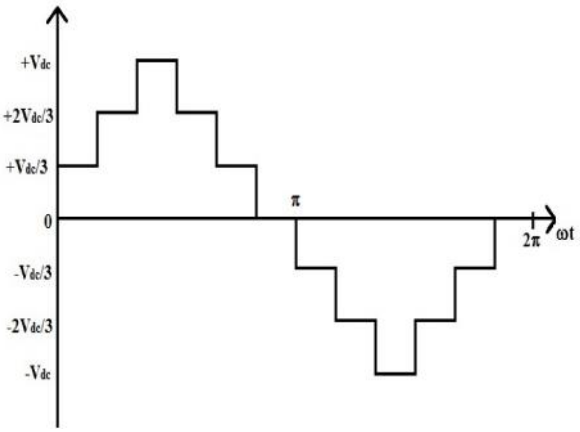


Table 1: Switching Combination Required to Generate 7-Level Output Voltage Waveform

S-1	S-2	S-3	S-4	S-5	S-6	Vo
ON	OFF	OFF	ON	OFF	OFF	+Vdc
OFF	OFF	OFF	ON	ON	OFF	+2Vdc/3
OFF	OFF	OFF	ON	OFF	ON	+Vdc/3
OFF	OFF	ON	ON	OFF	OFF	0
OFF	ON	OFF	OFF	ON	OFF	-Vdc/3
OFF	ON	OFF	OFF	OFF	ON	-2Vdc/3
OFF	ON	ON	OFF	OFF	OFF	-Vdc

Table 1 shows the switching combinations required to obtain seven levels of output voltage. Switches 1 to 6 are mentioned as S-1 to S-6 in the table and output voltage is denoted as *Vo*.

Table 2 clearly illustrates that the new proposed configuration has significant advantage over the other multilevel inverter topologies that are presently being used [1]. Though there are several advantages, each switch in this topology is required to block a voltage of Vs/2 [1].

Table 2: Comparison Between Four Different 7-Level Inverters Topologies

Multilevel Inverter Type	New Topology	Diode Clamped	Capacitor Clamped	Cascaded H-Bridge
Total Switches	6	36	36	36
Total Diodes	8	72	36	36
Total Capacitors	3	7	17	9

It can be seen that only six controlled switches are required for this configuration whereas thirty six switches are required by all other configurations. It means that there is a significant reduction (83%) of switches in this new proposed topology [1].

It is also to be noted that the passive components used by the proposed topology is very much lesser than the other three topologies. It uses only eight diodes whereas the next best topology uses thirty six diodes. Hence a 78% reduction of diodes can be

achieved from this topology. The total number of capacitors used in this proposed topology is only three compared to the other best topology which uses seven capacitors. Hence a 43% reduction in use of capacitors is achieved.

SIMULATION RESULTS

As the first step in the testing of the new seven level converter, the simulation of this proposed new topology is carried out using a computer-aided simulation tool to verify the validity of the circuit. The simulation is done using Matlab/ Simulink. The circuit is simulated with an input DC voltage of 30 V.

The Switches are controlled by giving signals by the pulse generator blocks in the simulation. Pulses to switches given are shown in below Figure 10. From the Figure 10, it can be seen that, switch 1 is turned ON only once in one cycle as required by the operation of new topology. Pulses to other switches given can also be seen and it is given as required by the new topology for its proper operation to get the seven output levels.

Figure 10: Pulses to Switches

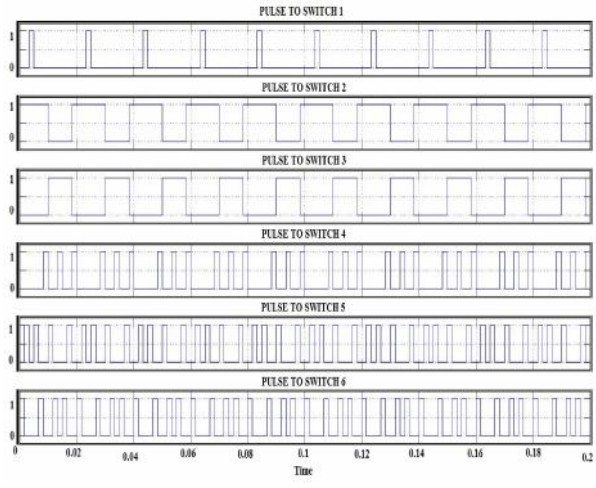
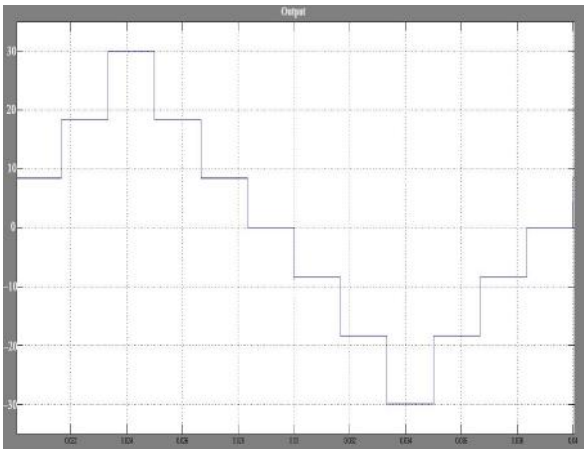


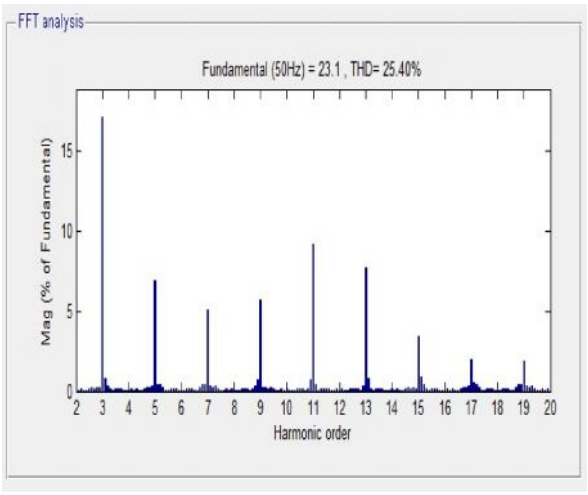
Figure 11 shows the simulation output window obtained from the Matlab. This output voltage waveform is taken from load terminals when the inverter fundamental output frequency is set at 50 Hz [1]. Since the proposed topology is simulated with 30 V DC, the obtained seven levels of output are Vo = +30 V, Vo = +20 V, Vo = +10 V, Vo = 0 V, Vo = -10 V, Vo = -20 V, Vo= -30 V as seen in figure 10. It can also be noted from the figure that the diode conduction losses effect a small voltage drop in the output voltage level +Vdc/3 and –Vdc/3. From the Figure 11, it is clearly visible that the simulated output is identical to the ideal output defined for a seven-level inverter.

Figure 11: Simulation Output Window



The output of any Inverter contains Harmonics. So it is necessary to evaluate the effect of harmonics in the output waveform of inverters [4]. The new proposed multilevel inverter is simulated and its output waveform is analysed using FFT to obtain the effect of harmonics in the output waveform. Figure 12 shows the magnitude of harmonics versus harmonic order. From the Figure 12 it can be seen that in this multilevel inverter the lower order harmonics are very much reduced.

Figure 12: Harmonics Analysis Using FFT



CONCLUSION

From the simulated results it can be seen that the proposed new 7-level multilevel topology works as expected. This new proposed topology is a combination of two auxiliary switches and four main power switches. This means that, the new proposed topology requires less components than the configuration that are already present. Hence the over losses will be reduced and the cost of the circuit is also reduced. Since the simulated results present no unexpected problems, and confirm the predicted advantages, the new configuration is aiming to proceed to the next stage of development of hardware prototype.

ACKNOWLEDGMENT

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