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Research Paper

NEW MULTILEVEL INVERTER TOPOLOGY WITH DECREASED NUMBER OF SWITCHES

Dinesh Kumar S B[1]* and Satisha K[1]

*Corresponding Author: Dinesh Kumar S B, ✉ dini.gubbi@gmail.com

The inverters are becoming one of the resources in many industries and enterprises for power quality and Uninterrupted Power Supply (UPS). The three-phase inverter with six switches is the main implementation circuit in any UPS system. But this inverter supplies harmonics to the load. Due to harmonics, the loss is high. So the multilevel inverters are used in the place of all the three-phase inverter. The multilevel inverter reduces the harmonics. The number of steps increase reduces the number of harmonics in the output. Number of increase in switch creates complications. In this work, reduced switch, increased level multi-level inverter is compared with cascaded H-Bridge multilevel inverter using fundamental switching technique. The various levels of multi-level inverter can be implemented with proposed strategy. The simulation is carried out using Matlab software.

Keywords: Cascaded H-bridge, Multilevel dc link inverter, Pulse width modulation, Total harmonic distortion

INTRODUCTION

The voltage source inverters produce an output voltage or current with levels either 0 or ±Vdc.They are known as the two-level inverters. To produce a quality output voltage wave form with less amount of ripple content, they require high switching frequency. In high-power and high voltage applications these two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and limitations of device ratings. These limitations can be avoided using multilevel inverters.[1]

Multilevel inverters are of 3types: flying capacitor multilevel inverter diode clamped multilevel inverter, and cascaded multilevel inverter. More number of components such as switches, capacitors, clamping diodes are required for these multilevel inverters. 2 (m-1) active switches are required for m number of voltage levels for the cascaded H-bridge multilevel inverters. Multilevel inversion is a power conversion technique in which output voltage obtained is step waveform which is closer to a sine wave and thus Total Harmonic Distortion (THD) [2,3,4] is reduced.

[1] Department of Electrical &, Electronics St. Joseph Engineering College, Mangalore.

In this work a 1–Φ seven level cascaded H-bridge multilevel inverter based on an multilevel DC link (MLDCL) and a bridge inverter. Compared with the existing cascaded multilevel inverters, the proposed MLDCL [1] inverter topologies can have enhanced performance. In this work comparing the performance of the proposed scheme with that of the existing cascaded H-bridge multilevel inverter is done using Fundamental switching technique. The proposed MLDCL inverter [1] can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. For a given number of voltage levels m, the cascaded MLDCL inverter requires m+3 active switches, roughly half the number of switches.

CASCADED H-BRIDGE INVERTER

The cascade H-bridge inverter is a cascade of H-bridges, or H-bridges in a series configuration. A single H-bridge inverter is shown in Figure 1 and three phase cascaded H-bridge inverter for seven-level inverter is shown in Figure 2. Figures 1 and 2 shows the basic power circuit of single H-bridge inverter and the cascade of H-bridge inverter for seven-level inverter respectively. An N level Cascaded H bridge inverter consists of series connected (N-1)/2 number of cells in each phase. Each cell consists of single phase H bridge inverter with separate dc source. There are four active devices in each cell and can produce three levels 0, Vdc/2 and –Vdc/2. Higher voltage levels can be obtained by connecting these cell in cascade and the phase voltage van is the sum of voltages of van = v1 + v2 + v3 + :::: + vN.

Figure 1: Configuration of Single-Phase H-Bridge Inverter

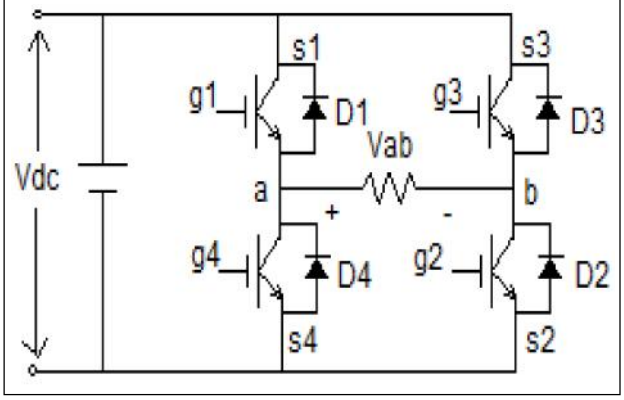


Table 1: Load Voltage with Corresponding Conducting Switches

Active Switches	Output Voltage (Vab)
S_1, S_2	+Vdc
S_3, S_4	–Vdc
S_1, S_4 or S_2, S_3	0

Figure 2: Configuration of Single Phase Cascaded Seven Level H-Bridge Inverter

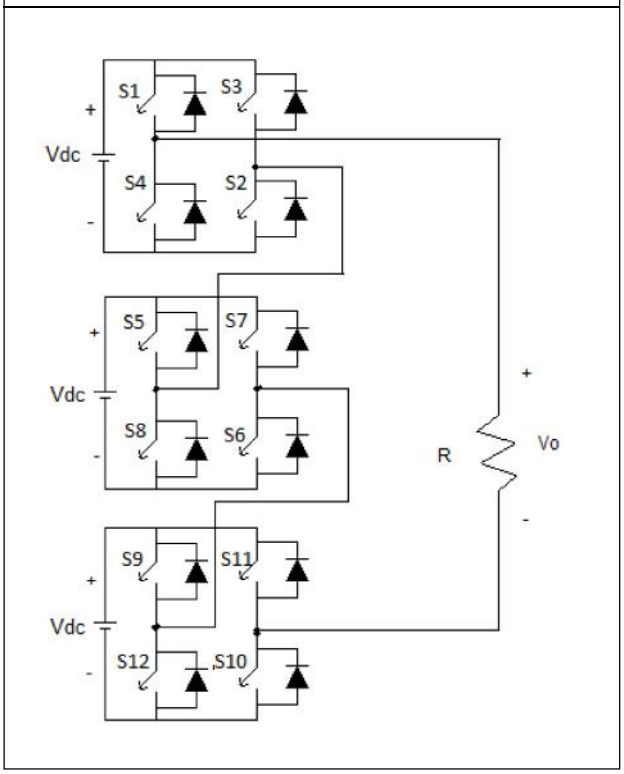


Figure 3: 1–Phase 7 Level Cascaded Inverter Output Waveform

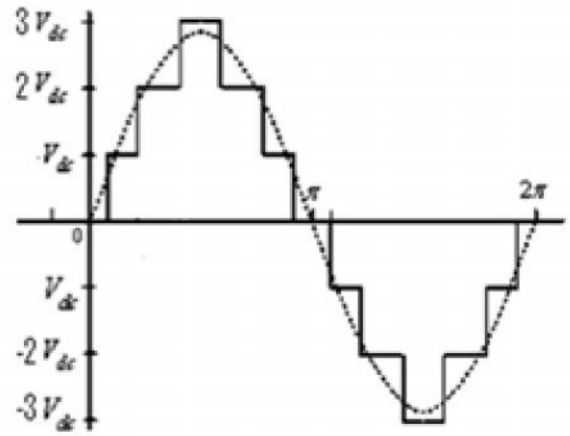


Figure 4: Configuration of Single-Phase Multilevel DC Link Inverter

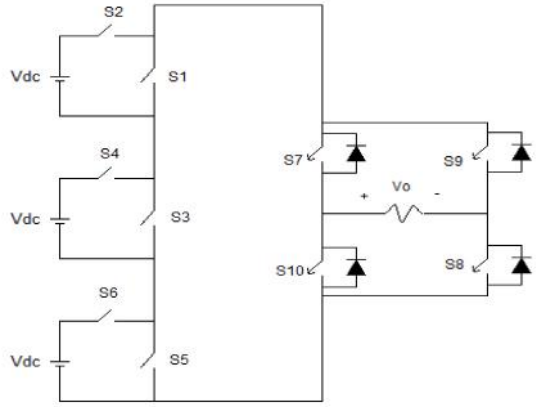


Table 2: Switching Sequence for 1–c 7 Level Cascaded Inverter

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
Vdc	1	1	0	0	0	1	0	1	0	1	0	1
2Vdc	1	1	0	0	1	1	0	0	0	1	0	1
3Vdc	1	1	0	0	1	1	0	0	1	1	0	0
0Vdc	0	1	0	1	0	1	0	1	0	1	0	1
–Vdc	0	0	1	1	0	1	0	1	0	1	0	1
–2Vdc	0	0	1	1	0	0	1	1	0	1	0	1
–3Vdc	0	0	1	1	0	0	1	1	0	0	1	1

PROPOSED MULTILEVEL DC LINK INVERTER TOPOLOGY

The configuration of the proposed inverter is given in Figure 4. single-phase seven-level MLDCL inverter involves various steps of operation and is Compared with the existing cascade H-bridge inverter, number of switches and gate drivers count are significantly reduced

Table 3: Switching Sequence for Single Phase 7 Level MLDCL Inverter

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
0Vdc	1	0	1	0	1	0	1	1	0	0
Vdc	0	1	1	0	1	0	1	1	0	0
2Vdc	0	1	0	1	1	0	1	1	0	0
3Vdc	0	1	0	1	0	1	1	1	0	0
–Vdc	0	1	1	0	1	0	0	0	1	1
–Vdc	0	1	0	1	1	0	0	0	1	1
–Vdc	0	1	0	1	0	1	0	0	1	1

by the new MLDCL inverters as the number of voltage levels increases. For a m number voltage levels given, the new MLDCL inverter requires m+3 active switches, nearly half of the no. of switches, clamping diodes, and voltage-splitting capacitors in the diode clamped configuration or clamping capacitors in the flying capacitor configuration. Simulation results are included to verify the operating principle of the proposed MLDCL inverters.

Comparison of the cascaded inverter and proposed MLDCL inverter based on required number of switches and number of levels is shown in the Figure 5. From this comparison it is clear that as the no. of voltage levels, m, grows, the number of active switches increases according to m+3 for the MLDCL inverter, compared to 2(m-1) for the cascaded H-bridge multilevel inverters.

MODULATION TECHNIQUE

A number of modulation techniques are used in the application of multilevel power conversion. Generally they can be classified into 3 categories:

- Fundamental frequency switching technique
- Carrier based PWM techniques
- Space Vector PWM techniques

For cascaded multilevel inverter, carrier based PWM methods and space vector methods are most used techniques of all the PWM methods but the space vector method will be very complicated with the increase of switching states if the number of output level is more than five. Therefore the carrier based PWM method is preferred if the number of output level is more than five in multilevel inverters. This paper focuses on Fundamental frequency switching technique.

SIMULATION RESULTS

The Simulation was conducted to verify the operation of the Cascaded H-Bridge MLI and proposed MLDCL inverter using Fundamental frequency switching technique.

Seven Level Cascaded H-bridge MLI for 1–c

Fundamental Frequency Switching Technique

Figure 5: Comparison of Required Number of Switches

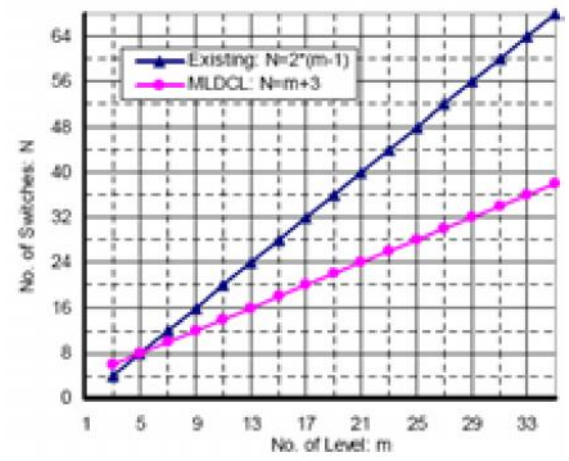


Figure 6: Line Voltage of 1–c Seven Level Cascaded H-Bridge MLI Using SPWM

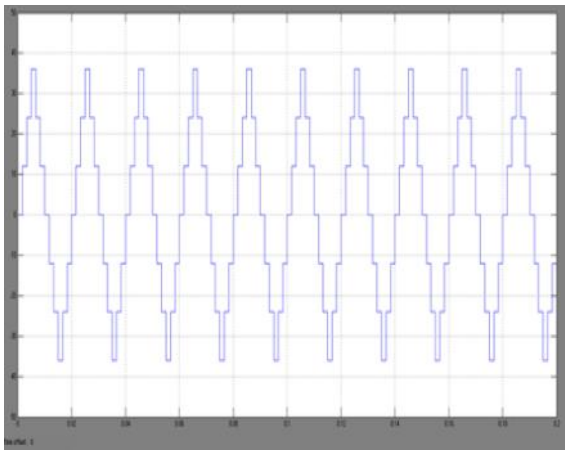
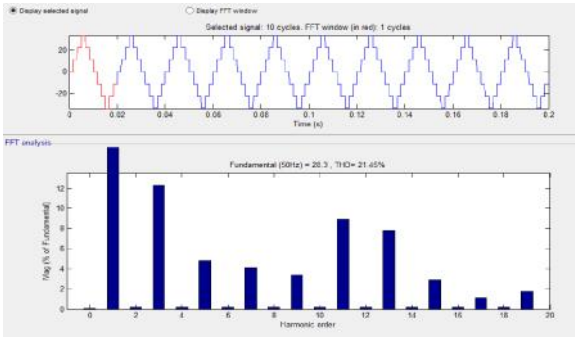


Figure 7: FFT Analysis of Line Voltage of 1–c Seven Level Cascaded H-Bridge MLI Using Fundamental Frequency Switching Technique



Proposed Seven Level MLDCLI for 1–c Fundamental Frequency Switching Technique

Figure 8: Line Voltage of 1–c Seven Level MLDCL Inverter Using Fundamental Frequency Switching Technique

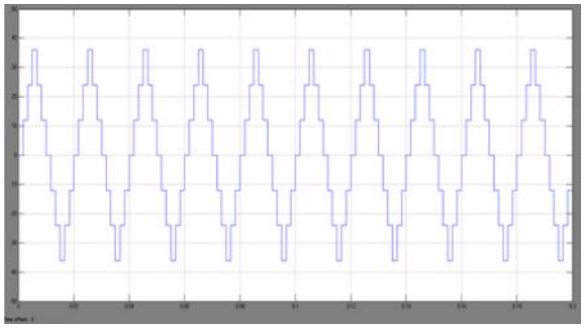
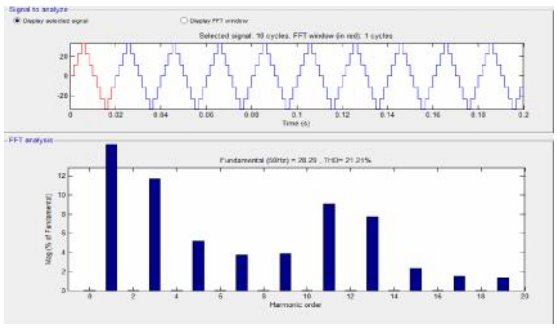


Figure 9: FFT analysis of Line Voltage of 1–c Seven Level MLDCL Inverter Using Fundamental Frequency Switching



Comparison of Results:

Input voltage = 36 v

Output voltage = 72 v (peak to peak)

Load = 12 Ω

A summary of THD and fundamental output voltage for various multilevel inverter topologies with their control strategies are presented. i.e., 1–Φ 7-Level cascaded inverter and 1–Φ 7-level MLDCL inverters were simulated using Fundamental frequency switching technique. And it is concluded that 1–Φ 7-level MLDCL inverter using Fundamental frequency switching technique voltage (28.3 V) with less THD (21.21%).

Table 4: Comparison of THD for Single Phase 7 Level MLDCL Inverter and H-Bridge MLI Fundamental Frequency Switching Technique

Switching Technique	Cascaded 7LI		Multilevel DCL 7LI	
	Fundamental output voltage(volts)	THD (%)	Fundamental output voltage(volts)	THD (%)
Fundamental frequency switching	28.29	21.45	28.3	21.21

CONCLUSION

The presented seven level MLDCL inverters can eliminate roughly half the number of switches, their gate drivers compared with the existing cascaded MLI counterparts. The cascaded MLDCL inverters are cost less due to the savings from the Reduced gate.

The simulation results with harmonic spectrum are presented for cascaded and proposed MLDCL inverters using Fundamental frequency switching technique and in this paper it is concluded that 1–Φ 7-level MLDCL inverter using Fundamental frequency switching technique has given good

fundamental output voltage (28.3 V) with less THD (21.21%) when compared with 1–Φ 7-Level cascaded inverter.

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