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Research Paper

DESIGN AND IMPLEMENTATION OF THREE-LEVEL BOOSTING PFC WITH SENSORLESS CAPACITOR VOLTAGE BALANCING CONTORL

R Mangaiyarkkarasy[1]*, P Marian Daphne[1], P Bhavatharani[1], S Sowmiya[1] and J Pratheebha[1]

*Corresponding Author: R Mangaiyarkkarasy, ✉ pmariandaphne@gmail.com

The three level boosting PFC converters on comparison with the conventional boosting PFC converter consists of two cascaded switches and two cascaded capacitor across DC side voltage. Because of the incompatible equivalent series resistance, incompatible capacitance and the incompatible conducting time of switches, the voltages of the two capacitor may vary in order to balance both the capacitor voltage and hence the controller has to sense the capacitor voltages. In this proposed system the number of feedback signals is reduced and SCVBC is used. This SCVBC is digitally implemented using a PIC based system.

Keywords: Sensorless control, Voltage-balancing control

INTRODUCTION

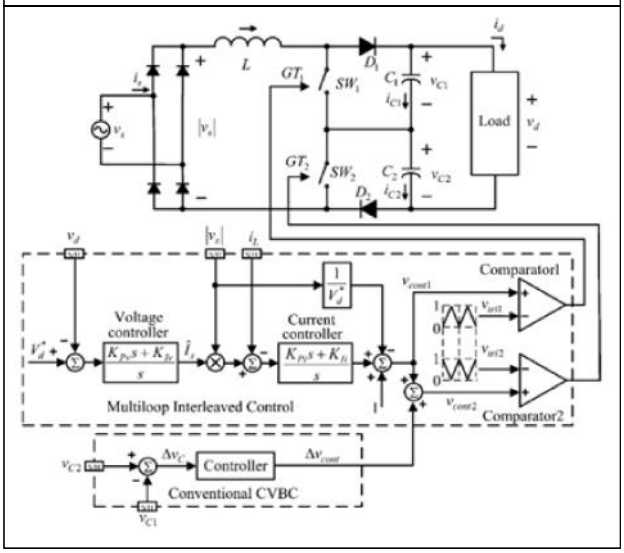
PFC function has to be introduced into several power electronic devices as to raise the system stability and to decrease the losses in power transmission [1]. The expected PFC will be provided by this boost derived PFC converters due to the continuous current properties. The PFC function has to shape the current waveform in ac side and to regulate the voltage waveform on DC side [2].

When switch blocks, then that switch has to withstand the output DC voltage in the conventional converter. But, in the three level boosting DC-DC converter, when one switch conduct another switch will block. When the two capacitor and voltage are balanced, then the blocking switch has to withstand only half of the output DC voltage.

When both the voltages of the capacitors are unbalanced then the switch will be damaged as the voltage of one of the capacitor exceeds the breakdown voltage of the switch. There are three levels of inductor voltage in the three level boost DC-DC Converter so that there will be lower inductor ripple current when compared to conventional boost converter.

[1] Valliammai Engineering College, Kattankulathur, Chennai 603203, India.

Figure 1: Three-Level Boosting PFC Converter with Multiloop Feedforward Control and the Conventional Capacitor Voltage Balancing Control Loop



Thus these converters are used in fuel cell applications [3] and [4] grid connected applications [5]-[7] and other high voltage ratio applications [8] and also they experience low switching losses and high efficiency [9].

The three level boosting PFC Converter consist of multi looped control and interleaved PWM scheme combined to form the multi loop interleaved control [13]. Multi loop control comprises of inner current loop, feed forward loop, and outer voltage loop.

The three phase PFC functionality can be obtained with redundancy [14] by using the delta connected three single phase three level boosting PFC converter.

The three level boosting converter's voltage balancing control loop can be found in the literature [7], [8], [11], [12], [15] and for controls of half bridge PFC converter [16], [17] and multi level inverter [18], [19]. The incompatible capacitances and ESR can cause imbalance in voltage. Therefore balance between the voltages of the two capacitor has to be taken into account. The capacitor voltage has to be balanced by the three level boosting converter controls. A method of voltage balance control by sensing only the inductor current was proposed in [20].

PFC CONVERTER IN THREE LEVEL BOOSTING

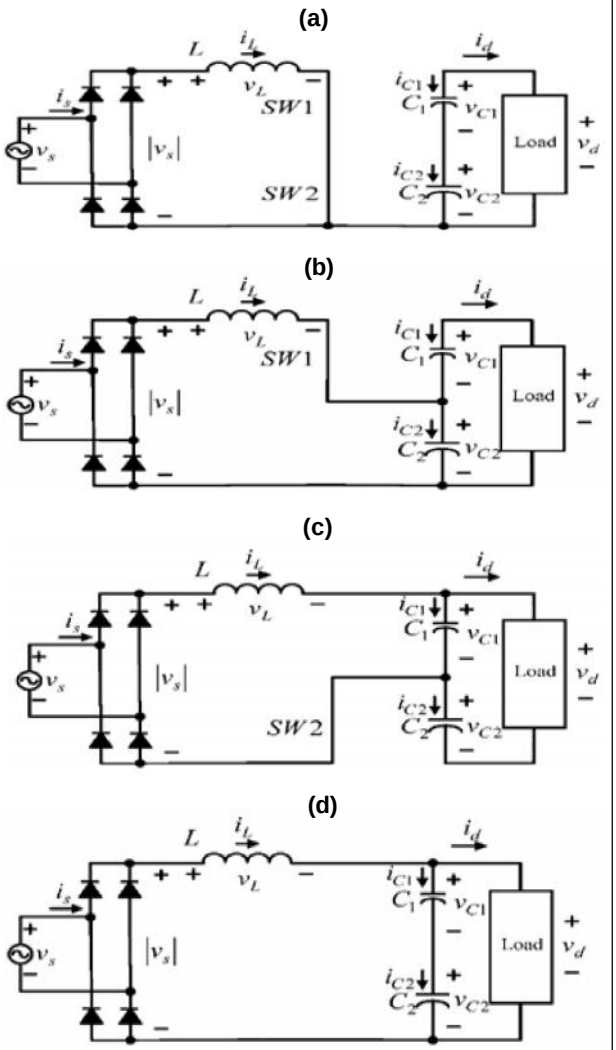
We assume the input ac voltage, $V_s = V_a \sin(2\pi ft)$ as a sinusoidal function which has a sinusoidal function which has a peak amplitude V_s. The three-level boosting converter's input voltage can be expressed through the diode rectifier. That is, the rectified voltage $|v_s|$. The control signals v_{cont1} and v_{cont2} are regarded as two constants for the switching period $Ts=1/f_s$ by the assumption that the value of switching frequency f_s is higher than the value of line frequency f. An ideal inductor and ideal capacitor are assumed there by assuming the value of inductor and capacitor resistance to be zero.

The interleaving of two triangular signals v_{tri1} and v_{tri2} by 180° is seen. The control signal v_{cont1} and the gate signal GT_1 are generated from the conventional multi loop control and by comparing the control signal v_{cont1} and the triangular signal v_{tri1} respectively.

By sensing both the capacitor voltages, the compensation signal vcont is generated by the conventional CVBC through the detection of the voltage imbalance. The compensation signal v_{cont} is added to the control signal v_{cont1} to obtain the other signal v_{cont2}. The comparison between the triangular signals v_{tri2} and the control signal v_{cont2} gives the gate signal GT_2.

Both switches can conduct at the same time without concerning about short circuit damage,

Figure 2: Possible Switching States in the Three-Level Boosting PFC Converter: (a) State 1, (b) State 2, (c) State 3, (d) State 4



because of the input inductor L and the two diodes D_1 and D_2 in the three-level boosting PFC converter. In the three-level boosting PFC converter there are four switching states.

In the switching state 1 both switches turn on. The inductor voltage v_L in the three level boosting PFC converter becomes equal to the rectified input voltage $v_L = |v_s|$ and the energy from both the capacitors is supplied to the load $i_{c1} = i_{c2} = (-i_d) < 0$.

The top and bottom switch turns ON and OFF respectively in the switching state 2.The final resulting inductor voltage v_L is equal to the subtraction the bottom capacitor voltage $v_L = |v_S| - v_{C2}$ from the rectified input voltage $|v_s|$. Energy to the load $i_{C1} = (-i_d) < 0$ is supplied from the capacitor C_1 and the energy from the input voltage is stored in the capacitor C_2, $i_{C2} = (i_L - i_d) > 0$.

Likewise the resulting inductor voltage is the subtraction of the top capacitor voltage from the rectified input voltage $v_L = |v_s| - v_{C1}$. The top capacitor C_1 is charged $i_{C1} = (i_L - i_d) > 0$ and then the bottom capacitor C_2 is discharged $i_{C2} = (-i_d) < 0$ in the switching state 3.

When both the switches are turned OFF the final inductor voltage is equal to the subtraction of the output voltage from the rectified input voltage $v_L = |v_s| - v_d = |v_s| - v_{C1} - v_{C2}$. The simultaneous charging of both capacitors and supply of load current from rectified input voltage $|v_s|$ takes place $i_{C1} = i_{C2} = (i_L - i_d) > 0$.

The capacitor currents in various switching states as shown in Table 1.

Two cases are noted in the behaviour of the three level boosting converter. Within the switching period T_s, $2 > v_{cont1} + v_{cont2} > 1$, two switches may conduct at the same state. Switching state 1, state2 and state 3 are present. In the other case, $1 > v_{cont1} + v_{cont2} > 0$, state 1 does not exist and the other states are present.

Considering the case of $2 > v_{cont1} + v_{cont2} > 1$, the conducting time of switching state 2 is $(1 - v_{cont2})\ T_S$ and the conducting time of switching state 3 is $(1 - v_{cont1})\ T_S$. For the switching state 1 the remaining time is $(v_{cont1} + v_{cont2} - 1)\ T_S$. Therefore the equations are,

Table 1: Capacitor Currents in each State

State		State 1	State 2	State 3	State 4
$2 > V_{cont1} + V_{cont2} > 1$	i_{C1}	$-i_d(<0)$	$-i_d(<0)$	$i_L - i_d(>0)$	–
	i_{C2}	$-i_d(<0)$	$i_L - i_d(>0)$	$-i_d(<0)$	–
$1 > V_{cont1} + V_{cont2} > 0$	i_{C1}	–	$-i_d(<0)$	$i_L - i_d(>0)$	$i_L - i_d(>0)$
	i_{C2}	–	$i_L - i_d(>0)$	$-i_d(<0)$	$i_L - i_d(>0)$

$$<i_{C1}>T_s = -i_d + (1 - v_{cont1})i_L \quad ...(1)$$

$$<i_{C2}>T_s = -i_d + (1 - v_{cont2})i_L \quad ...(1)$$

Considering the other case of $1 > v_{cont1} + v_{cont2} > 0$, the conducting time of the switching state 2 and the conducting time of the switching state 3 is $v_{cont1}\ T_S$ and $v_{cont2}\ T_S$, respectively. For the switching state 4 the remaining time is $(1 - v_{cont1} - v_{cont2})\ T_S$. When calculated the average c apacitor currents are equal to

$$<i_{C1}>_{Ts} - <i_{C2}>_{Ts} = (v_{cont\,2} - v_{cont\,1})i_L = \Delta v_{cont}\, i_L \quad ...(3)$$

voltage imbalance can be given as

$$\Delta v_{c(s)} = \frac{1}{s}\frac{\Delta v_{cont}}{C} i_L \quad ...(4)$$

where $\Delta v_{cont} = v_{cont2} - v_{cont1}$.

Closed-loop transfer function of $\Delta v_{c(s)}$ becomes

$$\frac{\Delta v_{c(s)}}{\Delta v^{*}_{c(s)}} = \frac{\frac{K_p}{c} i_L}{s + \frac{K_p}{c} i_L} \quad ...(5)$$

Thus balancing the capacitor voltage is made possible by design of conventional CVBC with simple P controller.

PROPOSED SYSTEM

Here the input voltage, output voltage, inductor current are to be sensed. The inductor current is three times the switching period with an average value of I_L along with I_{c1} and I_{c2}.

In order to obtain the expected PFC and to yield the control signal, the multi loop control is fed by the average current I_L. From the P controller, the compensating signal Δv_{cont} is obtained as

$$\Delta v_{cont} = K_p(I_{vC2} - I_{vC1}) \quad ...(6)$$

This control signal v_{cont1} is added to the compensating signal vcont thus the other control signal v_{cont2} is obtained as

$$v_{cont2} = v_{cont1} + \Delta v_{cont} = v_{cont1} + k_p(I_{vc2} - I_{vc1}) \quad ...(7)$$

At V_{tri} = 1 (triangular signal peak), the inductor current IL sample to obtain the average value I_L. The I_{vc1} is obtained by sampling the inductor current V_{tri1} rises to 2.5 and the I_{vc2} is obtained by sampling the inductor current when V_{tri1} falls to 0.5 from the peak.

After completing the above said actions, at the controller time, the multi loop control is executed and the two control signals are updated and the two cases obtained are

$$2 > v_{cont1} + v_{cont2} > 1 \quad ...(8)$$

The voltage imbalance waveforms are drawn in Figure, are the two divisions possible in the voltage imbalance $v_c > 0$.

At the switching state 3 the inductor current Il is falling. At the switching state 3 the current I_L is raising. The following equations are derived

$$\Delta I_{vC} = \frac{T_S}{2L}[\,(v_{C2} - v_{C1})(1 - v_{cont1}) - \Delta v_{cont} v_{C2}\,] \quad ...(9)$$

$$\Delta IvC = \frac{T_S\,(1-V_{cont\ 1})}{2L+T_s K_p v_{c2}}(v_{c2} - v_{c1}) = k_1(v_{c2} - v_{c1}) \quad ...(10)$$

$$1 > v_{cont\ 1} + v_{cont\ 2} > 0 \quad ...(11)$$

By the waveform symmetry the time t_1 present at the instants of sampling the value I_{vc1},the turning off instants of the gate signal GT_1 and the time present in the turning-on instance of the gate signal GT_1, the instance of sampling the value I_{vc2} are equal in nature . In terms of control signal v_{cont1} the time t_1 can be expressed as:

$$t_1 = \frac{\text{s of qt 1}}{\left(\frac{v_{cor}}{2}\right)} - \frac{1}{4}\text{signa}\ T_S \quad ...(12)$$

For switching state 2 the conducting time is $(1 - v_{cont2})\ T_s$ and the switching state 3 the conducting time is $(1 - v_{cont1})\ T_s$. For switching state 1 the remaining time is $(v_{cont1} + v_{cont2} - 1)\ T_s$.

In the three level boosting converter the average inductor voltage $(V_L)T_s$ can be written as:

$$\langle v_L \rangle T_s = |v_S| - v_{c1}(1 - v_{cont1}) - v_{c2}(1 - v_{cont2}) \quad ...(13)$$

$$|v_s| = (1 - v_{cont1})v_{c1} + (1 - v_{cont2})v_{c2} \quad ...(14)$$

The difference of the two sampled values I_{vC1} and I_{vC2}, ΔI_{vc} can be written in terms of time t_1.

$$\Delta I_{vC} = I_{vC2} - I_{vC1} = 2\frac{|v_S|}{L}t_1 + \frac{|v_S| - v_{c1}}{L}(1 - V_{cont1})T_S \quad ...(15)$$

Substituting (12) and (14) into (13) to obtained

$$\langle v_L \rangle T_s = |v_S| - v_{c1}(1 - v_{cont1}) - v_{c2}(1 - v_{cont2}) \quad ...(16)$$

$$\Delta I_{vC} = I_{vC2} - I_{vC1} = -\frac{|v_S| - v_{C2}}{L}v_{cont1}T_S - 2\frac{|v_s| - v_d}{L}t_2 \quad ...(17)$$

$$\Delta I_{vC} = \frac{T_S}{2L}[\,(v_{C2} - v_{C1})\,v_{cont1} + \Delta v_{cont} v_{C2}\,] \quad ...(18)$$

(18) can be re written as

$$\Delta I_{vC} = \frac{T_s v_{cont\ 1}}{2L - T_s K_p v_{c2}}(v_{c2} - v_{c1}) = k_2(v_{c2} - v_{c1}) \quad ...(19)$$

The coefficient may be either positive or negative

$$2L - T_s K_p v_{c2} > 0 \quad ...(20)$$

K_p should be in range

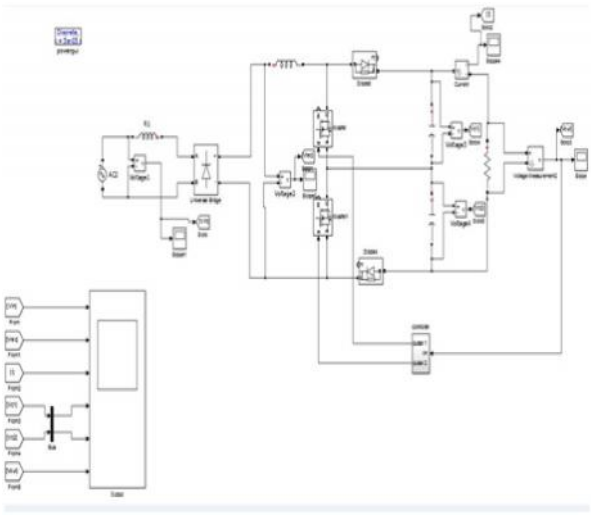
$$0 < K_p < \frac{2L}{T_s v_{c2,max}} \quad ...(21)$$

The difference value ΔI_{vc} is proportional to the value of voltage imbalance $(v_{c2} - v_{c1})$. The voltage imbalance can be detected using the difference ΔI_{vc} without the need to directly sense the capacitor voltages.

SIMULATION

The simulation is performed in MATLAB version 2013a. The scopes are present to view the waveforms corresponding to each parameters. The final Goto block is used to view the waveforms as a whole. The input output values can be know from the waveforms. From the simulation results it is seen that the boosting has occurred in the three level PFC converters. Thus it is seen that the simulation results match with the expected results.

Figure 3: Simulated Block



SIMULATION WAVEFORMS

The input voltage of 110 V is rectified at a voltage value of about 110 V which is supplied to the boost converter and thus an output voltage of about 330 V is obtained as a result of three level boosting.

Figure 4: Input Voltage Waveform

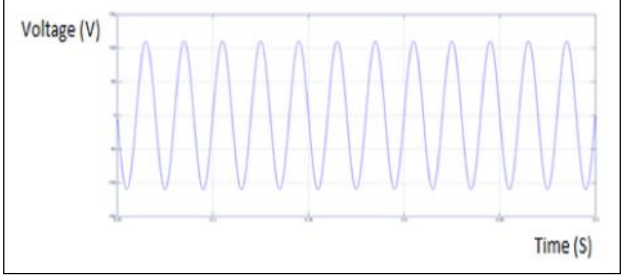


Figure 5: Rectifier Voltage Waveform

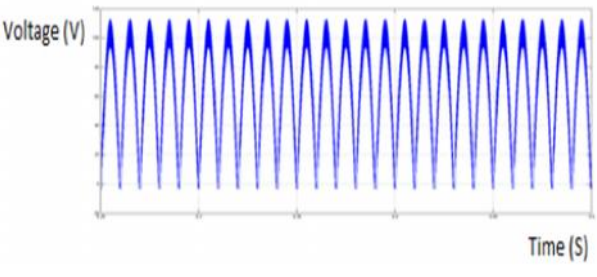


Figure 6: Capacitor C_1 Voltage Waveform

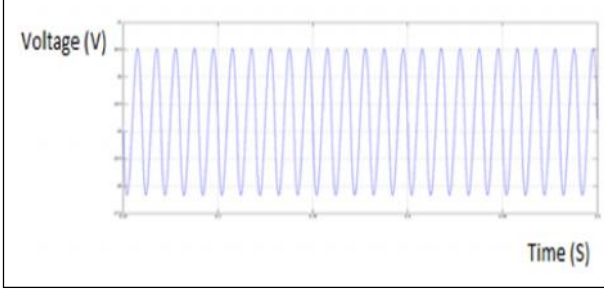


Figure 7: Capacitor C_2 Voltage Waveform

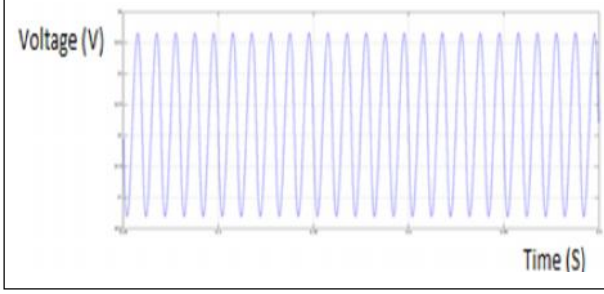


Figure 8: Load Current Waveform

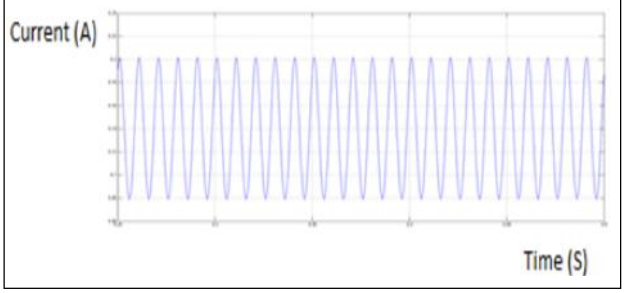
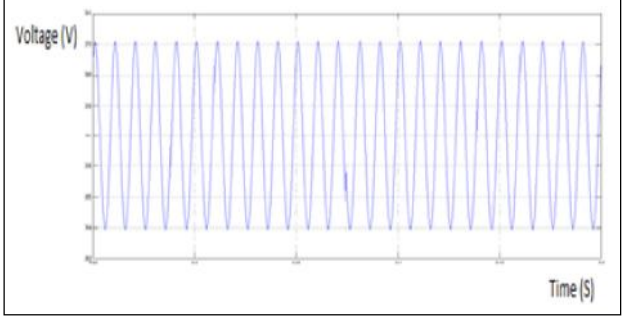


Figure 9: Output Voltage Waveform



SIMULATION RESULTS

Here, the three level boosting converter's simulation results are given and the Table 2

Table 2: Parameters Used in Three Level Boosting Converter

Parameters	Ratings
Input voltage	110 V(RMS),50 Hz
Output voltage	V_d^* = 300 V
Inductor	0.5 mH
Carrier frequency	20 KHz
Capacitor	C_1 = 2240, C_2 = 1410 Equivalent Capacitance = 865
Voltage balance parameter	K_p = 0.05

shows us the used parameters values. In the multi loop control the ratings of the voltage controller and current controller are k_{pv} = 0.1 , k_{iv} = 5 and k_{pi} = 0.02 and k_{li} = 10 respectively. We have seen from (), that the range of the parameter k_p should be between the value 0 and 0.1 with the consideration of the inductance variation k_p = 0.05 is selected.

For simulation 2 mismatched capacitances with values c_1 = 2240 and c_2 = 1410 are used. In the practical case the mismatched conditions do not occur but they are helpful for the demonstration of the proposed SCVBC.

Steady State Response

The three level boosting PFC converter's simulation results for 300 W and 600 W are seen. The input current and the input voltage vs are sinusoidal and in phase. Even though the capacitances are mismatched the capacitor voltages have the average values equal to the half average value of the dc voltage v_d.

The obtained value ΔI_{vc} is approximately equal to zero in the steady state. Therefore the conclusive result is that the proposed SCVBC is able to function like PFC in the three level boost converter without the need of directly sensing the capacitor voltage.

Transient Response

The simulation results during load regulation are plotted to observe the transient response. Due to the change of the load resistance from 300 to 150 ohm the output power changes from 300 W to 600 W. When operated the sinusoidal input current is and input voltage v_s are always in phase with each other and the output voltage v_d is regulated to the value 300 V.

Because the capacitance C_2 is smaller than the other capacitance C_1 at the bottom capacitor voltage V_{c2} has larger voltage dip than the top capacitor voltage V_{c1}. The difference I_{vc} which is the significant dip can be found during the transient operation.

The proposed SCVBC can detect the voltage imbalance and balance the capacitor voltages which is confirmed by knowing the value of the average capacitor voltages which are finally equal to half voltage command 150 v.

The difference Ivc becomes positive when the capacitor voltage v_{c2} is larger than the other capacitor voltage v_{c1} during the transient operation. When the resistor is removed the capacitor voltages are both finally imbalanced.

The above results shows us clearly that the SCVBC works without direct sensing of the capacitor voltages.

CONCLUSION

This paper proposes the SCVBC method for three-level boosting PFC converter. The voltage imbalance is detected by sensing the inductor current by the sampling and hold strategy in this proposed method. By the way the power factor is also simultaneously enhanced. By using this method we can

eliminate the need for extra sensors and reduces the control complexity, cost and size. The main advantage of the PFC converters are the reduction in cost and size. PIC-based system is used in the control method and the results are demonstrated.

REFERENCES

1. Singh B, Singh B N, Chandra A, Al-Haddad K, Pandey A and Kothari D P (2003), "A Review of Single-Phase Improved Power Quality ACDC Converters", *IEEE Trans. Ind. Electron.*, Vol. 50, No. 5, pp. 962-981.
2. Crebier J C, Revol B and Ferrieux J P (2005), "Boost-Chopper-Derived PFC Rectifiers: Interest and Reality", *IEEE Trans. Ind. Electron.*, Vol. 52, No. 1, pp. 36-45.
3. Yang L S, Liang T J, Lee H C and Chen J F (2011), "Novel High Step-Up DC-DC Converter with Coupled-Inductor and Voltage-Doubler Circuits", *IEEE Trans. Ind. Electron.*, Vol. 58, No. 9, pp. 4196-4206.
4. Shahin A, Hinaje M, Martin J P, Pierfederici S, Rael S and Davat B (2010), "High Voltage Ratio DC-DC Converter for Fuel-Cell Applications", *IEEE Trans. Ind. Electron.*, Vol. 57, No. 12, pp. 3944-3955.
5. Todorovic M H, Palma L and Enjeti P N (2008), "Design of a Wide Input Range DC-DC Converter with a Robust Power Control Scheme Suitable for Fuel Cell Power Conversion", *IEEE Trans. In. Electron.*, Vol. 55, No. 3, pp. 1247-1255.
6. Li W and He X (2011), "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid Connected Applications", *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1239-1250.
7. Kwon J M, Kwon B H and Nam K H (2008), "Three Phase Photo Voltaic System with Three Level Boostimg MPPT Control", *IEEE Trans. Power. Electron.*, Vol. 23, No. 5, pp. 2319-2327.
8. Yaramasu V and Wu B (2011), "Three-Level Boost Converter Based Medium Voltage Megawatt PMSG Wind Energy Conversion Systems", in *Proc. Energy Convers. Cong. Expo.*, pp. 561-567.
9. Zhang M T, Jiang Y, Lee F C and Jovanic M M (1995), "Single-Phase Three-Level Boost Power Factor Correction Converter", in *IEEE App. Power Electron. Conf.*, pp. 434-439.
10. Pinheiro J R, Lar Vidor D and Groundling H A (2000), "Dual Output Three Level Boost Power Factor Correction Converter with Unbalanced Loads", in Proc. IEEE App. Power Electron. Conf., April, pp. 245-252.
11. Wu H and He X (2002), "Single Phase Three Level Power Factor Correction Circuit with Passive Lossless Snubber", *IEEE Trans. Power. Electron.*, Vol. 17, No. 6, pp. 946-953.
12. Liao J Y and Chen H C (2011), "Multiloop Interleaved Control for Two-Switch Two-Capacitor Three-Level SMR Without Capacitor Voltage Balancing Loop", in *Proc. IEEE Energy Convers. Cong. Expo.*, pp. 3766-3772.

13. Greul R, Round S D and Kolar J W (2006), "The Delta-Rectifier: Analysis, Control and Operations", *IEEE Trans. Power Electron.*, Vol. 21, No. 6, pp. 1637-1648.

14. Riberio E, Cardoso A J M and Boccaletti C (2013), "Fault-Tolerant Strategy for a Photovoltaiv DC-DC Converter", *IEEE Trans. Power Electron.*, Vol. 28, No. 6, pp. 3008-3018.

15. Ghosh R and Narayanan G (2007), "A Simple Analog Controller for Single Phase Half Bridge Rectifier", *IEEE Trans. Power Electron.*, Vol. 22, No. 1, pp. 186-198.

16. Lin B R, Huang T L and Huang C H (2003), "Bi-Directional Single Phase Half-Bridge Rectifier for Power Quality Compensation", *IEEE, Electric Power Appl.*, Vol. 150, No. 4, pp. 397-406.

17. Shu Z, Ding N, Chen J, Zhu H and He X (2013), "Multilevel SVPWM with DC-Link Capacitor Voltage Balancing Contrl for Diode-Clamped Multilevel Converter Based STATCOM", *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 1884-1896.

18. Gao C, Jiang X, Li Y, Chen Z and Liu J (2013), "A DC-Link Voltage Self-Balancing Method for a Diode-Clamped Modular Multilevel Converter with Minimum Number of Voltage Sensor", *IEEE Trans. Power Electron.*, Vol. 28, No. 5, pp. 2125-2139.

19. Chen H C and Wen-Jan Lin (2014), "MPPT and Voltage Balancing Control with Sensing only Inductor Current for PV-Fed Three-Level Boost-Type Converters", *IEEE Trans. Power Electron.*, Vol. 29, No. 1, pp. 29-35.