ISSN 2319 – 2518 www.ijeetc.com Special Issue, Vol. 1, No. 1, March 2015 National Level Technical Conference P&E-BiDD-2015 © 2015 IJEETC. All Rights Reserved

**Research Paper** 

# COMPARATIVE ANALYSIS OF DIFFERENT N-LEVEL INVERTER

B Manikandan<sup>1</sup>\*, K Muthukumar<sup>1</sup>, C Muralitharan<sup>1</sup> and G Renukadevi<sup>1</sup>

\*Corresponding Author: B Manikandan, 🖂 bmanikandan@jeppiaarinstitute.org

This paper presents the comparative analysis of n-level inverter. An n-level inverter has many advantages, such as reduced Total Harmonic Distortion (THD), the dv/dt is low and the EMI from the system is low, lower switching frequencies can be used and hence reduction in switching losses. In this paper the generalized n-level inverter is developed in Matlab/Simulink environment. The n-level inverters are triggered by Sinusoidal Pulse Width Modulation Technique. The 2-level, 3-level and 5-level inverter results are analyzed in terms of fundamental voltage and THD.

Keywords: Fundamental voltage, n-level inverter, SPWM, THD

#### INTRODUCTION

Recently, with the dramatic improvements in high voltage technologies, High Voltage Insulated Gate Bipolar Transistor (HVIGBT) and Gate Commutated Thyristor (GCT) are expanding the area of their application. For the high performance ac drive systems at increased power level, high quality inverter output with low harmonic loss and torque pulsation is necessary. In case of the conventional two-level inverter configuration, the harmonic contents reduction of an inverter output current is achieved mainly by raising the switching frequency.

From the aspect of harmonic reduction and high dc-link voltage level, three-level approach

seems to be the most promising alternative. The harmonic contents of a five-level inverter are less than that of a two-level and three-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage. So the n-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems. While increasing modulation index, the total harmonic distortion will be reduced and the voltage will be increased. This paper discuss the comparative analysis of different n-level inverter in terms of fundamental voltage and THD. For the high performance ac drive systems at increased power level, high quality inverter output with low harmonic loss and torque pulsation is necessary. In case of the

<sup>1</sup> Department of Electrical and Electronics Engineering, Jeppiaar Institute of Technology, Sriperumbudhur, Chennai 631604, India.

conventional two-level inverter configuration, the harmonic contents reduction of an inverter output current is achieved mainly by raising the switching frequency. However, the harmonic contents of a n-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage.

Variable speed electric drives predominately utilize three-phase machines. However, since the variable speed ac drives require a power electronic converter for their supply. Supply for a three-phase variable speed drive is provided by a Voltage Source Inveters (VSI). A number of PWM techniques are available to control a two-level three-phase VSI. The most widely used pulse PWM techniques for three-phase inverters are the carrier-based sinusoidal PWM (including the offset addition) and the space vector PWM (SVPWM). These techniques have been extensively discussed in the literature (1-15). The number of voltage vectors of a two-level of phases increases. A simulation is preferred for different modulation indices for n-level VSI. The number of switched required for two level inverter is 6 switches, 3-level, 5-level and 7level inverter required 12, 24 and 36 switches respectively. This paper analysis the comparison between the n-level inverters in terms of fundamental voltage and THD.

## POWER CIRCUIT OF N-LEVEL INVERTER

Figures 1 and 2 shows the power circuit and block diagram of n-level voltage source inverter, the input supply is obtained from the rectifier (DC), the output of the DC is given to the n-level inverter, the output of the VSI is



connected to the three-phase induction motor load. The n-level inverter switches are triggered by multi carrier SPWM technique. The switches in the voltage source inverter can be turned on and off as required. In the simplest approach, the top switch is turned on and off only once in each cycle, a square wave waveform results. However, if turned on several times in a cycle an improved harmonic profile may be achieved. In the most straightforward implementation, generation of the desired



output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as depicted schematically in Figure 3. The fundamental frequency is 50 Hz, the carrier frequency is greater than fundamental frequency. The MI is ratio of amplitude of fundamental to the amplitude of carrier waveform.

$$MI = \frac{V_{ac}}{V_{carrier}}$$

# DESCRIPTION OF THREE LEVEL INVERTER

Figure 4 shows the power circuit of 3-level voltage source inverter. The three-level inverter



topology is generally used in realizing the high performance, high voltage ac drive systems. The 3-level inverter requires 4 switches in one arms, totally 12 switches are used in this circuit. The harmonic reduction and high dclink voltage level, three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage. The number of switches required for 5-level and 7-level inverter is 24 and 36 switches respectively.

### MODELING OF THREE-PHASE INDUCTION MOTOR

High performance drive control, such as vector or field oriented control is based on the dynamic D-Q model of the machine. Three phase machine can be represented as a two phase equivalent with  $d_s - q_s$  corresponding to stator direct and quadrature axes that are fixed on the stator axis and  $d_r - q_r$  corresponding to rotor direct and quadrature axes that are rotating with a fixed speed on the rotor axis. The effect of time varying inductance can be eliminated by referring the stator and rotor variables to a common reference frame which rotates at any speed. A three phase induction motor can be modeled by the following steps as follows. A  $3\Omega$  inverter with its pulse given through SPWM technique is used to provide a  $3\Omega$  supply to the induction motor

$$V_{a} = V \cos_{\mu} e$$

$$V_{b} = V \cos(_{\mu} e - \Gamma) \qquad \dots(1)$$

$$V_{c} = V \cos(_{\mu} e - 2\Gamma)$$

where

$$r=\frac{2f}{3}, _{\# e}=\int \check{S}_{e}$$

The first two rows of the matrix define variables that will lead to fundamental flux and torque production. The last row defines the zero sequence components. Equations for pairs of x-y components are completely decoupled and do not contribute to torque production when sinusoidal distribution of the flux around the air-gap is assumed. Stator variables in stationary reference frame are transformed to synchronous reference frame. In this transformation the q-axis of the voltage variable is aligned to zero and only the d-axis variable is present for easy control.

$$\begin{pmatrix} V_{ds} \\ V_{qs} \end{pmatrix} = \begin{pmatrix} \cos w_{e} & \sin w_{e} \\ -\sin w_{e} & \cos w_{e} \end{pmatrix} * \begin{pmatrix} V_{ds} \\ V_{qs} \end{pmatrix} \qquad \dots (2)$$

The stator and the rotor voltage equations in synchronous reference frame are given by Equations (3) and (4)

$$V_{ds}^{e} = i_{ds}^{e} R_{s} + \frac{d}{dt} \mathbb{E}_{dr}^{e} - \check{S}_{s} \mathbb{E}_{qs}^{e}$$
$$V_{qs}^{e} = i_{qs}^{e} R_{s} + \frac{d}{dt} \mathbb{E}_{qr}^{e} + \check{S}_{s} \mathbb{E}_{ds}^{e} \qquad \dots (3)$$

$$V_{dr}^{e} = i_{dr}^{e} R_{r} + \frac{d}{dt} \mathbb{E}_{dr}^{e} - (\tilde{S}_{e} - \tilde{S}_{r}) \mathbb{E}_{qr}^{e}$$
$$V_{qr}^{e} = i_{qr}^{e} R_{r} + \frac{d}{dt} \mathbb{E}_{qr}^{e} - (\tilde{S}_{e} - \tilde{S}_{r}) \mathbb{E}_{dr}^{e} \qquad \dots (4)$$

Flux Expressions are obtained by rearranging the Equations (3) and (4)

$$\mathbb{E}_{ds}^{e} = \int V_{ds}^{e} - id_{s}^{e} R_{s} + \check{S} \cdot \mathbb{E}_{qs}^{e}$$

$$\mathbb{E}_{qs}^{e} = \int V_{qs}^{e} - iq_{s}^{e} R_{s} - \check{S} \cdot \mathbb{E} d_{s}^{e}$$

$$\mathbb{E}_{ds}^{e} = \int V_{ds}^{e} - id_{s}^{e} R_{s} + (\check{S}_{e} - \check{S}_{r}) \cdot \mathbb{E}_{qr}^{e} \qquad \dots (5)$$

$$\mathbb{E}_{qs}^{e} = \int V_{qs}^{e} - iq_{s}^{e} R_{s} - (\check{S}_{e} - \check{S}_{r}) \cdot \mathbb{E}_{dr}^{e}$$

Current expression in terms of flux linkage and leakage inductance of the motor

$$i_{qs}^{e} = \frac{\bigoplus qs}{(L_{lr} + L_{m}] - L_{m} \bigoplus qr}{(L_{ls}L_{lr} + L_{ls}L_{m} + L_{m}L_{lr})}$$

$$i_{ds}^{e} = \frac{\bigoplus ds}{(L_{lr} + L_{m}] - L_{m} \bigoplus dr}{(L_{ls}L_{lr} + L_{ls}L_{m} + L_{m}L_{lr})}$$

$$i_{qr}^{e} = \frac{\bigoplus qr}{(L_{ls}L_{lr} + L_{lr}L_{m} + L_{m}L_{ls})} \qquad \dots (6)$$

$$i_{dr}^{e} = \frac{\bigoplus qr}{(L_{ls}L_{lr} + L_{lr}L_{m} + L_{m}L_{ls})}$$

Transformation of stator current in synchronous reference frame to stationary reference frame

$$\begin{pmatrix} i_{ds}^{s} \\ i_{qs}^{s} \end{pmatrix} = \begin{pmatrix} \cos_{y} e & -\sin_{y} e \\ \sin_{y} e & \cos_{y} e \end{pmatrix} * \begin{pmatrix} i_{ds}^{e} \\ i_{qs}^{e} \end{pmatrix} \qquad \dots (7)$$

To obtain the three phase stator current from the stator currents in stationary reference frame by  $2\Omega$  to  $3\Omega$  transformation

$$i_{a} = i_{qs}^{s} \cos_{w} e + i_{ds}^{s} \sin_{w} e$$
  

$$i_{b} = i_{qs}^{s} \cos_{w} e - r + i_{ds}^{s} \sin_{w} e - i_{ds}^{s} \sin_{w} e - i_{ds}^{s} \sin_{w} e - r + i_{ds}^{s} \sin_{w} e - r + i_{ds}^{s} \sin_{w} e$$

Electromechanical torque and rotor speed of the five phase induction motor is obtained by (9) and (10) respectively

$$T_e = p^* L_m^* (i_{qs} i_{dr} - i_{ds} i_{qr})$$
  
=  $p^* (\mathbb{E}_{qs} i_{dr} - \mathbb{E}_{ds} i_{qr})$  ...(9)

$$\check{S}_r = \int \frac{p}{2} * \frac{(T_e - T_l - B)}{J} dt$$
 ...(10)

## SIMULATION RESULTS

The n-level inverter is simulated with the above said switching scheme and the results are observed. The input DC is fixing to 1 volt, switching frequency of the VSI is chosen as 10 kHz and the fundamental frequency is set to 50 Hz. The simulation results are discussed and compared in different modulation indices. The Figures 5 and 6 shows the simulation results for 3-level voltage source inverter. Figure 5 shows the phase voltage of 3 level inverter at modulation indices 1 condition. It is found that increasing modulation indices the fundamental voltage is increased and total harmonic distortion is reduced. Similarly the simulation results are obtained 5-level inverter. Table 1 shows the simulation results for different 3-level inverter its seen that when increasing modulation Indices the THD is reduced and the fundamental voltage is increased. Table 2 shows the simulation results for different 3-level inverter its seen that when increasing modulation Indices the THD is reduced and the fundamental voltage is increased. Table 3 shows the comparative analysis of 3-level and 5-level inverter at



modulation index 1 condition. It is seen that maximum voltage and minimum THD is observed in the 5-level inverter. Figure 7 shows the three-level voltage source inverter fed threephase induction motor drive results. It is



Table 1: Line Voltage and Phase Voltage of 3-Level Inverter				
мі	V_		V <sub>Ph</sub>	
	RMS	THD	RMS	THD
0.2	0.07784	211.44	0.04466	211.61
0.4	0.2132	109.32	0.1232	109.11
0.6	0.3409	56.68	0.1968	56.95
0.8	0.4111	43.19	0.2677	43.22
1	0.5943	35.26	0.344	35.31

Table 2: Line Voltage and Phase Voltage of 5-Level Inverter				
	V_		V <sub>Ph</sub>	
IVII	RMS	тно	RMS	тно

	RMS	THD	RMS	THD
0.2	0.1249	110.65	0.0252	111.25
0.4	0.2132	109.32	0.1232	109.11
0.6	0.3409	56.68	0.1968	56.95
0.8	0.4111	43.19	0.2677	43.22
1	0.6152	16.27	32.52	25.59

Table 3: Comparative Analysis of 3-Level and 5-Level Voltage Source Inverter

МІ	Line Voltage of 3-Level Inverter		Line Voltage of 5-Level Inverter	
	RMS	THD	RMS	THD
1	0.5943	35.26	0.6152	16.27

Figure 7: Three-Level Voltage Source Inverter Fed Three-Phase Induction Motor Drive



observed that load is maintained 50 Nm and corresponding stator current, speed and motor torque are found. From the simulation results the motor torque follows the load torque.

### CONCLUSION

This paper presents the comparative analysis of n-level inverter. The n-level inverter is developed in matalab/simulink environment. The performance of the multi-level inverter is analyzed for different modulation indices. The reduced THD of n-level inverters are very useful in high power and power quality application. The integrated 3-level inverter fed induction motor results are obtained. From the simulation results increasing modulation index THD is reduced. If increasing the more number of levels the THD is reduced significantly.

#### REFERENCES

- Calais M, Borle L J and Agelidis V G (2001), "Analysis of Multicarrier PWM Methods for a Single-Phase Five Level Inverter", in Proc. 32<sup>nd</sup> IEEE Power Electronics Specialists Conference, PESC'01, July, pp. 1351-1356.
- Carrara G, Gardella S, Marchesoni M, Salutari R and Sciutto G (1992), "A New Multilevel PWM Method: A Theoretical Analysis", *IEEE Trans. Power Electron*, Vol. 7, pp. 497-505.
- Fang Zheng Peng, Jih-Sheng Lai and Rodriguez J (2002), "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", *Industrial Electronics, IEEE Transactions*, Vol. 49, No. 4, pp. 724-738.
- 4. Gregory Patangia D (2007), "A Novel Multilevel Strategy in SPWM Design,

Industrial Electronics", *IEEE International Symposium*, ISIE, pp. 515-520.

- Holmes D G and McGrath B P (2002), "Multi Carrier PWM Strategies for Multilevel Inverters", *Industrial Electronics, IEEE Transactions*, Vol. 49, No. 4, pp. 858-867.
- Jeevananthan R and Nandhakumar P (2007), "Inverted Sine Carrier for Fundamental Fortification in PWM Inverters and FPGA Based Implementations", Serbian Journal of Electrical Engineering, Vol. 4, No. 2, pp. 171-187.
- Jin B S, Lee W K, Kim T J, Kang D W and Hyun D S (2005), "A Study on the Multi Carrier PWM Methods for Voltage Balancing of Flying Capacitor in the Flying Capacitor Multilevel Inverter", in Proc. IEEE Ind. Electron. Conf., November, pp. 721-726.
- Ki-Seon Kim, Young-Gook Jung and Young-Cheol Lim (2009), "A New Hybrid Random PWM Scheme", *IEEE Transactions on Power Electronics*, Vol. 24, No. 1.
- Lai J S and Peng F Z (1996), "Multilevel Converters—A New Breed of Power Converters", *IEEE Trans. Ind. Applicat.*, Vol. 32, pp. 509-517.
- Renukadevi G and Rajambal K (2011), "Novel Carrier-Based PWM Technique for n-Phase VSI", *International Journal of Energy Technologies and Policy*, Vol. 1, No. 3, pp. 1-9.

- Renukadevi G and Rajambal K (2012), "Performance Investigation of Multi-Phase VSI with Simple PWM Switching Techniques", *International Journal of Engineering*, Vol. 26, No. 1, pp. 289-296.
- Renukadevi G and Rajambal K (2013), "Novel PWM Technique for n<sup>th</sup> Harmonic Injection for N-Phase VSIs", IEEE-International Conference on Computation of Power, Energy Information & Communication (ICCPEIC-13), April 17-18, Adhiparasakthi Engineering College, Melmaruvathur.
- Rodríguez J, Wu B, Bernet S, Pontt J and Kouro S (2007), "Multilevel Voltage-Source- Converter Topologies for Industrial Medium-Voltage Drives", *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6, pp. 2930-2945.
- Shanthi B and Natarajan S P (2009), "Comparative Study on Uni Polar Multi Carrier PWM Strategies for Five Level Flying Capacitor Inverter", International Conference on Control Automation Communication and Energy Conservation, June 4-6.
- Yan Deng, Hongyan Wang, Chao Zhang, Lei Hu and Xiangning He (2005), "Multilevel PWM Methods Based on Control Degrees of Freedom Combination and its Theoretical Analysis", IEEE IAS Conference Record No. 0-7803-9208-6/05, pp.1692-1699.