International Journal of Electrical and Electronic Engineering & Telecommunications

ISSN 2319 – 2518 www.ijeetc.com
Special Issue, Vol. 1, No. 1, March 2015
National Level Technical Conference P&E- BiDD-2015

Research Paper

PROPOSED BUCK-BOOST CONVERTER COMBING KY AND BUCK CONVERTER

Nikhitha C[1]* and Sheryl Grace Colaco[1]

*Corresponding Author: Nikhitha C, ✉ nikkiroy.c@gmail.com

This paper presents a Buck-Boost converter that combines KY converter and the traditional Synchronously Rectified (SR) buck converter with positive output voltage. The operation of these converters in Continuous Conduction Mode (CCM) result in a non-pulsating output current that reduces output voltage ripples. The analysis is presented as by considering the input voltage of the KY converter from the input voltage source during magnetization period, whereas during the demagnetization period, the input voltage of the KY converter is derived from the output voltage of the SR buck converter. The simulation results indicate smaller ripple voltage in output. Using controller we can reduce these ripples to achieve steady state. These combined converters have no right half plane zero.

Keywords: CCM, KY converter, Buck-boost converter, SR buck converter, Right half plane zero

INTRODUCTION

KY Buck-Boost Converter uses four switches, thereby increases the cost (Hwu and Yau, 2009). To reduce number of switches, the KY and SR Buck converter is combined into Buck-Boost Converter so that both converters use same power switches. This converter has the non-pulsating output inductor current, hence output ripple is decreased and hence, the corresponding output voltage ripples is small. In this converters voltage across two energy transferring capacitors C_1 and C_2 are both D times input voltage. There are several non-isolated voltage buck/boosting converter (Luo, 1999; Chen *et al.*, 1999; Mohan *et al.*, 2003; Luo and Ye, 2003; and Zhu and Luo, 1988 and 2007).

Comparisons between this modified buck-boost converter and the KY converter are given below:

- Both these converters always operate in CCM.
- Both these converters have output inductors results in non-pulsating output currents.
- The modified converter has the voltage gain

[1] Department of Electrical and Electronics, St. Joseph Engineering College, Vamanjoor, India.

of 2D, and results in voltage bucking with the duty cycle is between 0 and 0.5 and voltage boosting with the duty cycle is between 0.5 and 1.

- The KY converter has the voltage gain of 1 + D, and hence results in voltage boosting with the duty cycle is between 0 and 1. Therefore maximum voltage conversion ratios for both are identical, equal to 2.
- Both these converters can operate bi-directionally. Comparison between converters is given in Axelrod *et al.* (2005).

PROPOSED CONVERTER STRUCTURE

Figure 1 shows block diagram of proposed converter.

Figure 1: Block Diagram of Proposed Converter

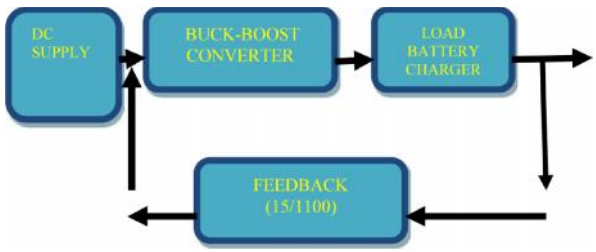
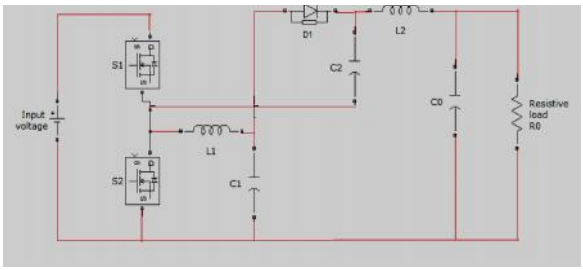


Figure 2: Circuit Diagram of Proposed Buck-Boost Converter

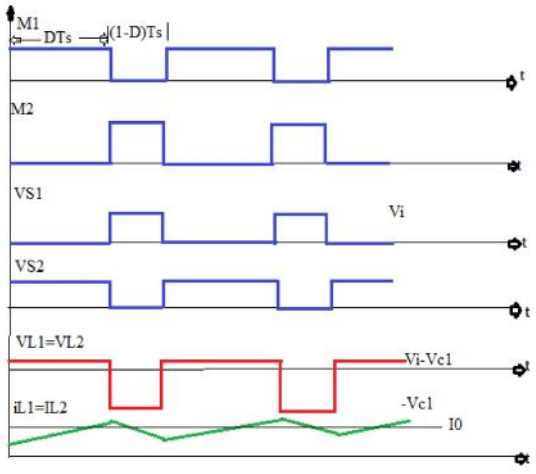


It combines two converters using same power switches. One is SR Buck converter, which uses two power switches S_1 and S_2, one inductor L_1 and one energy-transferring capacitor C_1, whereas other is KY Converter, which uses same two power switches S_1 and S_2, one power diode D_1 which is disconnected from the input voltage source and connected to the output of the SR buck converter, one energy transferring capacitor C_2, one output inductor L_2, and one output capacitor C_o. The output load is represented by R_o.

During S_1 being ON and S_2 being OFF, L_1 and L_2 are both magnetized. At this time, C_1 is charged, and hence, the voltage across C_1 is positive, whereas C_2 is reverse charged, and hence, the voltage across C_2 is negative. During the period with S_1 being OFF and S_2 being ON, L_1 and L_2 are both demagnetized, C_1 is discharged. Since C_2 is connected in parallel with C_1, C_2 is reverse charged with the voltage across C_2 being from negative to positive, and finally, the voltage across C_2 is the same as the voltage across C_1.

Timing sequence of proposed converter is shown in Figure 2 with ON period DTs and OFF period (1-*D*)Ts.

Figure 3: Key Waveforms of Proposed Converter



OPERATING PRINCIPLES

There are some assumptions made and some symbols are given to components.

- The values of C_1 and C_2 are large enough to keep V_{C1} and V_{C2} almost constant.
- DC input voltage is signified by V_i, the DC output voltage is represented by V_o, DC output current is expressed by I_o, the gate driving signals for S_1 and S_2 are indicated by M_1 and M_2, respectively, the voltages on S_1 and S_2 are represented by vS_1 and vS_2, respectively, the voltages on L_1 and L_2 are denoted by V_{L1} and V_{L2}, respectively, the currents in L_1 and L_2 are signified by i_{L1} and i_{L2}, and the input current is expressed by I_i.
- The currents flowing through L_1 and L_2 are both positive.

Since this converter operates in CCM, the turn-on and Off type is (D, 1 – D), where D is the duty cycle of the gate driving signal for S_1 and 1 – D is the duty cycle of the gate driving signal for S_2.

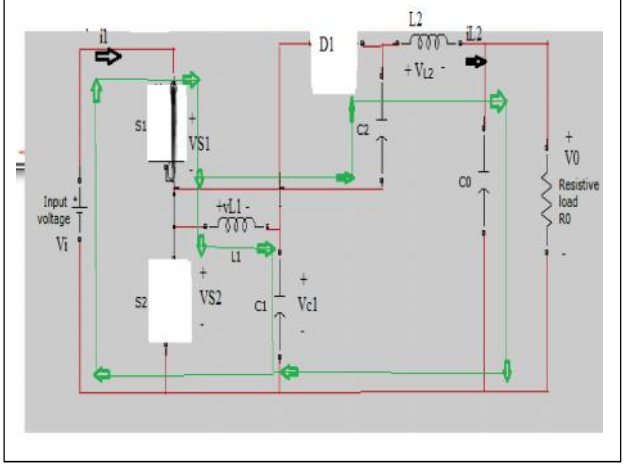
There are two operating modes to be discussed.

Mode 1

In this mode, S_1 is turned ON but S_2 is turned OFF. During this mode, the input voltage provides energy for L_1 and C_1. The voltage across L_1 is V_i minus V_{C1}, L_1 is magnetized now, and C_1 is charged. At the same time, the input voltage, together with C_2, provides the energy for L_2 and the output. Hence, the voltage across L_2 is V_i plus V_{C2} minus V_o, thereby L_2 to be magnetized, and C_2 is discharged. Therefore, the related equations are:

$$V_{L1} = V_i - V_{C1} \quad ...(1)$$

Figure 3: Current Flow in State 1



$$V_{L2} = V_i + V_{C2} - V_o \quad ...(2)$$

Mode 2

In this mode, S_1 is turned OFF but S_2 is turned ON. During this mode, the energy stored in L_1 and C_1 is released to C_2 and the output via L_2. The voltage across L_1 is minus V_{C1}, thereby L_1 to be demagnetized, and C_1 is discharged. At this same time, the voltage across L_2 is V_{C2} minus V_o, thereby causing L_2 to be demagnetized, and C_2 is charged.

Therefore, the related equations are given below:

$$V_{L1} = -V_{C1} \quad ...(3)$$

$$V_{L2} = V_{C2} - V_o \quad ...(4)$$

$$V_{C2} = V_{C1} \quad ...(5)$$

By applying the voltage-second balance to (1) and (3), the following equation is obtained.

$$(V_i - V_{C1})*D*Ts + (-V_{C1}) * (1 - D)*Ts \quad ...(6)$$

$$V_{C1} = DV_i \quad ...(7)$$

By applying the voltage-second balance to (2) and (4), the following equation is obtained.

$$(V_i + V_{C2} - V_o)*D*Ts + (V_{C2} - V_o) * (1 - D)*Ts = 0 \quad ...(8)$$

By substituting (5) and (7) into (8), the voltage conversion ratio of the modified Buck-Boost converter can be obtained as

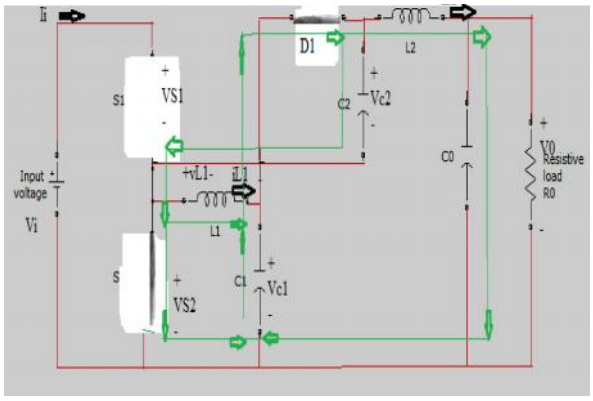
$$V_o/V_i = 2*D \quad ...(9)$$

Therefore, such a converter can operate in the buck mode when the duty cycle D is smaller than 0.5, whereas it can operate in the boost mode when D is larger than 0.5.

Based on (5), (7), and (9), the dc voltages across C_1 and C_2 can be expressed to be

$$V_{C1} = V_{C2} = 0.5V_o \quad ...(10)$$

Figure 4: Current Flow in State 2



KEY DESIGN SPECIFICATIONS

Some specifications to design proposed converters are given as follows:

a. DC input voltage V_i is varies from 20 V to 30 V.

b. DC output voltage is 24 V.

c. Rated DC load current I_0-rated is 0.417 A.

d. The switching frequency fs is 200 KHZ.

e. Product name of S_1 and S_2 is IRFZ44.

f. Driver IC is IR2110.

g. Product name of D_1 is 1N4007.

Inductor Design

The peak values of inductor currents i_{L1} and i_{L2} are expressed by Δi_{L1} and Δi_{L2} respectively.

These can be obtained as 10% of i_{L1} and i_{L2}.

Therefore $\Delta i_{L1} = \Delta i_{L2} = 0.1\ I_0$-rated = 0.0417 A ...(11)

$$L_1 \geq D_{min}\ (V_i - V_{C1})/\Delta i_{L1}\ f_s \quad ...(12)$$

$$L_2 \geq D_{min}(V_i + V_{C2} - V_o)/\Delta i_{L2}\ f_s \quad ...(13)$$

Inductor value designed as follows:

Table 1: Inductor Values for Different Duty Cycle and Input Voltages

V_i(V)	$D = V_0/2V_i = 24/2V_i$	L(«H)
20	0.6 = D_{max}	383
21	0.571	432
22	0.545	479
23	0.522	527
24	0.50	575
25	0.48	623
26	0.462	670
27	0.444	719
28	0.428	767
29	0.413	815
30	0.40 = D_{min}	862 = $L_1 = L_2$

Therefore maximum values of L_1 and L_2 are chosen for high input voltage of 30 V and corresponding duty cycle $D_{min} = 0.4$.

Capacitor Design

Output Capacitor Design: High value of output capacitor C_0 is chosen to have small output voltage ripples. In this design C_0-value taken is 470 «F to make output voltage ripple is 1% of DC output voltage.

Energy Transferring Capacitor Design: Prior to design of converter, variations in V_{C1} and V_{C2} are assumed to be quite small. And

Table 2: Capacitor values for different duty cycle and input voltages

$V_i(V)$	$D = V_0/2V_i = 24/2V_i$	$C(\mu F)$
20	0.6 = D_{max}	104.25
21	0.571	104.30
22	0.545	104.30
23	0.522	104.20
24	0.50	104.25
25	0.48	104.25
26	0.462	104.41
27	0.444	104.35
28	0.428	104.38
29	0.413	104.45 = $C_1 = C_2$
30	0.40 = D_{min}	104.25

assumed to be smaller than 1% of V_{C1} and V_{C2}. In state 1 C_1 is charged and in state 2 C_2 is discharged.

$$C_1 \geq I_o - \text{rated} * D_{max}/\Delta V_{C1} * f_s \quad ...(15)$$

$$C_2 \geq I_o - \text{rated} * D_{max}/\Delta V_{C1} * f_s \quad ...(16)$$

Since the maximum duty cycle D_{max} occurs at the input voltage of 20 V, namely 0.6. Both the values of C_1 and C_2 are not less than 104.25 μF.

Resistor Design

Designed output voltage is 24 V and rated load current is 0.417 A.

Therefore,

$R_0 = V_0/I_0 = 24/0.417 = 57.55\Omega$

Designed values are

$L_1 > = L_2 > = 862\ \mu H$

$C_1 > = C_2 > = 104.45\ \mu F$

$C_0 = 470\ \mu F$

$R_0 = 57.55\ \Omega$

SIMULATION RESULTS

The Simulation has been implemented in Matlab/Simulink software. This model uses switching frequency of 200 KHZ. Proposed converter uses resistor as load for simulation. This load is replaced by battery charger for hardware implementation. Figure 5 shows Simulink model of closed loop proposed converter. Figure 6 shows subsystem of PI controller with *Kp* = 15 and *Ki* = 1100. By trial and error method we chose proportional and integral gain such that output voltage to be maintained at 24 V. Ramp and reference DC signal is compared with these gains to get pulses, which drives switches S_1 and S_2.

Figure 5: Simulink Model of Closed Loop Proposed Converter

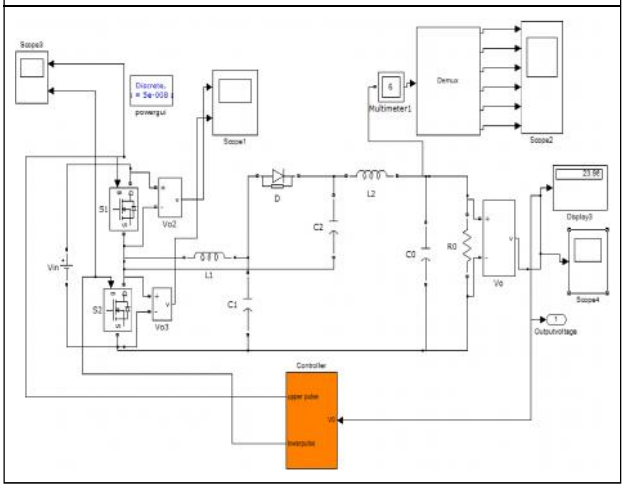


Figure 6: Subsystem of Controller

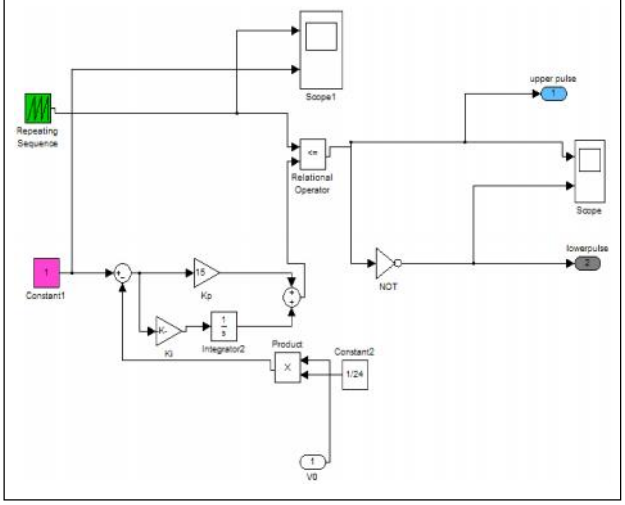


Figure 7 shows Simulink waveforms of voltage across L_1. Figure 8 shows current in L_1 and L_2. Figure 9 shows voltage across L_2. Figure 9 shows output voltage of closed loop simulation. Figure 10 shows Simulink model for supply variations. Here input is replaced by continuous voltage source and step. Figure 11 shows output for supply variations.

Figure 12 shows Simulink model for load variations. Resistive load is compared with step input. For first step time it takes R_0 as load and for next time it takes parallel combination of R_0 and R_1. Figure 13 shows output for load variations.

Figure 7: Waveform of Voltage Across L_1

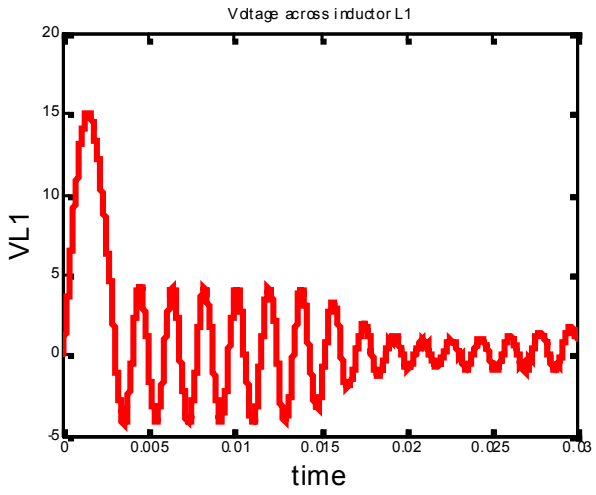


Figure 8: Waveform of Current in L_1 and L_2

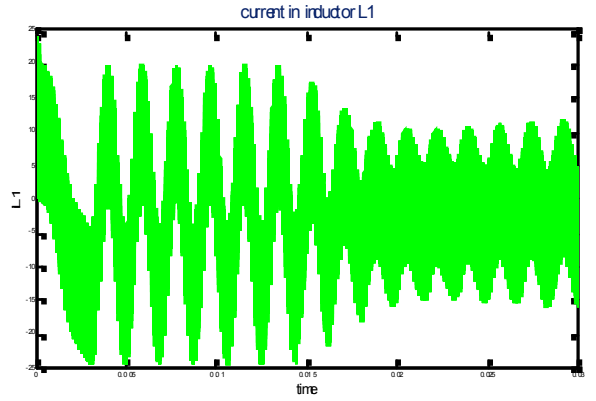


Figure 9: Waveform of Voltage Across L_2

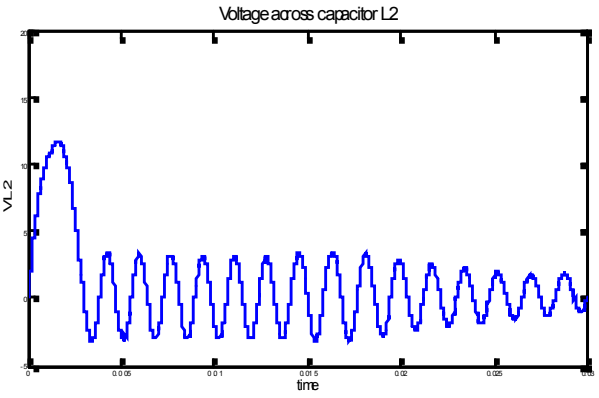


Figure 10: Waveform of Output Load Voltage of Closed Loop

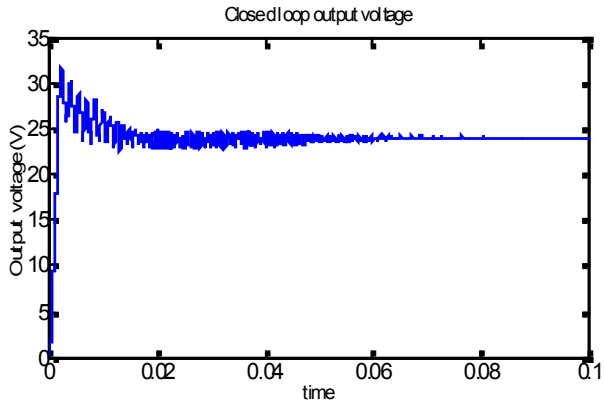


Figure 11: Simulink Model for Supply Variations

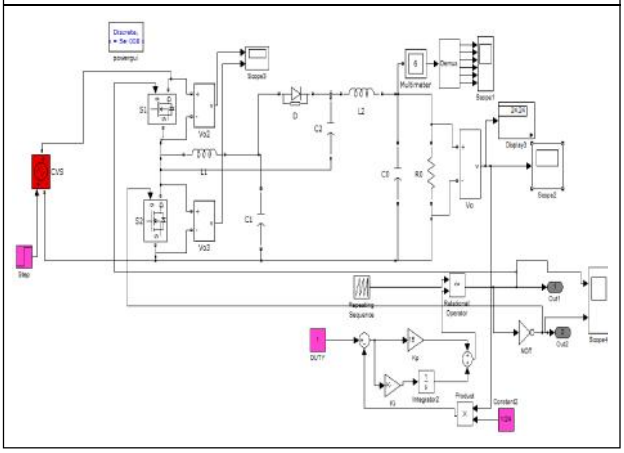


Figure 12: Waveform of Supply Variations

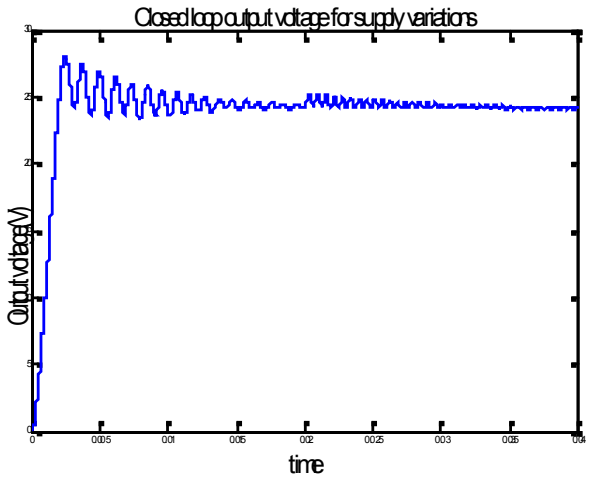


Figure 13: Simulink Model for Load Variations

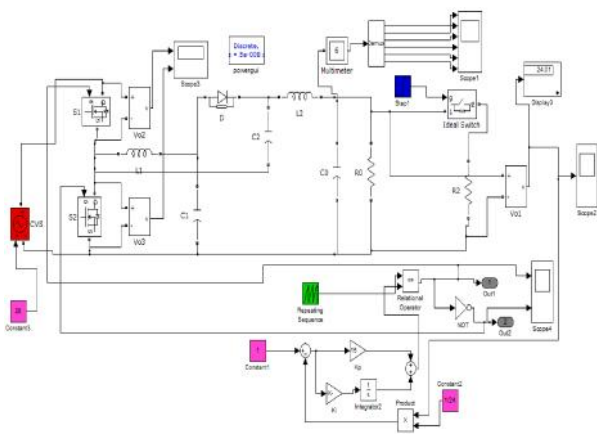
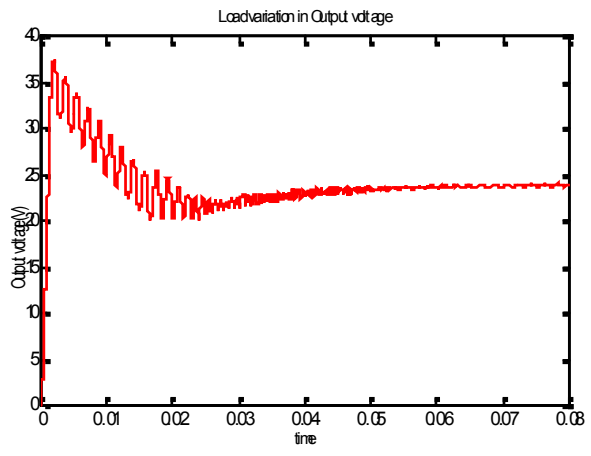


Figure 14: Waveform for Load Variations



CONCLUSION

Proposed converter always operates on CCM, thereby causing variations in duty cycle, hence controller is necessary. These converter produces non-pulsating output current, hence reduces current stress on output capacitor. Both the converters use same power switches hence size is reduced and cost also reduced. From simulation we can see that for any input voltage, the proposed converter can stably work with constant output voltage of 24 V.

ACKNOWLEDGMENT

I would like to acknowledge the most sincere appreciation to all the authors mentioned in reference papers that made this paper easier for simulation.

I would like to express my deepest gratitude and sincere thanks to Principal, HOD of Electrical and Electronics Department and also to my project guide of St. Joseph Engineering College, Vamanjoor for their support and guidance.

REFERENCES

1. Axelrod B, Berkovich Y and Ioinovici A (2005), “Hybrid Switched-Capacitor-Cuk/ Zeta/Sepic Converters in Step-Up Mode”, Proc. IEEE Int. Symp. Circuits Syst., pp. 1310-1313.
2. Chen X, Luo F L and Ye H (1999), “Modified Positive Output Luo Converter”, in Proc. IEEE Int. Conf. Power Electron. Drive Syst., pp. 450-455.
3. Hwu K I and Yau Y T (2009), “Two Types of KY Buck-Boost Converters”, *IEEE Trans. Ind. Electron.*, Vol. 56, No. 8, pp. 2970-2980.

4. Luo F L (1999), "Positive Output Luo Converters: Voltage Lift Technique", *IEEE Proc. Elect. Power Appl.*, Vol. 4, No. 146, pp. 415-432.
5. Luo F L and Ye H (2003), "Positive Output Super-Lift Converters", *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 105-113.
6. Mohan N, Undeland T M and Robbins W P (2003), *Power Electronics*, 2nd Edition, Willey, New York.
7. Zhu M and Luo F L (2007), "Development of Voltage Lift Technique on Doubleoutput Transformerless DC-DC Converter", in Proc. 33rd Annu Conf. Ind. Electron. Soc., pp. 1983-1988.
8. Zhu M and Luo L (2007), "Implementing of Developed Voltage Lift Technique on SEPIC, Cuk and Double-Output DC-DC Converters", in Proc. IEEE Int. Conf. Ind. Electron., pp. 674-681.