This paper presents a Buck-Boost converter that combines KY converter and the traditional Synchronously Rectified (SR) buck converter with positive output voltage. The operation of these converters in Continuous Conduction Mode (CCM) result in a non-pulsating output current that reduces output voltage ripples. The analysis is presented as by considering the input voltage of the KY converter from the input voltage source during magnetization period, whereas during the demagnetization period, the input voltage of the KY converter is derived from the output voltage of the SR buck converter. The simulation results indicate smaller ripple voltage in output. Using controller we can reduce these ripples to achieve steady state. These combined converters have no right half plane zero.

**Keywords:** CCM, KY converter, Buck-boost converter, SR buck converter, Right half plane zero

**INTRODUCTION**

KY Buck-Boost Converter uses four switches, thereby increases the cost (Hwu and Yau, 2009). To reduce number of switches, the KY and SR Buck converter is combined into Buck-Boost Converter so that both converters use same power switches. This converter has the non-pulsating output inductor current, hence output ripple is decreased and hence, the corresponding output voltage ripples is small. In this converters voltage across two energy transferring capacitors $C_1$ and $C_2$ are both $D$ times input voltage. There are several non-isolated voltage buck/boosting converter (Luo, 1999; Chen et al., 1999; Mohan et al., 2003; Luo and Ye, 2003; and Zhu and Luo, 1988 and 2007).

Comparisons between this modified buck-boost converter and the KY converter are given below:

- Both these converters always operate in CCM.
- Both these converters have output inductors results in non-pulsating output currents.
- The modified converter has the voltage gain...
of 2D, and results in voltage bucking with the duty cycle is between 0 and 0.5 and voltage boosting with the duty cycle is between 0.5 and 1.

- The KY converter has the voltage gain of 1 + D, and hence results in voltage boosting with the duty cycle is between 0 and 1. Therefore maximum voltage conversion ratios for both are identical, equal to 2.

- Both these converters can operate bi-directionally. Comparison between converters is given in Axelrod et al. (2005).

PROPOSED CONVERTER STRUCTURE

Figure 1 shows block diagram of proposed converter.

It combines two converters using same power switches. One is SR Buck converter, which uses two power switches $S_1$ and $S_2$, one inductor $L_1$ and one energy-transferring capacitor $C_1$, whereas other is KY Converter, which uses same two power switches $S_1$ and $S_2$, one power diode $D_1$ which is disconnected from the input voltage source and connected to the output of the SR buck converter, one energy transferring capacitor $C_2$, one output inductor $L_2$, and one output capacitor $C_o$. The output load is represented by $R_o$.

During $S_1$ being ON and $S_2$ being OFF, $L_1$ and $L_2$ are both magnetized. At this time, $C_1$ is charged, and hence, the voltage across $C_1$ is positive, whereas $C_2$ is reverse charged, and hence, the voltage across $C_2$ is negative. During the period with $S_1$ being OFF and $S_2$ being ON, $L_1$ and $L_2$ are both demagnetized, $C_1$ is discharged. Since $C_2$ is connected in parallel with $C_1$, $C_2$ is reverse charged with the voltage across $C_2$ being from negative to positive, and finally, the voltage across $C_2$ is the same as the voltage across $C_1$.

Timing sequence of proposed converter is shown in Figure 2 with ON period $DT_s$ and OFF period $(1-D)T_s$.

Figure 3: Key Waveforms of Proposed Converter
OPERATING PRINCIPLES

There are some assumptions made and some symbols are given to components.

- The values of \( C_1 \) and \( C_2 \) are large enough to keep \( V_{C1} \) and \( V_{C2} \) almost constant.
- DC input voltage is signified by \( V_i \), the DC output voltage is represented by \( V_o \), DC output current is expressed by \( I_o \), the gate driving signals for \( S_1 \) and \( S_2 \) are indicated by \( M_1 \) and \( M_2 \), respectively, the voltages on \( S_1 \) and \( S_2 \) are represented by \( v_{S1} \) and \( v_{S2} \), respectively, the voltages on \( L_1 \) and \( L_2 \) are denoted by \( V_{L1} \) and \( V_{L2} \), respectively, the currents in \( L_1 \) and \( L_2 \) are signified by \( i_{L1} \) and \( i_{L2} \), and the input current is expressed by \( I_i \).
- The currents flowing through \( L_1 \) and \( L_2 \) are both positive.

Since this converter operates in CCM, the turn-on and Off type is \((D, 1 – D)\), where \( D \) is the duty cycle of the gate driving signal for \( S_1 \) and \( 1 – D \) is the duty cycle of the gate driving signal for \( S_2 \).

There are two operating modes to be discussed.

**Mode 1**

In this mode, \( S_1 \) is turned ON but \( S_2 \) is turned OFF. During this mode, the energy stored in \( L_1 \) and \( C_1 \) is released to \( C_2 \) and the output via \( L_2 \). The voltage across \( L_1 \) is \( V_i \) minus \( V_{C1} \), thereby causing \( L_1 \) to be demagnetized, and \( C_1 \) is charged. At the same time, the voltage across \( L_2 \) is \( V_{C2} \) minus \( V_o \), thereby causing \( L_2 \) to be demagnetized, and \( C_2 \) is charged.

Therefore, the related equations are given below:

\[
V_{L1} = V_i - V_{C1} \quad \text{...(1)}
\]

\[
V_{L2} = V_{C2} - V_o \quad \text{...(2)}
\]

\[
V_{C2} = V_{C1} \quad \text{...(5)}
\]

By applying the voltage-second balance to (1) and (3), the following equation is obtained.

\[
(V_i - V_{C1})^* D^* Ts + (-V_{C1})^* (1 - D)^* Ts = 0 \quad \text{...(6)}
\]

**Mode 2**

In this mode, \( S_1 \) is turned OFF but \( S_2 \) is turned ON. During this mode, the input voltage provides energy for \( L_1 \) and \( C_1 \). The voltage across \( L_1 \) is \( V_i \) minus \( V_{C1} \), \( L_1 \) is magnetized now, and \( C_1 \) is charged. At the same time, the voltage across \( L_2 \) is \( V_{C2} \) minus \( V_o \), thereby causing \( L_2 \) to be demagnetized, and \( C_2 \) is charged.

Therefore, the related equations are given below:

\[
V_{L1} = -V_{C1} \quad \text{...(3)}
\]

\[
V_{L2} = V_{C2} - V_o \quad \text{...(4)}
\]

\[
V_{C2} = V_{C1} \quad \text{...(5)}
\]

By applying the voltage-second balance to (2) and (4), the following equation is obtained.

\[
(V_i + V_{C2} - V_o)^* D^* Ts + (V_{C2} - V_o)^* (1 - D)^* Ts = 0 \quad \text{...(8)}
\]
By substituting (5) and (7) into (8), the voltage conversion ratio of the modified Buck-Boost converter can be obtained as

\[ V_o/V_i = 2* D \]  \hspace{1cm} (9)

Therefore, such a converter can operate in the buck mode when the duty cycle \( D \) is smaller than 0.5, whereas it can operate in the boost mode when \( D \) is larger than 0.5.

Based on (5), (7), and (9), the dc voltages across \( C_1 \) and \( C_2 \) can be expressed to be

\[ V_{C1} = V_{C2} = 0.5V_o \]  \hspace{1cm} (10)

**Inductor Design**

The peak values of inductor currents \( i_{L1} \) and \( i_{L2} \) are expressed by \( \Delta i_{L1} \) and \( \Delta i_{L2} \) respectively.

These can be obtained as 10\% of \( i_{L1} \) and \( i_{L2} \).

Therefore \( \Delta i_{L1} = \Delta i_{L2} = 0.1 \) \( I_0 \)-rated = 0.0417 A \hspace{1cm} (11)

\[ L_1 \geq D_{min} (V_i - V_{C1})/\Delta i_{L1} f_s \]  \hspace{1cm} (12)

\[ L_2 \geq D_{min} (V_i + V_{C2} - V_o)/\Delta i_{L2} f_s \]  \hspace{1cm} (13)

Inductor value designed as follows:

<table>
<thead>
<tr>
<th>( V_i ) (V)</th>
<th>( D ) = ( V_i/2V_i = 24/2V_i )</th>
<th>( L(\mu H) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.6 = ( D_{max} )</td>
<td>383</td>
</tr>
<tr>
<td>21</td>
<td>0.571</td>
<td>432</td>
</tr>
<tr>
<td>22</td>
<td>0.545</td>
<td>479</td>
</tr>
<tr>
<td>23</td>
<td>0.522</td>
<td>527</td>
</tr>
<tr>
<td>24</td>
<td>0.50</td>
<td>575</td>
</tr>
<tr>
<td>25</td>
<td>0.48</td>
<td>623</td>
</tr>
<tr>
<td>26</td>
<td>0.462</td>
<td>670</td>
</tr>
<tr>
<td>27</td>
<td>0.444</td>
<td>719</td>
</tr>
<tr>
<td>28</td>
<td>0.428</td>
<td>767</td>
</tr>
<tr>
<td>29</td>
<td>0.413</td>
<td>815</td>
</tr>
<tr>
<td>30</td>
<td>0.40 = ( D_{min} )</td>
<td>862 = ( L_1 = L_2 )</td>
</tr>
</tbody>
</table>

Table 1: Inductor Values for Different Duty Cycle and Input Voltages

Therefore maximum values of \( L_1 \) and \( L_2 \) are chosen for high input voltage of 30 V and corresponding duty cycle \( D_{min} = 0.4 \).

**Capacitor Design**

**Output Capacitor Design:** High value of output capacitor \( C_0 \) is chosen to have small output voltage ripples. In this design \( C_0 \) value taken is 470 \( \mu F \) to make output voltage ripple is 1\% of DC output voltage.

**Energy Transferring Capacitor Design:** Prior to design of converter, variations in \( V_{C1} \) and \( V_{C2} \) are assumed to be quite small. And
assumed to be smaller than 1% of $V_{C1}$ and $V_{C2}$.

In state 1 $C_1$ is charged and in state 2 $C_2$ is discharged.

$$C_1 \geq I_o - \text{rated} \cdot \frac{D_{\max}}{\Delta V_{C1}} \cdot f_s \quad \text{...(15)}$$

$$C_2 \geq I_o - \text{rated} \cdot \frac{D_{\max}}{\Delta V_{C1}} \cdot f_s \quad \text{...(16)}$$

Since the maximum duty cycle $D_{\max}$ occurs at the input voltage of 20 V, namely 0.6. Both the values of $C_1$ and $C_2$ are not less than 104.25 $\mu$F.

**Resistor Design**

Designed output voltage is 24 V and rated load current is 0.417 A.

Therefore,

$$R_0 = \frac{V_o}{I_o} = \frac{24}{0.417} = 57.55 \Omega$$

Designed values are

$$L_1 > = L_2 > = 862 \mu H$$

$$C_1 > = C_2 > = 104.45 \mu F$$

$$C_0 = 470 \mu F$$

$$R_0 = 57.55 \Omega$$

**SIMULATION RESULTS**

The Simulation has been implemented in Matlab/Simulink software. This model uses switching frequency of 200 KHZ. Proposed converter uses resistor as load for simulation. This load is replaced by battery charger for hardware implementation. Figure 5 shows Simulink model of closed loop proposed converter. Figure 6 shows subsystem of PI controller with $K_p = 15$ and $K_i = 1100$. By trial and error method we chose proportional and integral gain such that output voltage to be maintained at 24 V. Ramp and reference DC signal is compared with these gains to get pulses, which drives switches $S_1$ and $S_2$. 

<table>
<thead>
<tr>
<th>$V_i$ (V)</th>
<th>$D = \frac{V_i}{2V} = \frac{24}{2V_i}$</th>
<th>$C$ ($\mu$F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.6 $D_{\max}$</td>
<td>104.25</td>
</tr>
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<td>21</td>
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<tr>
<td>30</td>
<td>0.40 $D_{\min}$</td>
<td>104.25</td>
</tr>
</tbody>
</table>
Figure 7 shows Simulink waveforms of voltage across $L_1$. Figure 8 shows current in $L_1$ and $L_2$. Figure 9 shows voltage across $L_2$. Figure 9 shows output voltage of closed loop simulation. Figure 10 shows Simulink model for supply variations. Here input is replaced by continuous voltage source and step. Figure 11 shows output for supply variations.

Figure 12 shows Simulink model for load variations. Resistive load is compared with step input. For first step time it takes $R_0$ as load and for next time it takes parallel combination of $R_0$ and $R_1$. Figure 13 shows output for load variations.
CONCLUSION

Proposed converter always operates on CCM, thereby causing variations in duty cycle, hence controller is necessary. These converter produces non-pulsating output current, hence reduces current stress on output capacitor. Both the converters use same power switches hence size is reduced and cost also reduced. From simulation we can see that for any input voltage, the proposed converter can stably work with constant output voltage of 24 V.

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REFERENCES


