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Research Paper

REDUCTION OF POWER ELECTRONIC SWITCHES FOR THREE PHASE MULTI LEVEL INVERTER FED DRIVE APPLICATIONS

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In this paper a new toplogy has been introduced that reduces number of switches required for higher number of output levels. By this complexity in switching can be also decreased. This is achieved by using an alternate DC source that is linked in opposite polarities via power switches. It requires only a few number of switches when compared to the classical topologies. The proposed system is examined with the help of a three phase, multilevel inverter. The overall Total Harmonic Distortion (THD) of the multilevel inverter is also reduced by using motor load along with the Fuzzy controller. A MATLAB/Simulink based model was developed and simulation results are presented.

Keywords: Classical topologies, Multilevel inverter, Total Harmonic Distortion (THD), Fuzzy-controller

INTRODUCTION

Today, energy saving is the major aspect of the industrialized countries, and nearly 70% of electric energy is consumed by electric motor and about 60% of mechanical energy is obtained throughthe pump and induction motor with conversion of electrical energy. Thus, it is important for considering energy savings in these types of drives. Need of Medium-Voltage (MV) drives fans and high power pumps, keeps on increasing. MV machine designs offers to the improvements of electric power components in thermal performance and cost saving.

Multilevel converters and inverters are the adequate power conversion technology for high voltage and high power applications such as Motor Drives, transportation systems and industrial motor drivesand even forpower grids, High Voltage Direct Current transmissions (HVDC), especially in Distributed Generation systems (DG), Flexible AC Transmission Systems (FACTS) devices and electrical drives.

There are many switching strategies used nowadays, which are applied mainly to the multilevel inverter topologies, they are Diode-clamped multilevelinverter, Flying-

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capacitor multilevel inverter, Cascade Multilevel inverter.

Multilevel inverter has the output voltage in step of smaller increments in a large number of switching states.This results in minimum switching loss and less harmonics. Further, the lower dv/dt (voltage stress) reduces the leakage current.

CASCADED H-BRIDGE MULTILEVEL INVERTER STRUCTURE

In the family of multilevel and multi-pulse inverters, conventional cascaded multilevel inverter plays a vital role. To achieve a desired AC voltage several numbers of DC sources are connected back to back fashion.

The DC voltage levels are considered to be identical, the DC voltage means either fuel cells or photovoltaic's, natural choice, batteries, etc., in Cascaded H-Bridge inverter requires only a least number of components when compared to diode-clamped and flying capacitors type multilevel inverters and no specially designed transformer are needed as compared to multi pulse inverter.

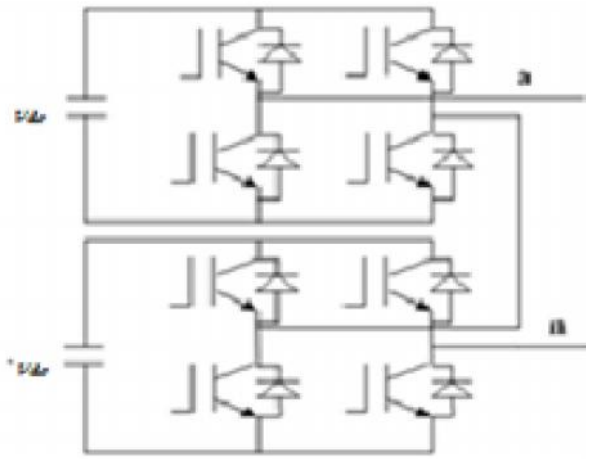
A separate DC sources are required for cascaded multi-level inverter connected in cascaded manner as shown in the figure. The different combinations of the four switches S1, S2, S3, and S4 can be obtained by connecting the DC source to Ac output side

The output voltage of overall multilevel inverter can be given by the following equation

$$V_0 = V_{01} + V_{02} + V_{03} + V_{0n}$$

Consider the five level inverter with 8 IGBT switches and two DC sources. Each H-bridge has three carrier output voltage such as $+V_{dc}$, $-V_{dc}$ and zero volts

Figure 1: Cascaded H-Bridge Inverter



The cascaded H-bridge multilevel inverter introduces the idea of using Separate DC sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC sources V_{dc}. By cascading the AC output of each H-bridge inverter, an AC voltage waveform is developed. By closing the required switches, each H-bridge inverter can produce five different voltages $+V_{dc}$, $+ V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$. In proposed system concentration paid over only to number of switches.

Figure 2: Output Waveform

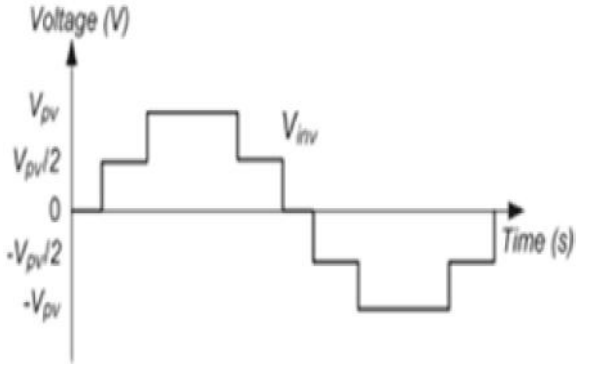
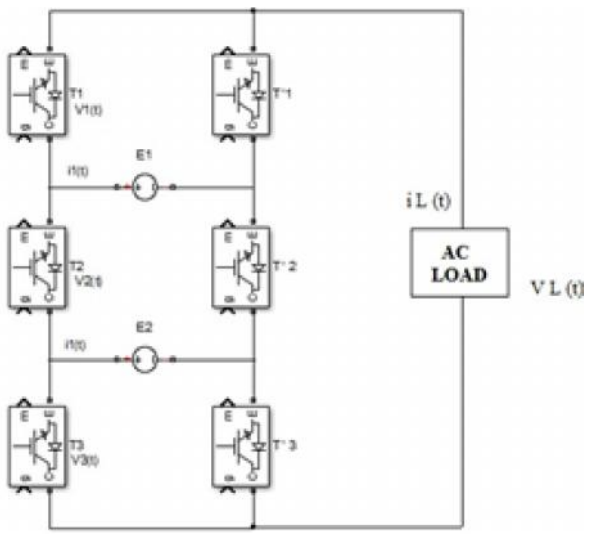


Figure 3: Single Phase Inverter Based on the Proposed Topology



PROPOSED TOPOLOGY

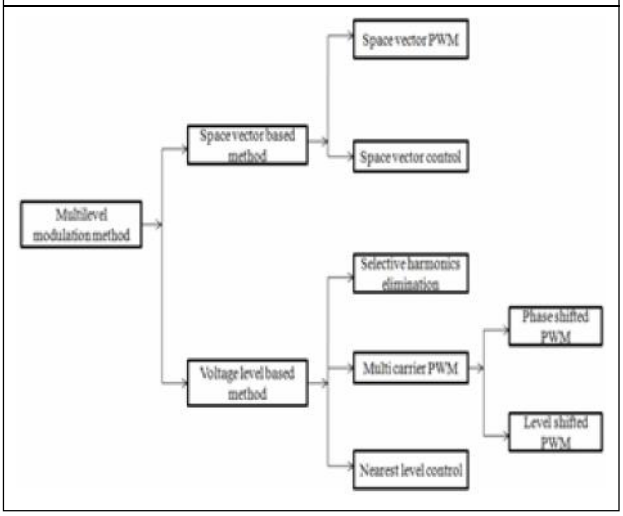
The structure of the proposed topology is introduced and its working principle is explained with the help of a single phase five level inverter.

MODULATION TECHNIQUES

A Definition of Modulation

Mainly the power electronic converters are operated in the "mode of switching". The working of switches in the converter has been always in either one of the two states-turned on (saturated with only a small voltage drop across the switch) or turned off (no current flows), which is termed asswitched mode. Here the switches are alternated between the on and off stage in order to control the power flow in the converter. The switched component is attenuated and the desired DC or low frequency AC component is obtained. This process is called Pulse Width Modulation (PWM), since the average value is controlled by modulating the width of the pulses.

Figure 4: Modulation Strategies for Multilevel Inverter

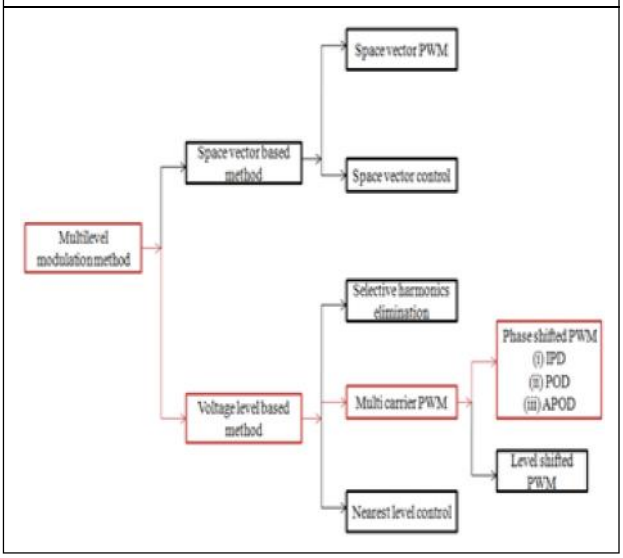


Phase Shifted Modulation

Classification of Control Strategies

In multilevel inverter the main aim of the modulation strategy is to synthesize the output voltage as close as possible to the sinusoidal waveform. To reduce the harmonic content and switching loss various modulation techniques have been developed so far. Based on the switching frequency, the modulation

Figure 5: Various Multilevel Modulation Techniques



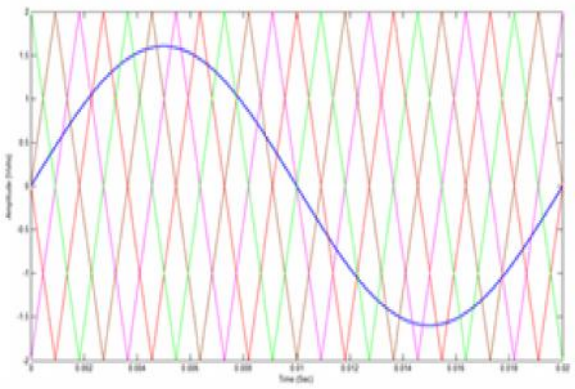
techniques used in multilevel inverters can be classified as shown in Figure 5. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. The classic carrier-based Sinusoidal PWM (SPWM) a very popular method of industrial application that uses the phase shifting technique to reduce the harmonics in the load voltage.

This work is the intersection of a sine wave with a triangular wave to generate firing pulses.

Phase Shift PWM (PSPWM) Strategy

The phase shift multicarrier PWM technique which is shown in (Figure 6) uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltages. The gate signals for the chosen inverter can be derived directly by the comparison of the carrier with the sinusoidal reference.

Figure 6: Carrierar Ranges for PSPWM Strategy (m_a = 0. 8 and m_f = 40)



Induction Motor

It is robust, more reliable and also they can operate in both dirt and explosive environments. This type of motors requires less investment cost, and requires little maintenances with high efficiency compared to other types of motors. The above mentioned features make them attractive for its applications such as industrial drives. The induction motor considered for the simulation studies has the following parameters:

Table 1: Parameters of Typical Induction Motor

Parameters of Typical Induction Machine	
Stator resistance (Rs)	6.03
Rotor resistance (Rr)	6.085
Stator inductance (Ls)	489.3e-3
Rotor inductance (Lr)	489.3e-3
Mutual inductance (M)	450.3e-3
Poles (P)	4
Inertia (J)	0.00488

FUZZY LOGIC CONTROL

Fuzzy logic control is developed in this work to obtain desired output voltage and minimize the harmonics of the chosen inverter. According to these criteria, a rule base is derived as in Table 2.

Table 2: Fuzzy Rule Developed for Cascaded MLI

e\ce	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NM	NM	NS	NS	Z
NM	NB	NM	NM	NS	NS	Z	PS
NS	NM	NM	NS	NS	Z	PS	PS
Z	NM	NS	NS	Z	PS	PS	PM
PS	NS	NS	Z	PS	PS	PM	PM
PM	NS	Z	PS	PS	PM	PM	PB
PB	Z	PS	PS	PM	PM	PB	PB

SIMULATION RESULTS

The three phase cascaded H-bridge five level inverter is modelled in SIMULINK using power

system block set. The performance of the proposed modified cascaded multilevel inverter for induction motor drive is verified through the simulation results. It can be seen from Figure 10 output voltages for three phase MLI. Figure 11 shows the simulation diagram of three phase cascaded multilevel inverter for induction motor drive. From that multilevel inverter five level can be easily achieved by making the switching pulse sequences as shown in Figure 7. The Figures 12 and 13, shows the MATLAB simulation output waveform of speed and torque curve of induction motor. From the speed and torque characteristics curves, it is concreted that rated speed is achieved within 0.01 msec and the torque is quickly settled at 0.1 msec.

Figure 7: Simulation Diagram of Three Phase Multilevel Inverter

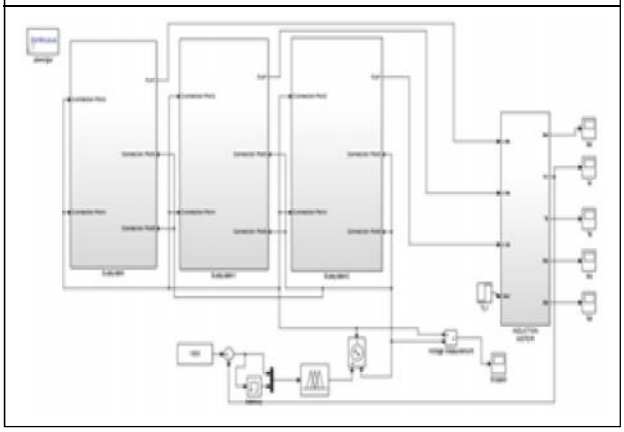


Figure 8: Single Phase Output Voltage Waveform for Cascaded H-Bridge Multilevel Inverter

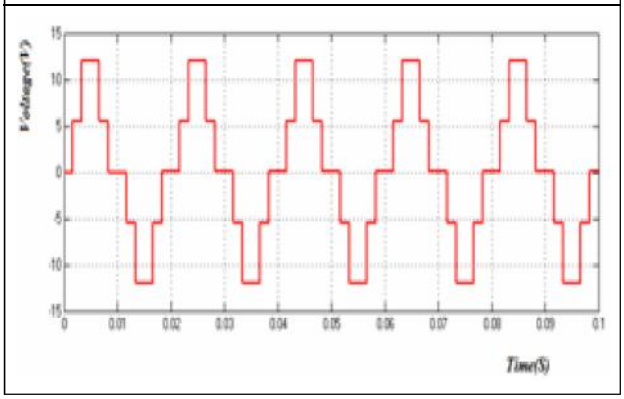


Figure 9: Output Voltage Waveform of Cascaded H-Bridge Multilevel Inverter for Single Phase Carrier

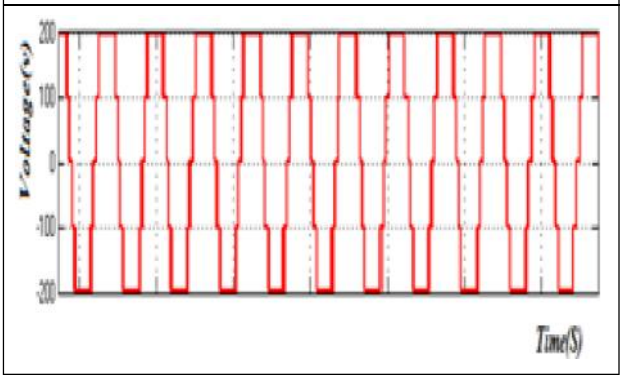


Figure 10: Three Phase Voltage Waveform for Cascaded H-Bridge Multilevel Inverter

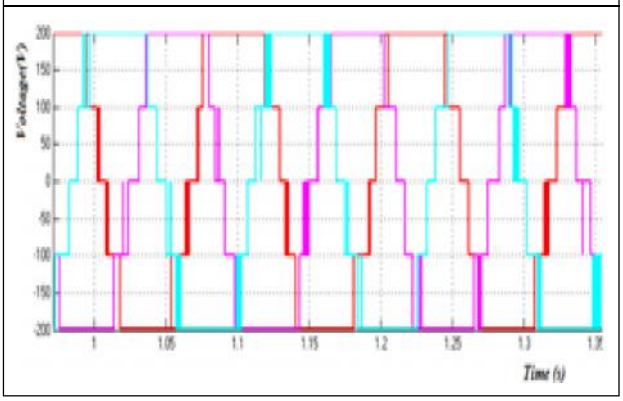


Figure 11: Three Phase Output Current Waveform for Cascaded H-Bridge Multilevel Inverter

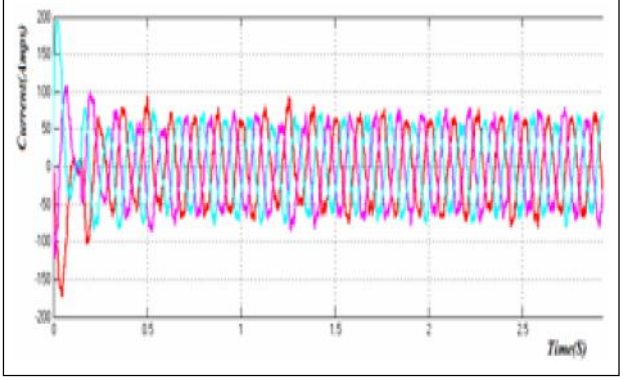


Figure 12: Speed Curve of a Cascaded H-Bridge Multilevel Inverter Fed Induction Motor Drive

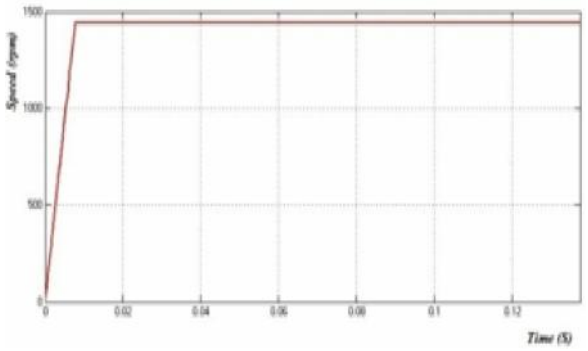


Figure 13: Torque Curve of a Cascaded H-Bridge Multilevel Inverter Fed Induction Motor Drive

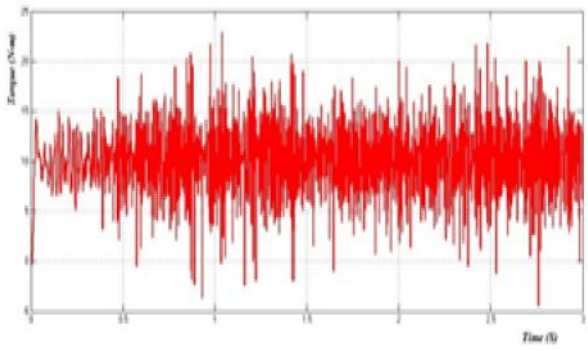


Figure 14: Stator Current Waveform of Cascaded H-Bridge Multilevel Inverter Fed Induction Motor Drive

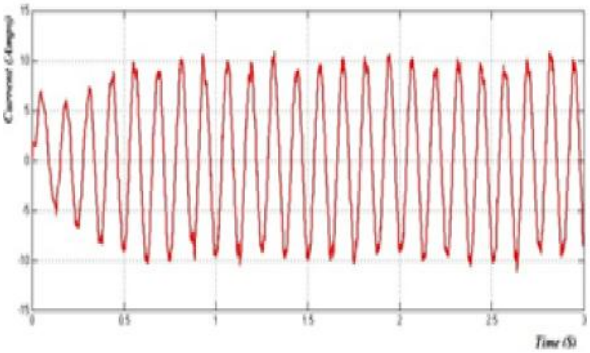
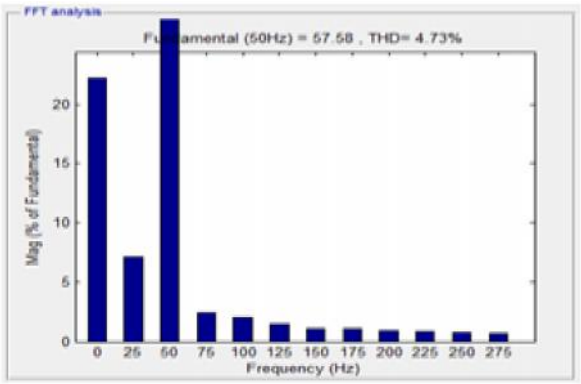


Figure 14 shows the stator current waveform of induction motor. By varying the frequency of multilevel inverter the proposed multilevel inverter can be used for variable speed drives. From FFT analysis, it can be derived that when the number of levels is increased, the harmonic content and total harmonics distortion is reduced. Figure 15 shows THD value of proposed five level inverter.

Figure 15: FFT Analysis for Five Level Cascaded Multilevel Inverter



CONCLUSION

A novel topology for MLI has been proposed in this paper is to reduce the device count. Here harmonics content can be reduced in aappreciable form. In this work the simulation results of three phase five level cascaded H-bridge multilevel inverter fed Induction Motor load with various modulating strategies are obtained through MATLAB/SIMULINK platform. The outputs like a phase voltage, THD spectrum for phase voltage, and torque-speed characteristics of induction motor are obtained.

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