International Journal of Electrical and Electronic Engineering & Telecommunications

ISSN 2319 – 2518 www.ijeetc.com
Vol. 3, No. 4, October 2014

Research Paper

16 BIT ALU DESIGN USING REVERSIBLE LOGIC

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Reversible logic has emerged as one of the most important approaches for the power optimization with its application in low power VLSI design. It has wide applications in the field of, low power CMOS design, optical information processing and nanotechnology. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. This paper proposes a rewiew on design of a reversible ALU. The ALU consists of arithmetic and logical operations. The arithmetic operations include addition, subtraction and the logical operations include AND, OR, NOT and XOR. The degined ALU has better efficiency as it has less power loses and reduction in power loss upto 51% is obtained.

Keywords: Reversible ALU, Reversible gates, Reversible logic

INTRODUCTION

Conventional combinational logic circuits dissipate heat for every bit of information that is lost during their operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit, if it is constructed using the reversible logic gates will allow the recovery of the information. Energy loss is an important consideration in digital circuit design. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. In Landauer (1961) introduced that losing of bit in circuits causes the smallest amount of heat in computation and the theoretical limit of energy dissipation for losing of one bit computation is KTln2 (Landauer, 1961). Where K is a Boltzmann s constant equals to $1.3807 \times 10^{-23} JK^{-1}$ and T is the temperature at which the computation is performed (Landauer, 1961). At T = 300 K, this limit is 4×10^{-21} Joules. Although the amount of energy for single bit operation in single logic of a complex circuit is decreasing (10^{-15} J now a day) but overall heat generation by the circuit is increasing which cause the problems energy costs money and systems overheat.

Bennett (1973) showed that this heat dissipation due to information loss can be avoided if the circuit is designed using

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reversible logic gates. Reversible computing comes from the thermodynamics which taught us the benefits of the reversible process over irreversible process.

REVERSIBLE GATES

A reversible logic gate is an n-input, n-output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit. The logical reversibility means there should be same number of output lines as the number of input lines, i.e., the number of input lines and output line must be same or there should be one to one mapping between the input and output . The later one, i.e., physical reversibility means towards the retrieval of input by the input. The gate must be run forward and backward, i.e., the input can also be recovered or retrieved from the output.

A reversible logic circuit should have the following features:

- Use minimum number of reversible gates
- Use minimum number of garbage outputs
- Use minimum constant inputs

Reversible gate is realized by using 1*1 *NOT* gates and 2*2 Reversible gates, such as *V*, *V*+ (*V* is square root of *NOT* gate and *V*+ is its hermitian) and FG gate which is also known as CNOT gate. The *V* and *V*+ Quantum gates have the property given in the Equations (1, 2 and 3).

$$V * V = NOT \quad ...(1)$$

$$V * V+ = V+ * V = I \quad ...(2)$$

$$V+ * V+ = NOT \quad ...(3)$$

The Quantum Cost of a Reversible gate is calculated by counting the number of *V*, *V*+ and CNOTgates.Several reversible gates have come out in the recent years which are explained below;

Not Gate

The Reversible 1*1 gate is *NOT* Gate with zero Quantum Cost is as shown in the Figure 1.

Feynman / CNOT Gate

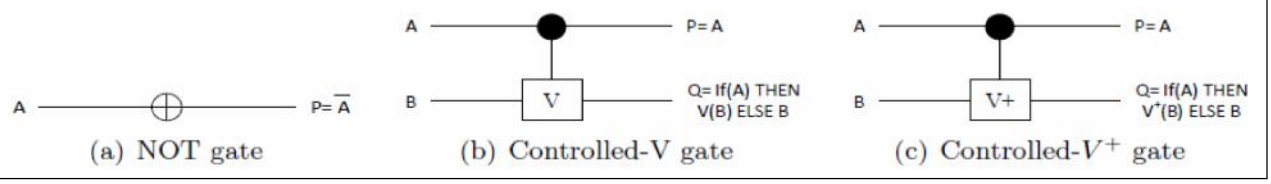
The Reversible 2*2 gate with Quantum Cost of one having mapping input (*A*, *B*) to output (*P* = *A*, *Q* = *A*•"*B*) as shown in the Figure 2 Here A is the controlling input and *B* is the controlled input; *P*, *Q* are the two outputs. Since the Feynman gate is a 2 x 2.

Taffoli Gate

The Toffoli Gate (TG) is a 3*3 reversible logic gate with three inputs and three outputs. The input to output mapping of a Toffoli gate can be represented as (A ,B ,C) to (P = A, Q = B, R = ((A B) ⊕ C), where A,B,C are the inputs and P, Q, R are the outputs of a Toffoli gate. Figure 3 shows the block diagram of a Toffoli gate.

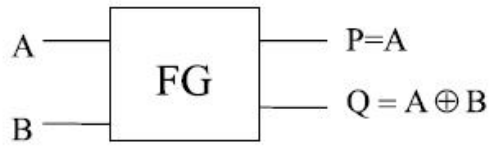
A Toffoli gate has a quantum cost of 5 as it can implemented using 2 V gates, 1 V + gate and 2 CNOT gates. Figure shows the quantum implementation of a Toffoli gate.

Figure 1: NOT Gate

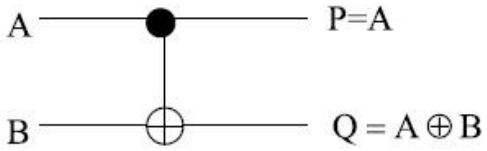


(a) NOT gate (b) Controlled-V gate (c) Controlled-V^+ gate

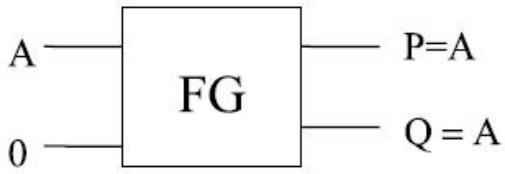
Figure 2: (a) CNOT Gate, (b) Quantum Representation of CNOT Gate, (c) Feynman Gate for Avoiding the Fanout, (d) Feynman Gate for Generating the Complement of Signal



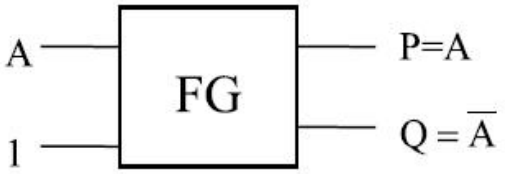
(a) CNOT Gate



(b) Quantum representation of the CNOT gate

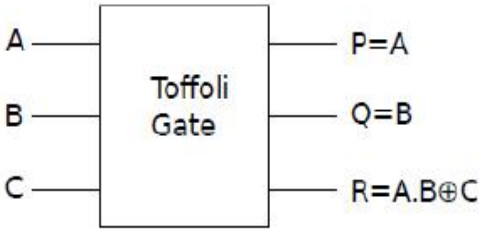


(c) Feynman gate for avoiding the fanout

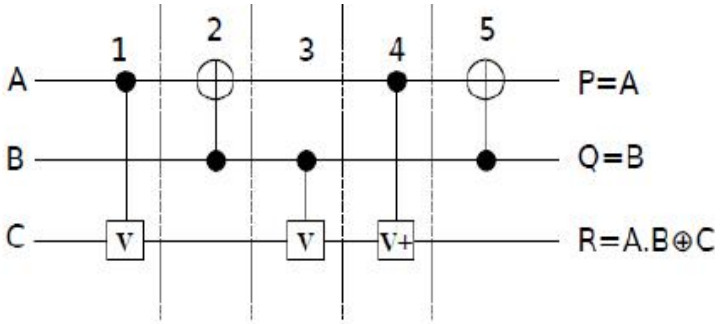


(d) Feynman gate for generating the complement of a signal

Figure 3: Toffoli Gate and its Quantum Implementation



(a) Toffoli Gate



(b) Quantum representation of the Toffoli Gate

Peres Gate

It is a 3*3 Peres gate . The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A ⊕ B and R = AB ⊕ C. Quantum cost of a Peres gate is 4. Figure 4 shows a 3*3 Peres gate.

Fredkin Gate

Fredkin gate is a 3*3 reversible logic gate with three inputs and three outputs.The Fredkin gate maps (A, B, C) to (P = A, Q = A^{-}B + AC, R = AB + A^{-}C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. A Fredkin gate can work as 2:1 MUX, as it is able to swap its other two inputs depending on the value of its first input. Quantum cost of 5 and it requires two dotted rectangles, is equivalent to a 2*2 Feynman gate with Quantum cost of each dotted rectangle is 1, 1 V and 2 CNOT gates as shown in Figure 5.

Double Peer Gate (DPG)

DPG gate is achieved by cascading two 3*3 Peres gate. The quantum realization cost

Figure 4: Peres Gate

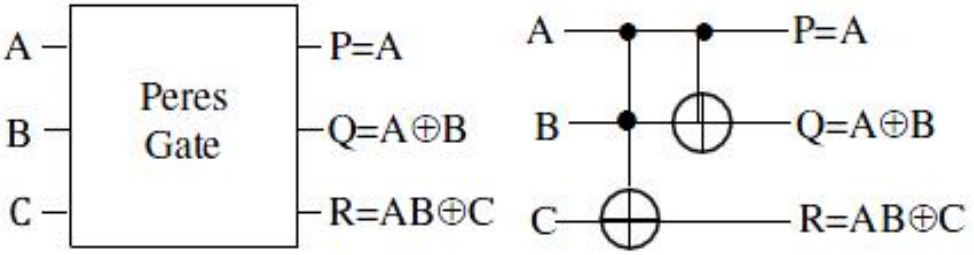


Figure 5: Fredkin Gate

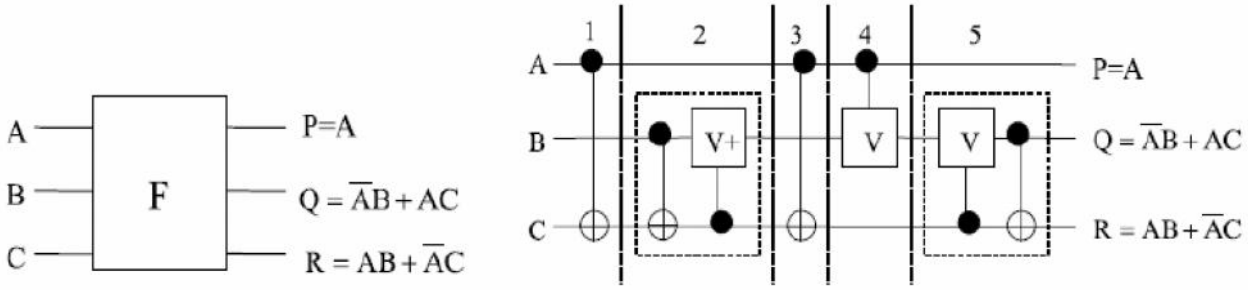
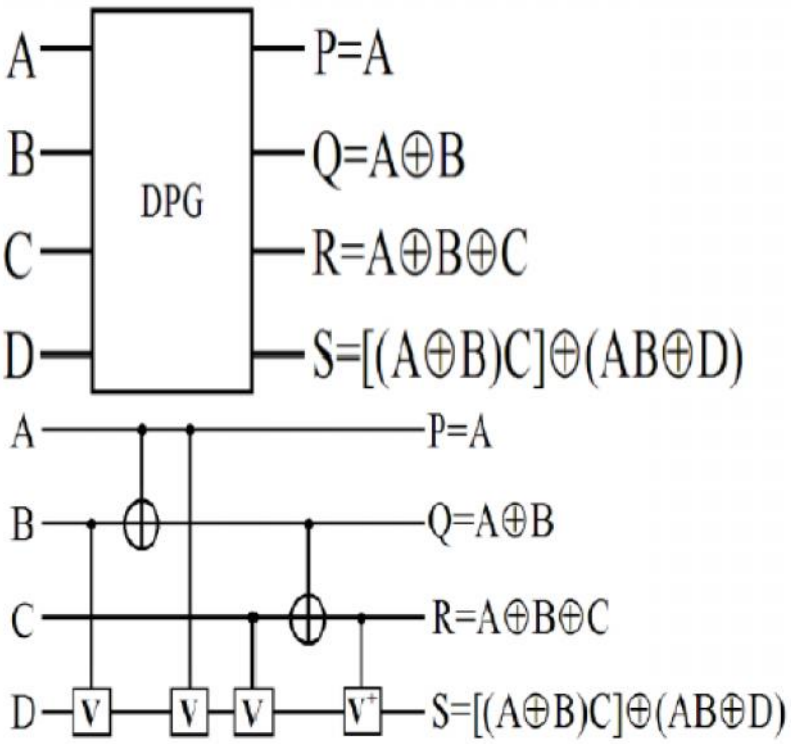


Figure 6: DPG Gate and its Quantum Implementation



of this gate is 6. Since it includes two 3*3 Peres gates. The gate can work singly as a reversible full adder circuit when its fourth input is set to zero (D = 0) as shown in Figure 6.

DESIGN OF ALU USING REVERSIBLE GATES

16-bit ALU is presented in this section.The Arithmatic and Logical Units are designed using Taffoli, fredkin, Feyman and DPG gates. The Proposed ALU performs eight arithmetic and four logical operations. Table 1 represents the table of functions to be performed by the reversible ALU. This ALU is constructed so that the cost of the circuit remains low and power losses can be reduced.

After performing these functions the simulation of the ALU is carried out. Then the power analysis for the reversible ALU and irreversible ALU is done and compared. The results are shown in Figure 7.

Table 1: Functional Table for Reversible ALU

S	S0	S1	Cin	Fun
0	0	0	0	A + B
0	0	0	1	A + B+1
0	0	1	0	A + $\overline{B}$
0	0	1	1	A – B
0	1	0	0	A
0	1	0	1	A+1
0	1	1	0	A-1
0	1	1	1	A
1	0	0	X	XOR
1	0	1	X	AND
1	1	0	X	OR
1	1	1	X	NOT

Power Comparison Table for ALU

The power consumed by irreversible and reversible ALU is presented in Table 2 given below:

Figure 7: Total Power for 16 Bit Irreversible ALU

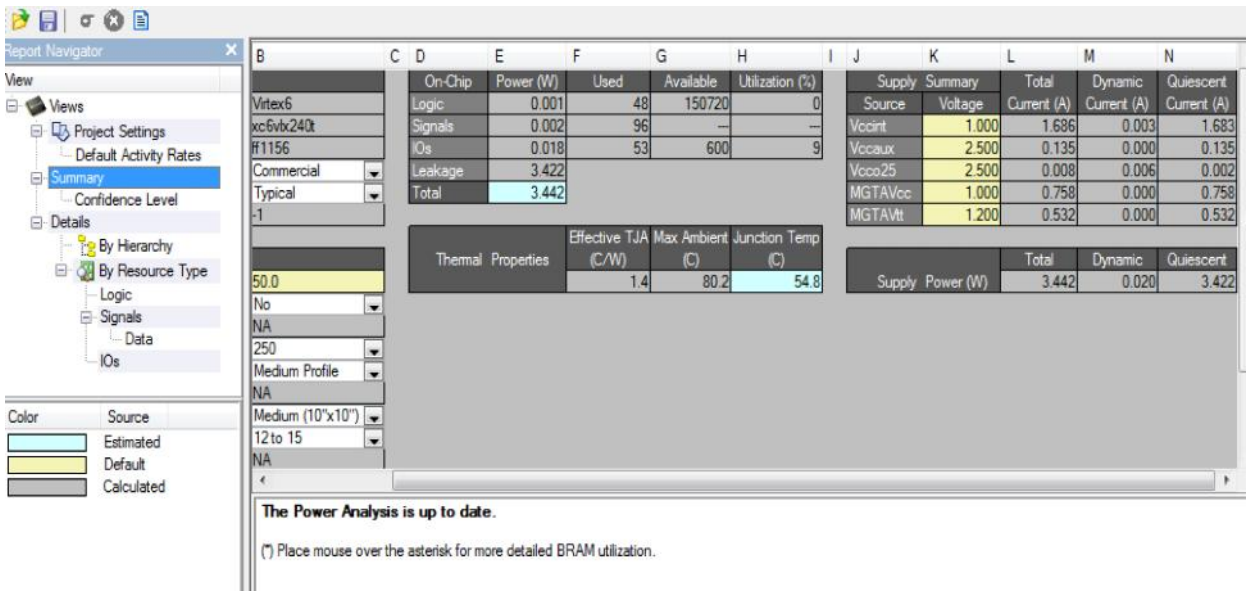


Figure 8: Logic Power for Irreversible ALU

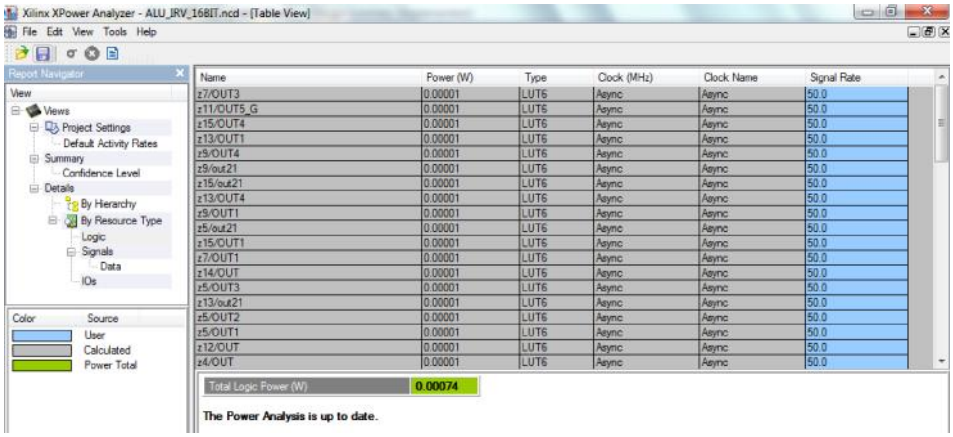


Figure 9: Total Power for 16 Bit Reversible ALU

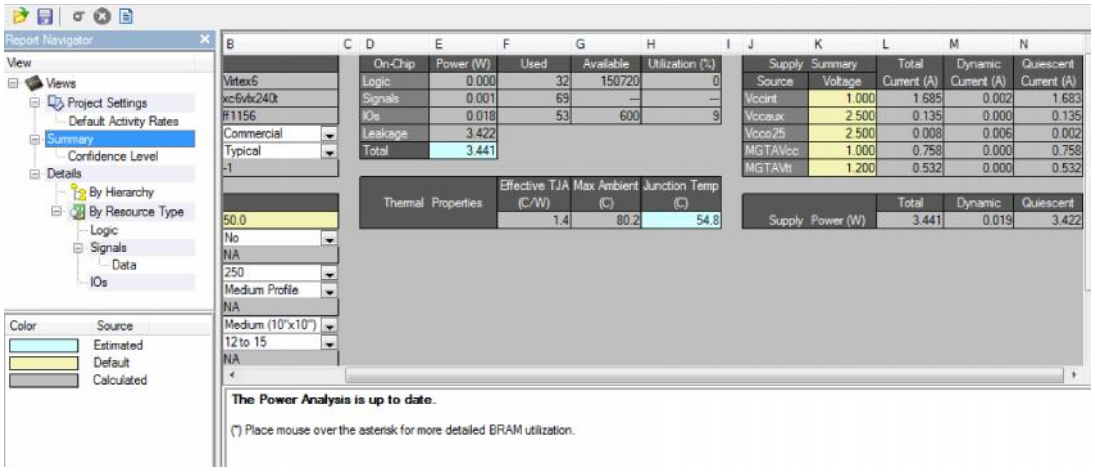


Figure 10: Logic Power for Reversible ALU

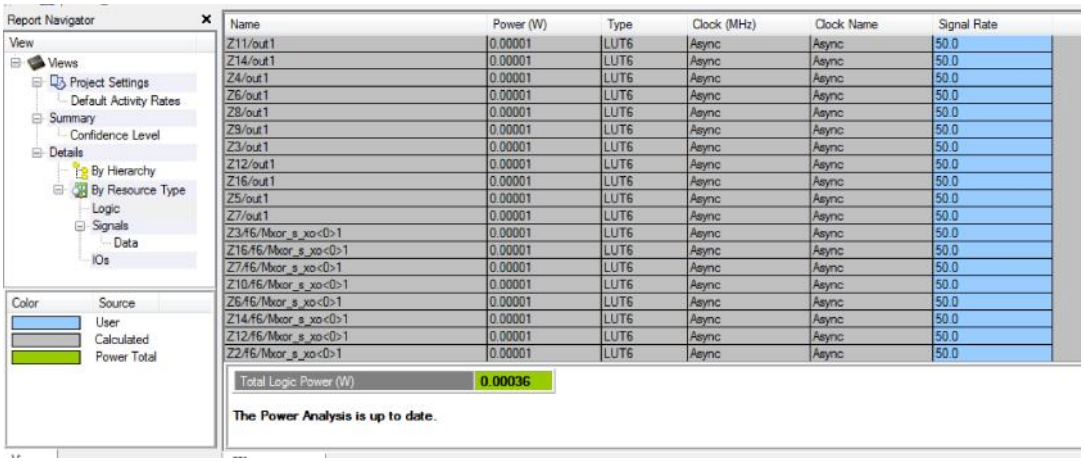


Table 2: Power Comparison Table for ALU

Type	16 Bit Irreversible ALU (mW)	16 Bit Reversible ALU (mW)
Logic Power	1.83	1.10
Total Power	20.21	19.0

CONCLUSION

This paper has introduced and proposed reversible circuits for realizing ALU. The proposed design leads to the reduction of power consumption compared with conventional logic circuits helps to increase the energy efficiency to a greater extent. The proposed reversible ALU design has shown that the logic power can be reduced by 51% than the irreversible ALU.

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