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Research Paper

A HIGH PERFORMANCE VIDEO TRANSFORM ENGINE BY USING SPACE-TIME SCHEDULING STRATEGY REVERSIBLE VEDIC GATES

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In this paper a new approach termed as space-time scheduling (STS) strategy is introduced where both area and performance evaluations are improved simultaneously. To reduce the area the proposed architecture is designed in such a way that the same architecture is used for both 1D and 2D applications using cascading approaches. In that it can calculate first-dimensional and second-dimensional transformations simultaneously in single 1-D discrete cosine transform (DCT) core to reach less hardware utilization. The DA-precision bit length is chosen as 9 bits instead of the traditional 12 bits to reduce the size of the chip without any degradation of the performance. Modules in the 1-D DCT core, including the modified two-input butterfly (MBF2), the pre-reorder, the process element even (PEE), the process element odd (PEO), and the post reorder share the hardware resources in order to reduce the area. The adders in the design are replaced by a low power and area efficient reversible Vedic adders to improve the overall performance of the system.

Keywords: Discrete cosines transform (DCT), Reversible logic and Vedic mathematics

INTRODUCTION

Transform coding constitutes an integral component of contemporary image/video processing applications. Transform coding relies on the premise that pixels in an image exhibit a certain level of correlation with their neighboring pixels. Similarly in a video transmission system, adjacent pixels in consecutive frames2 show very high correlation. Consequently, these Correlations can be exploited to predict the value of a pixel from its respective neighbors. A transformation is, therefore, defined to map this spatial (correlated) data into transformed (uncorrelated) coefficients. Clearly, the transformation should utilize the fact that the information content of an individual pixel is relatively small i.e., to a large extent visual contribution of a pixel can be predicted using its neighbors.

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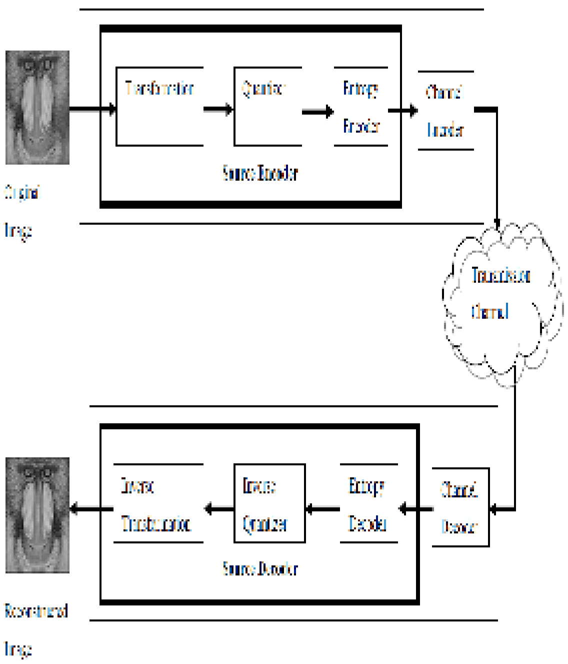
A typical image/video transmission system is outlined in Figure 1. The objective of the source encoder is to exploit the redundancies in image data to provide compression. In other words, the source encoder reduces the entropy, which in our case means decrease in the average number of bits required to represent the image. On the contrary, the channel encoder adds redundancy to the output of the source encoder in order to enhance the reliability of the transmission. Clearly, both these high-level blocks have contradictory objectives and their interplay is an active research area. However, discussion on joint source channel coding is out of the scope of this document and this document mainly focuses on the *transformation* block in the source encoder. Nevertheless, pertinent details about other blocks will be provided as required.

Figure 1: Components of a Typical Image/Video Transmission System



The Discrete Cosine Transform

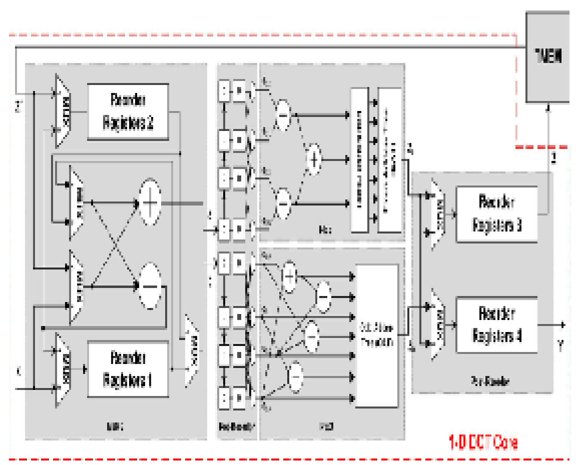
Like other transforms, the Discrete Cosine Transform (DCT) attempts to decorrelate the image data. After decorrelation each transform coefficient can be encoded independently without losing compression efficiency. This section describes the DCT and some of its important properties.

A discrete cosine transform (DCT) expresses a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio (e.g. MP3) and images (e.g. JPEG) (where small high-frequency components can be discarded), to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical for compression, since it turns out (as described below) that fewer cosine functions are needed to approximate a typical signal, whereas for differential equations the cosines express a particular choice of boundary conditions.

In particular, a DCT is a Fourier-related transform similar to the discrete Fourier transform (DFT), but using only real numbers. DCTs are equivalent to DFTs of roughly twice the length, operating on real data with even symmetry (since the Fourier transform of a real and even function is real and even), where in some variants the input and/or output data are shifted by half a sample. There are eight standard DCT variants, of which four are common. The most common variant of discrete cosine transform is the type-II DCT, which is often called simply "the DCT", its inverse, the type-III DCT, is correspondingly often called simply "the inverse DCT" or "the IDCT". Two related transforms are the discrete sine transform (DST), which is equivalent to a DFT of real and odd functions, and the modified discrete cosine transform (MDCT), which is based on a DCT of overlapping data.

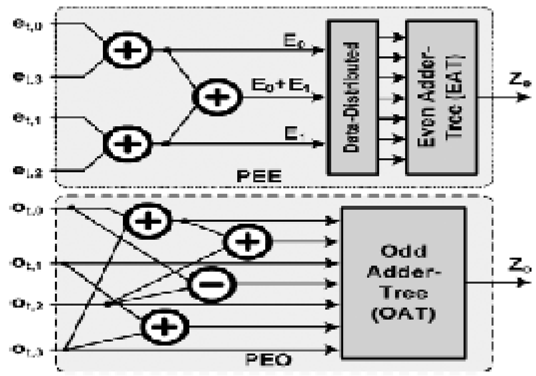
Formally, the discrete cosine transform is a linear, invertible function $f : \mathbb{R}^N \to \mathbb{R}^N$ (where $\mathbb{R}$ denotes the set of real numbers), or equivalently an invertible $N \times N$ square matrix. There are several variants of the DCT with slightly modified definitions. The N real numbers $x_0, ..., x_{N-1}$ are transformed into the N real numbers $X_0, ..., X_{N-1}$ according to one of the formulas:

Figure 2: Proposed 2-D DCT Architecture



The DCT, and in particular the DCT-II, is often used in signal and image processing, especially for lossy data compression, because it has a strong "energy compaction" property, most of the signal information tends to be concentrated in a few low-frequency components of the DCT, approaching the Karhunen-Loève transform (which is optimal in the decorrelation sense) for signals based on certain limits of Markov processes. As explained below, this stems from the boundary conditions implicit in the cosine functions.

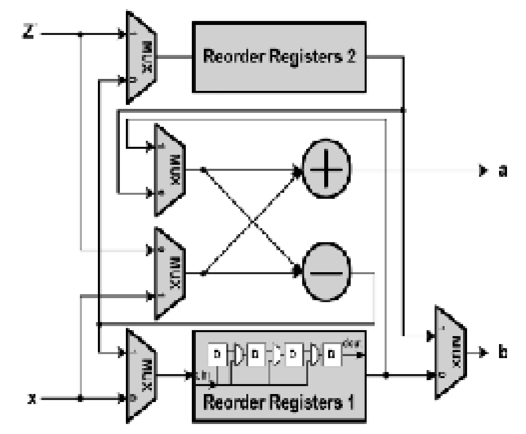
Figure 3: Architecture for Proposed PEE and PEO



A related transform, the modified discrete cosine transform, or MDCT (based on the DCT-IV), is used in AAC, Vorbis, WMA, and MP3 audio compression. DCTs are also widely employed in solving partial differential equations by spectral methods, where the different variants of the DCT correspond to slightly different even/odd boundary conditions at the two ends of the array. DCTs are also closely related to Chebyshev polynomials, and fast DCT algorithms (below) are used inChebyshev approximation of arbitrary functions by series of Chebyshev polynomials, for example inClenshaw–Curtis quadrature.

Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations . This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts

Figure 4: MBF2 Architecuture



put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved.

With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them.

Vedic mathematics can be aptly employed here to perform multiplication.Another important area which any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a tradeoff between the power dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. Thus during the design of any reversible circuit the delay is the only criteria that has to be taken care of. In a reversible Urdhva Tiryakbhayam Multiplier had been proposed.

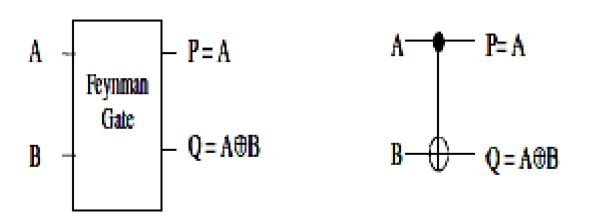
REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs.

Feynman Gate

Figure 1 shows a 2*2 Feynman gate. Quantum cost of a Feynman gate is 1. Feynman gate is called as Controlled NOT gate or CNOT gate. It is equivalent to single control input tofili gate.

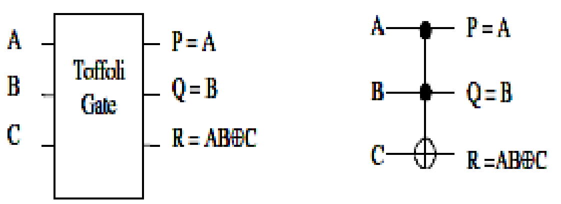
Figure 1: Feyman Gate and Its Symbolic Representation



Toffoli Gate

Figure 2 shows a 3*3 Toffoli gate The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=A(B xor C). Quantum cost of a Toffoli gate is 5. It has two control inputs.

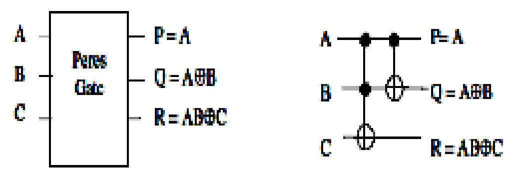
Figure 2: Toffoli Gate and Its Symbolic Representation



Peres Gate

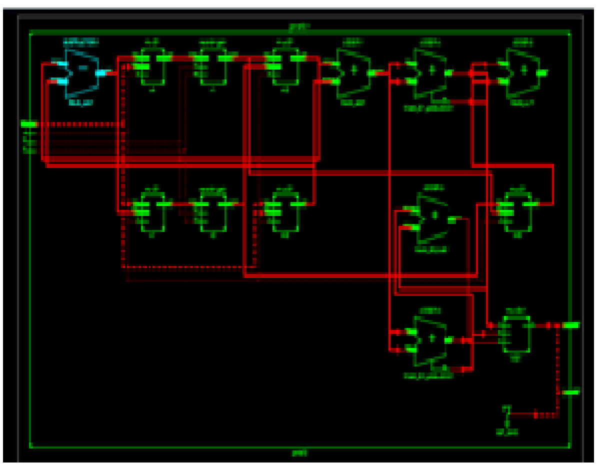
Figure 3 shows a 3 * 3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A. Q = A ⊕ B and R = AB ⊕ C. Quantum cost of a Peres gate is 4. It is needs two Toffoli gates for its construction.

Figure 3: 3*3 Peres Gate

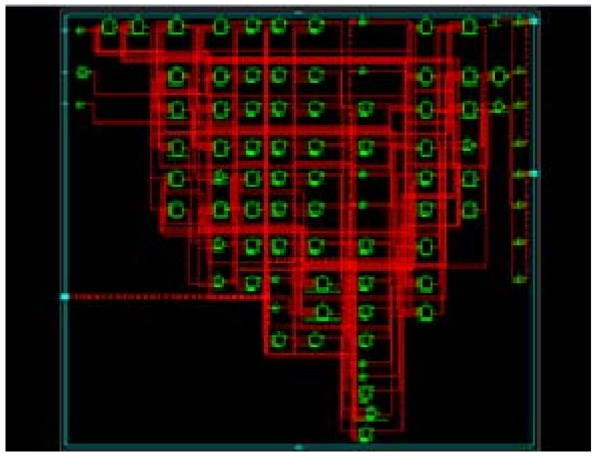


RESULTS

RTL Schematic



Technology schematics



Waveform

CONCLUSION

In this paper the 2-D DCT Architecture is implemented by using Reversible Vedic adder approach. To reduce the area the proposed architecture is designed in such a way that the same architecture is used for both 1D and 2D applications using cascading approaches. In that it can calculate first-dimensional and second-dimensional transformations simultaneously in single 1-D discrete cosine transform (DCT) core to reach less hardware utilization. The functionality and synthesis is carried out using XILINX ISE 12.3i. VERILOG HDL is used to describe the functionality. From the Synthesis results it is concluded that the total memory usage is 133636 kilobytes with the total Delay of 11.512ns along with low power consumption of 0.24458mw due to replacement of adders with reversible Vedic adder approach.

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