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Research Paper

DESIGN OF SIGNATURE REGISTERS USING SCAN FLIP-FLOPS FOR ON-CHIP DELAY MEASUREMENT

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This paper presents a delay measurement techniques using signature analysis, and a scan design for the proposed delay measurement technique to detect small-delay defects. The proposed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors. The evaluation with Rohm 0.18 m process shows that the measurement time is 67.8% reduced compared with that of the delay measurement with standard scan design on average. The area overhead is 23.4% larger than that of the delay measurement architecture using standard scan design, and the difference of the area overhead between enhanced scan design and the proposed method is 7.4% on average. The data volume is 2.2 times of that of test set for normal testing on average.

Keywords: Delay estimation, Design For Testability (DFT), Integrated circuit measurements, Semiconductor device reliability, Signature register

INTRODUCTION

With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems (Ahmed and Tehranipoor, 2007). If small-delay defects cannot be detected in LSI screening, the chips will behave abnormally under particular operations in certain applications, and their lifetime may become very short due to the vulnerability to the transistor aging. Therefore to keep the reliability after shipping, enhancing the quality of the testing for the small-delay defect detection is an urgent need. The delay measurement of paths inside the circuits is useful for detection and debugging of small-delay defects (Noguchi *et al.*, 2008). However, it is impossible to measure the small circuit path delays using an external tester, even if the resolution is high. Therefore development

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of the embedded delay measurement technique is required.

Some embedded delay measurement techniques have been proposed. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement techniques (Dervisoglu and Stong, 1991). In this technique, the delay of a path is measured by continuous sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the fiip fiop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation.

However, it has a drawback. The measurement time of the technique depends on the time for the scan operation. These days, the gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical. Noguchi *et al.* proposed the self testing scan-FF. The fiip fiop reduces the required number of scan operations, which makes the measurement time practical (Noguchi *et al.*, 2008). They also proposed the area reduction technique of the self testing scan-FF (Noguchi *et al.*, 2009). However, the area overhead of these methods is still expensive compared with the conventional scan designs.

This paper presents a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for design for test (DFT). The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging.

PRELIMINARIES

Related Works

These days, various methods for small-delay defect detection have been proposed. The path delay fault testing with a normal clock width is the most popular and is widely used (Krstic and Chen, 1998). In this method, we choose the longer paths to detect the smaller cumulative delay due to the small delay distributed on the paths. The larger the cumulative delays, the higher the probability of the detection of the distributed small delay. However, the coverage of the small delay defect detection largely depends on the normal clock width, which is a problem of this method.

On the other hand, to solve the problem, methods with delay fault testing using a variable clock generator have been proposed. The delay fault testing with a smaller test clock reduces the slack of the paths. Therefore the smaller delay defects which cannot be captured with the normal clock width can be

captured with the appropriate smaller test clock width.

These days, small-delay defect detection methods using on-chip delay measurement techniques have been proposed. The direct measurement of the real delay of each path of each chip screens outlier chips robustly even in the presence of process variation or the gap between real and simulation environment. It realizes higher fault coverage of small-delay defects than the simulation-based ones.

In addition, it can be used not only for the detection of small-delay defects, but also for the debugging (Sharma and Patel, 2000; and Flanigan *et al.*, 2006). Because modern chips are too huge and complex, LSI CAD tools cannot optimize the design enough. Hence, the manufactured first silicon chip usually does not meet the specification in spite of the tighter Release To Production (RTP) schedule. Therefore silicon debugging and Design For Debugging (DFD) become much more important in modern chips (Balachandran *et al.*, 2002). Various silicon debugging technologies and DFD methods have been proposed (Yang and Touba, 2008 and 2009; and Wang and Tehranipoor, 2009a and 2009b).

On-chip delay measurement provides accurate information of the delay of inside paths for the debugging of small-delay defects (Chen and Liou, 2008). Most of the conventional works of on-chip delay measurement are classified to either a proposal of an embedded delay measurement circuit or that of a scan architecture for scan-based on-chip delay measurement with a variable clock generator.

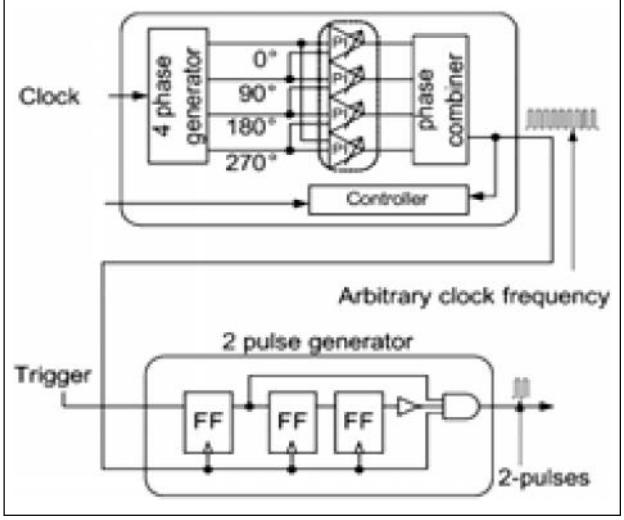
Some works proposed embedded delay measurement circuits of modified Vernier Delay Line (VDL). Datta *et al.* proposed the embedded delay measurement circuit with high resolution . It is the first work of an embedded measurement circuit of modified VDL to the best of our knowledge. Tsai *et al.* proposed the area efficient and noise-insensitive modified VDL with coarse and fine parts namely BIDM . Pei *et al.* also proposed the area efficient modified VDL. The feature of this method is delay range of each stage of VDL. The delay ranges increase by a factor of two gradually, which reduces the required stages. Therefore the area is smaller than Datta's work. The modified VDLs achieve high resolution. However they require redundant lines to feed the input and output signals of the measured paths, which needs the compensation of the delay effect of the redundant lines. Tanabe *et al.* solved the problem by removing the delay of the redundant lines from the measured delay using some additional embedded circuits. The proposed technique is categorized to the scan-based one.

Variable Clock Generator

In the proposed method, the clock width should be reduced continuously by a constant interval as explained later. It is difficult for an external tester to control this clock operation. Therefore an on-chip variable clock generator is indispensable for the proposed method. In this paper, we use the on-chip variable clock generator proposed by Noguchi *et al.* (2008).

Figure 1 illustrates the circuit. The circuit consists of the phase-interpolator-based clock generator and the 2-pulse generator. The phase-interpolator-based clock generator

Figure 1: 2-Pulse Generator (Variable)



generates an arbitrary clock width. The 2-pulse generator generates 2-pulse test clocks with arbitrary timing in response to a trigger signal. Some of the specification and the evaluation results are shown in Table 1 (Wang and Tehranipoor, 2009a).

Table 1: Specification and Measurement Result

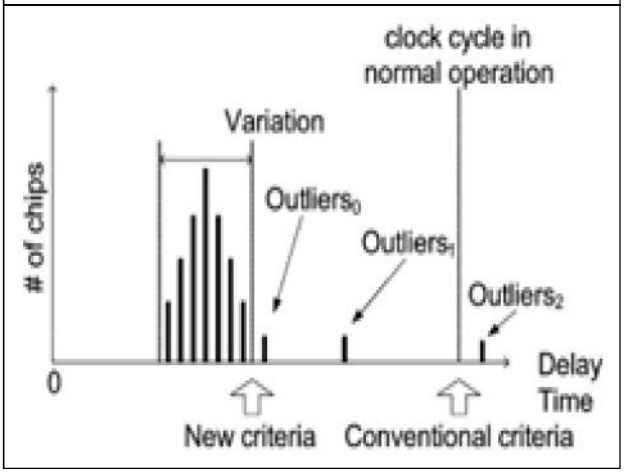
Process	90 nm CMOS
Occupied Area	300 (μm) x 128 (μm)
Input Clock	1.5 GHz 4 Phase
Output Clock	1 GHz to 2 GHz 4 Phase
Functions	Frequency Control
	Jitter Generation
	Duty Ratio Control
	Phase Control
Timing (Phase) Step Resolution	5.2 ps (2.8°)
Step Error	±1.3 ps ~ ±2.4 ps
(5 Chip Measured)	(±0.7° ~ ±1.3°)
Cumulative	Best Chip Worst Chip
Timing Error	±5.4 ps ~ ±11.2 ps
(5 Chip Measured)	(±2.9° ~ ±6.3°)

Source: Wang and Tehranipoor (2009a)

Small-Delay Defect Detection with Delay Measurement of Chips

The proposed method uses the Noguchi's small-delay defect detection technique (Noguchi *et al.*, 2008). In this technique, the test clock width for delay fault testing of each path is determined with the normal path-delay distribution of each path.

Figure 2: Decision of Test Clock Width Based on Path Delay Distribution Obtained by Chip Measurement



This strategy has already been applied to various small-delay detection techniques(Chen and Liou, 2008).

But its originality is to obtain the path-delay distribution with the delay measurement of the paths of the fabricated chips. Figure 2 shows the path delay distribution of a path obtained by the delay measurement of the fabricated sample chips. The horizontal axis is measured delay. The vertical axis is the number of chips. The chips which have delay inside the range Variation are normal chips. The chips which have delay outside the range Variation, namely Outliers0, Outliers1, Outliers2, are abnormal chips. The delay is the outside of the clock cycle in normal operation. Therefore it will be detected by

conventional delay fault testing with the clock cycle in normal clock operation which is Conventional criteria. The delay Outliers0 and Outliers1 are within the clock cycle in normal operation. The conventional delay fault testing regards them as good chips. However because the delay is outside Variation, it will cause improper operations under particular operation in certain applications and may cause improper operations after shipping due to the effect of aging (Noguchi *et al.*, 2008). In Noguchi's technique, the test clock cycle is set to the upper limit of the distribution of normal chips, which is New criteria. Then all the outlier chips are detected by the delay fault testing.

The aim of the technique is to screen the chips which have abnormal delay in gates or wires. Therefore the test set for the measurement should detect all the transition faults which are sensitized through single-path sensitizable paths. The proposed method is a new delay measurement technique for the small-delay defect detection technique.

Basics

This section explains the concept of the proposed delay measurement. The target paths of the proposed method are single path sensitizable (Krstic and Chen, 1998).

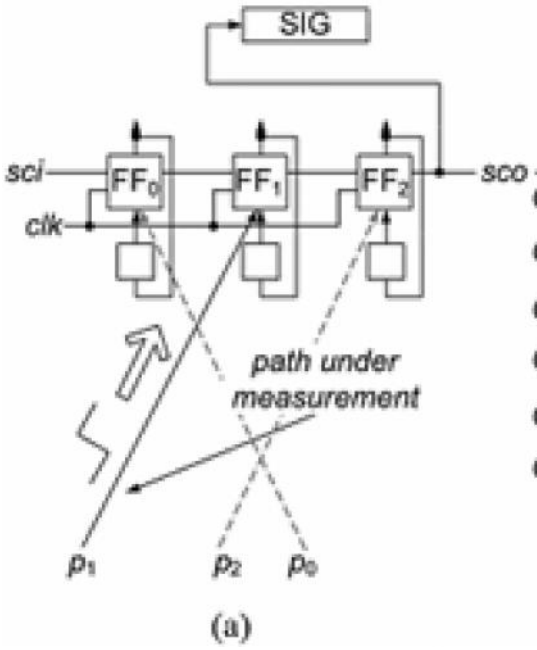
Basically, the proposed method is scan-based delay measurement. The difference from the basic one is the usage of the signature registers and the additional latches for the acceleration of the delay measurement.

Figure 3a shows the basics of the proposed method. This example has three fiip fiops FF_0, FF_1, and FF_2. Each fiip fiop has the input line (bottom), the output line (upper), and the clock line clk. Each fiip fiop FF_i is connected to an extra latch. At first, we assume that each fiip fiop has its own extra latch. The value of each fiip fiop is stored in the correspondent latch, and the value of each latch can be loaded to the correspondent fiip fiops in arbitrary timing. In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be loaded from these latches in a clock without scan-in operation.It reduces the time for multiple sensitization of a path drastically. The horizontal line through these fiip fiops represents the scan path. The symbols sci and sco represent the scan input and output, respectively.

The rectangle SIG represents the signature register using the linear feedback shift register as its basic component. The input of SIG is connected to the output of the last fiip fiop FF_2. More detail structures of the fiip fops and the signature register are shown in Figures 4 and 5, respectively.

Here, we measure the delay of p_1. In this example, we assume that the clock width of normal operation is 10 ns, and the resolution of the delay measurement is 2 ns. First, SIG is initialized with reset operation. Second, the target path p_1 is tested continuously 5 times with the test clock reduced gradually by the resolution. The multiple clock width testing is realized by the variable clock generator was also explained in previous section. The test clock of the 1st testing (#1) is 10 ns. After the test, the test response is sent to SIG through the scan path with two clock shift out operation.

Figure 3: Concept of Proposed Delay Measurement (a) Basics of Proposed Measurement (b) Signature Table



	Test Clock #1	#2	#3	#4	#5	Delay (ns)	Sig. val. sig$_r$ sig$_f$
Case$_0$	F	F	F	F	F	10-	000 010
Case$_1$	P	F	F	F	F	8-10	011 001
Case$_2$	P	P	F	F	F	6-8	101 111
Case$_3$	P	P	P	F	F	4-6	100 110
Case$_4$	P	P	P	P	F	2-4	110 100
Case$_5$	P	P	P	P	P	0-2	010 000

P : Pass, F : Fail
Sig. val. : Expected signature value

(b)

Figure 4: Scan Flip Flops for Proposed Measurement

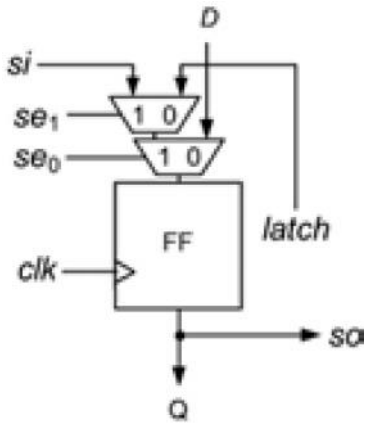
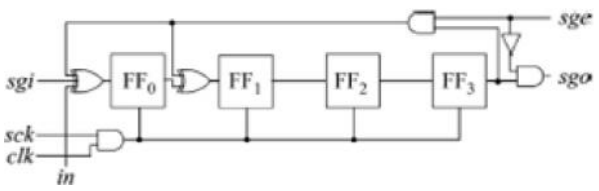


Figure 5: Four Bit Reconfigurable Signature Register



The test clock of the second testing (#2) is 8 ns. Similarly, the test clock width of the third, fourth, and fifth testings (#3, #4, #5) are the difference between 2 ns and the previous test clock width. Each test response is sent to SIG with two clocks. After the above 5 times of delay fault testings, the signature value of SIG is retrieved. To estimate the delay, the retrieved signature value is compared with the expected signature values of the signature table. Figure 3b shows the signature table in this example. The table has four columns. The first column is the cases of the measurement. The second column is the sequences of the test responses of #1-#5. The third column is the path delay value. The fourth column is the signature values of each case. Here, sigr and sigf are the signature values for rising and falling transition testings, respectively. The delay of each path is decided as more than 10, 8-10, 6-8, 4-6, 2-

4, or 0-2 ns, with 2 ns resolution. The sequences of the test responses of the 5 times measurement are shown in Figure 3b. The symbols $Case_0$, $Case_1$, $Case_2$, $Case_3$, $Case_4$, $Case_5$ indicate the cases with path delays, more than 10, 8-10, 6-8, 4-6, 2-4, 0-2 ns, respectively. The symbols *P* and *F* represent the pass and fail of a testing, respectively. In case of rising transition testing, $P = 1$ and $F = 0$, and in case of falling transition testing, $P = 0$ and $F = 1$. The retrieved signature value is compared with the expected signature values on the table, and decides the delay value.

When the number of fiip fiops is *n*, clock width is *T*, the measurement resolution is ΔT, and the continuous testing time is N_{meas}, the delay measurement sequence of a target path is as follows. Here, we assume that the test vector is already stored in the latches. The end point of the measured path is $FF_k (0 \le k \le n-1)$.

Step 1: Initializing SIG.

Step 2: Test vector is loaded from the latches.

Step 3: Test clock width *T* is set to normal clock width.

Step 4: Test clock is applied.

Step 5: The test response is sent to SIG which is connected to the output of FF_{n-1} with $n-k$ clocks.

Step 6: If testing time is equal to N_{meas}, go to Step 7 after the signature value of SIG is retrieved, otherwise go back to Step 2 after the test clock width *T* is updated to $T-\Delta T$.

Step 7: The delay value is estimated by comparing the retrieved signature value and the signature table.

Implementation

In this subsection, we explain the implementation of the proposed measurement system. First we explain the important components to understand the whole system. After that, the whole system is presented.

Scan Flip Flop for Measurement: Figure 4 is the gate level description of the scan fiip fiop for the proposed measurement. The lines *D*, *Q*, and clk are the input, output, and clock lines, respectively. The line is connected to an extra latch which provides the test bit to the fiip fiop. The lines *si* and *so* are the input and output for constructing the scan path. The input *si* is connected to *so* of an adjacent scan fiip fiop or the scan input.The output *so* is connected to *si* of an adjacent scan fiip fiop or the scan output. The fiip fiop has two multiplexers. The lines *si* and latch are the inputs of the upper multiplexer controlled by se_1. The output of the upper multiplexer and *D* are the inputs of the bottom multiplexer controlled by se_0. When $se_0 = 0$, the fiip fiop is in normal operation mode. When $se_0 = 1$ and $se_1 = 1$, the fiip fiop is in scan operation mode. When $se_0 = 1$, $se_1 = 0$, the fiip fiop loads the value stored in the latch connected to the latch line.

Reconfigurable Signature Register: The signature register for the proposed measurement requires the following functions to meet the demand of the proposed measurement.

- Capturing the test response in arbitrary timing.
- Shifting out the signature data in arbitrary timing.

Figure 5 shows the architecture of the signature register for the proposed measurement. The length of the signature register in this example is four bit. Therefore it has four fiip fiops FF_0, FF_1, FF_2, FF_3.

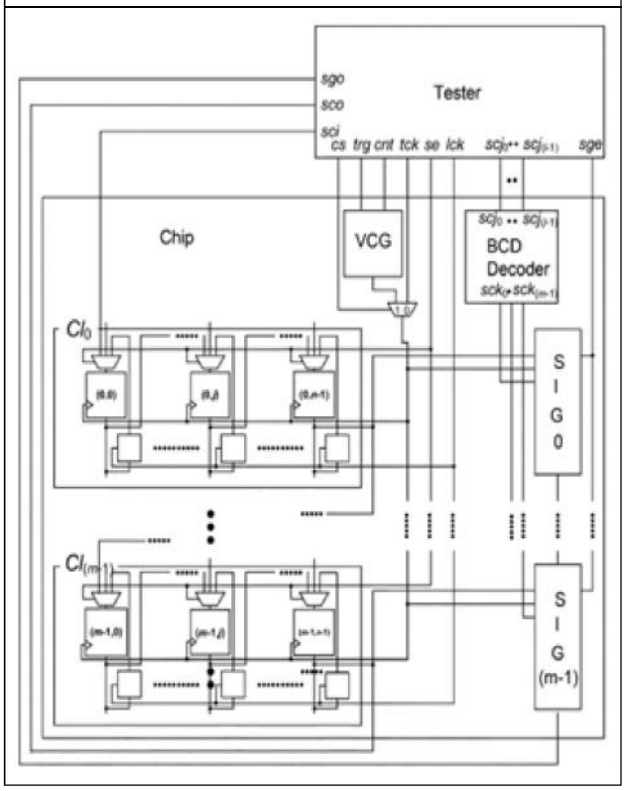
The signature register can be configured to a shift register. The line *sge* controls the configuration. When *sge* = 1, it works as a signature register. When *sge* = 0, it works as a shift register.

The line in is the input of the signature register. During measurement, test responses are sent to in. The line clk is clock line. The clock line is controlled by *sck*. When *sck* = 0, the signature register does not capture the input value. When *sck* = 1, the signature register captures the input value synchronizing with the positive edge of *clk*. By controlling *sck*, the signature registers capture only the target test response.

When *sge* = 0, this circuit is configure to the shift register. The input is *sgi*. The output is *sgo*. As explained later, the measurement system requires multiple signature registers generally. The input and output are connected to the output and the input of adjacent signature registers to construct a long shift register for sending all the signature values to the external tester.

Whole System: Figure 6 shows the proposed measurement system. The proposed system consists of the low cost tester and the chip with the Variable Clock Generator (VCG) was explained in previous section and a BCD decoder. The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the fiip fiops and the signature registers independently. The reset operations are controlled by the tester.

Figure 6: Proposed Measurement System



The low cost tester controls the whole measurement sequence. The clock frequency *tck* is slower than the functional clock. The line *sgo* retrieves the signature data from the signature registers to estimate the measured delay. The line *sci* sends the test vectors to the scan input of the chip. The line *sco* gets the data of the fiip fiops from the scan output of the chip. In the proposed measurement sequence, *sco* is not used. However, it is used to check the fiip fiops or the additional latches before the measurement. The line *cs* is the clock control line. The proposed measurement uses both the slow tester clock *tck* and the fast double pulse generated by on-chip VCG. The line *cs* selects the slow and fast clock. If *cs* is 1, the fast clock is sent to

the clock line of the components. Otherwise the slow tester clock *tck* is sent. The lines trg and cnt are the input lines for VCG. The fast double pulse is launched synchronizing with the positive edge of *trg*. The line *cnt* controls the width of the double pulse. The line *se* controls the scan fiip fiops. The line *lck* controls the latches for storing test vectors. The lines scj_0, ..., scj_{l-1} are the inputs for the encoded data to control the capture operation of the signature registers. The BCD decoder decodes the encoded input data to the control data of the signature registers sck_0, ..., sck_{m-1}. As explained later, the decoder is used to reduce the input lines for the control data of the signature registers. The *sge* is the enable signal for the signature registers. The fiip fiops in the chip are classified to the clusters $C1_0$, ..., $C1_{(m-1)}$. Here, we assume that each cluster has *n* fiip fiops, and thus the number of the fiip fiops is *mn*. In general, the number of the fiip fiops of the last cluster is $N_{FF}mod_n$, where N_{FF} is the number of fiip fiops, or *n*. The coordinate (*i*, *j*) written in the fiip fiops indicates the location. The number *i* is the cluster *id*. The number *j* is the order in the cluster. The output of the fiip fiop of (*i*, *n*-1) which is the tail fiip fiop of each cluster Cl_i is connected to the fiip fiop of (*i*+1, 0) which is the head fiip fiop of Cl_i+1.

These lines construct the scan chain. The output of the tail fiip fiop of each cluster is connected to the input of the corresponding signature register. The paths whose test response is captured by the fiip fiops included in Cl_i is measured by SIG_i. The control lines of the signature registers are connected to the BCD decoder.

Measurement Sequence

Here, we explain the measurement sequence. First, the measurement sequence of the paths simultaneously sensitized in a test vector is explained in previous section.

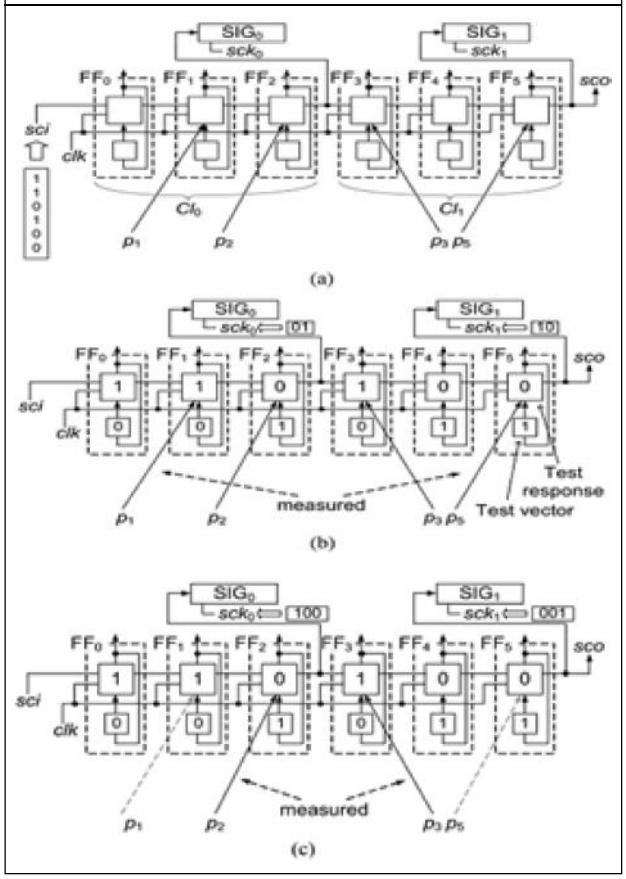
Measurement Sequence Per a Test Vector

We explain the measurement strategy using the example depicted in Figure 7. In this example, the proposed method is applied to the circuit with six fiip fiops FF_0-FF_5. These fiip fiops are classified to the two clusters Cl_0 and Cl_1. The cluster Cl_0 includes (FF_0, FF_1, FF_2), and Cl_1 includes (FF_3, FF_4, FF_5). The cluster Cl_0 has the signature register SIG_0. The cluster Cl_1 has the signature register SIG_1. The clock line *clk* controls these fiip fiops. The control lines sck_0 controls the capture operation of SIG_0, and sck_1 controls the capture operation of SIG_1. The paths p_1, p_2, p_3, p_5 are sensitized simultaneously by the test vector (FF_0, FF_1, FF_2, FF_3, FF_4, FF_5) = (0, 0, 1, 0, 1, 1). The test response of p_i is captured by FF_i. The expected test response is (FF_0, FF_1, FF_2, FF3, FF_4, FF_5) = (1, 1, 0, 1, 0, 0).

The paths p_1 and p_2 are measured by SIG_0. The paths p_3 and p_5 are measured by SIG_1. The combination of the two paths, one of which is selected from p_1 and p_2, the other of which is selected from p_3 and p_5, can be measured simultaneously.

First, the test vector is set to the fiip fiops with scan-in operation. After that, the values of the fiip fiops are set to the extra latches (a). Second, the first stage measurement is performed (b). Third, the second stage measurement is performed (c). In each stage,

Figure 7: Measurement of Paths Sensitized in a Test Vector in Parallel, (a) Scan-in Test Vector and Store it to Latches, (b) STG0-After Each Testing, Send Test Responses of p_1 and p_5 to SIG_0 and SIG_1, Respectively, (c) STG1-After Each Testing, Send Test Responses of p_2 and p_3 to SIG_0 and SIG_1, Respectively



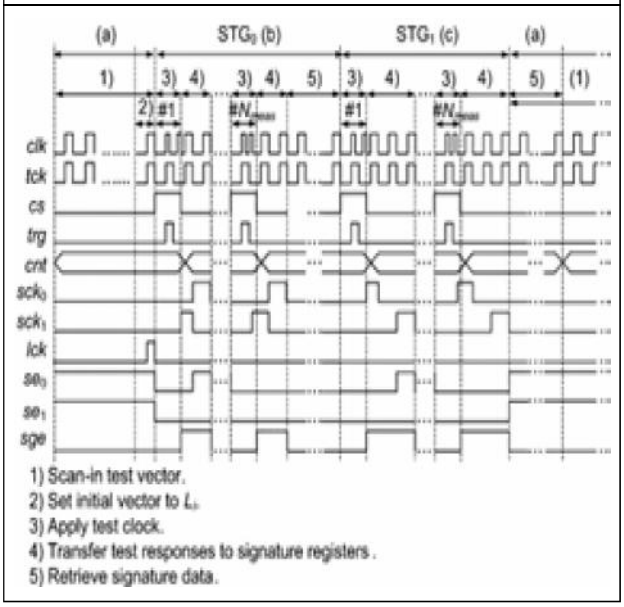
the paths under measurement are tested multiple times with reducing the test clock width. Steps (b) and (c) show the state just after the test execution. The fiip fiops hold the test response. The latches hold the test vector. After the testing, the test responses are shifted to the signature registers SIG_0 and SIG_1 with the clock operation of *clk*. The required number of shift clocks of a stage is the maximum number of the shift clocks among the paths measured simultaneously in the stage. For example, in STG_0, two clocks are required to send the test response of p_1 to SIG_0, while one clock is required to send the test response of p_5 to SIG_1. Therefore the shift clocks of STG_0 are two clocks. Similarly the shift clocks of STG_1 are three clocks. To capture only the target test response value, the control bit sequences are sent to sck_0 and sck_1. In SIG_0, the test response of p_1 is captured to FF_1. Therefore SIG_0 should capture the value two clocks later. This operation is realized by sending the bit sequence "01" to sck_0 synchronizing to the *clk*. To capture the test result of p_5, SIG_1 should capture the value one clock later. This operation is realized by sending the bit sequence "10" to synchronizing to the *clk* in STG_0. In STG_1, the test response of p_2 is captured by sending the bit sequence "100" to sck_0, and the test response of p_3 is captured by sending the bit sequence "001" to sck_1, respectively.

Figure 8 shows the timing chart of this operation. The clock selection is controlled by *cs*. The trigger signal and the control signal is provided to VCG. In STG_0, SIG_0 captures the test response in the second shift-out clock. Therefore sck_0 turns to 1 synchronizing with the negative edge of the first clock of the shift-out operation. The latch clock *lck* captures the values of the fiip fiops just after the scan-in operation is finished.

Tester Channel Reduction

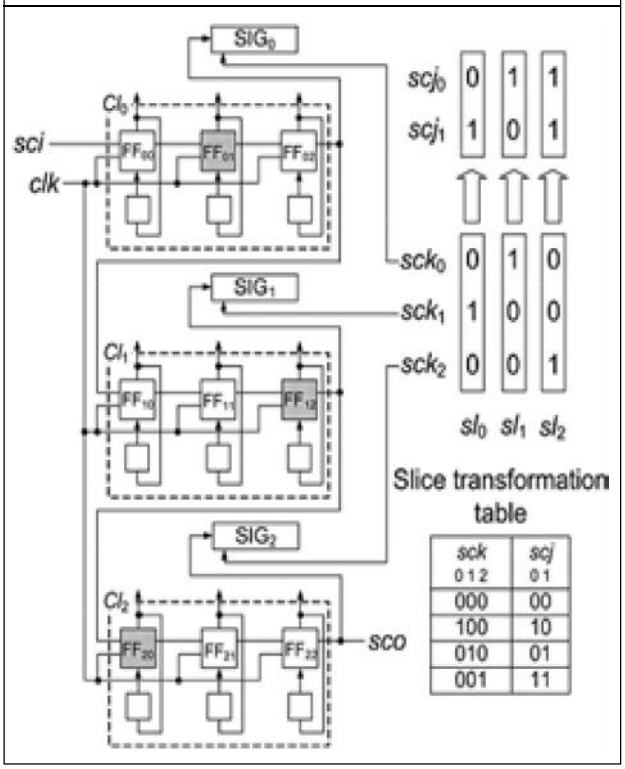
If sck of each signature register is directly fed to the inputs of the chip, it requires the same number of the extra inputs as the number of the signature registers. It increases tester channel width. To keep the tester channel width short, we use the BCD decoder as depicted in Figure 6. The decoder circuit

Figure 8: Timing Chart of the Sequence of Figure 7



transforms n bit binary code to the corresponding 2^n width decimal code. For example, when n = 2, $scj_0\, scj_1$ = 01, the corresponding decimal code is $sck_0 sck_1 sck_2 sck_3$ = 0100. We explain how to encode the *sck* bit sequences to the corresponding binary code scj with the example depicted in Figure 9. This example consists of three clusters CI_0, CI_1 and CI_2. Each cluster has three fiip fiops. Consider the case that the test response of the sensitized paths are captured in FF_{01}, FF_{12}, FF_{20}. In the shift out operation after a testing, the test response of FF_{01} is captured by SIG_0 two clocks later. Therefore the bit sequence "010" should be sent to sck_0. The test response of FF_{12} is captured by SIG_1 one clock later. Therefore the bit sequence "100" should be sent to sck_1. The test response of FF_{20} is captured by SIG_2 three clock later. Therefore the bit sequence "001" should be sent to sck_2. Each bit value of these bit sequences is grouped. The group of the 0th bit values is

Figure 9: Encoding the Output Data of BCD Decoder sck to the Input Data of BCD Decoder scj



$sck_0 sck_1 sck_2$ = 010. Those of the first bit values and second bit values are $sck_0 sck_1 sck_2$ = 100, $sck_0 sck_1 sck_2$ = 001 respectively. We call each group slice. Here, sl_i represents the slice of i^{th} bit. Finally, these decimal codes are transformed into the corresponding binary code. The 0th slice sl_0"010" is transformed to "01". The 1st slice sl_1"100" is transformed to "10". The second slice sl_2"001" is transformed to "11". As a result, the bit width of the data is reduced from 3 bit to 2 bit by this transformation.

Test Response Tracing

The target paths of the proposed measurement are single-path sensitizable. However, some applications require lowest failing frequency, and trace the test response sequence in a continuous sensitization of the path under

measurement with reducing the test clock frequency.

In single-path sensitizable path measurement, it is guaranteed that once the test fails, the test with higher frequency than the failing frequency is fail.

But in single-path unsensitizable path measurement (for example, multiple reconvergent paths), it is not guaranteed. For example, in case of the example of Fig. 3, only the 6 patterns, "*FFFFF*", "*PFFFF*", "*PPFFF*", "*PPPFF*", "*PPPPF*", and "*PPPPP*" should be considered.

When a single-path unsensitizable path is measured, we could have responses such as "*PPFPF*". For such a case, the proposed method has the test response tracing mode as an optional function. In this mode, the test response patterns are not compacted by signature registers. We get the raw test response pattern. This mode is realized by cutting off the feedback loop with *sge* = 0 during the measurement.

SIMULATION RESULTS

Variable Clock Generator

The Variable Clock Generator Generates 2 Pulse Signal Output, which is applied to Signature Registers & Scan Flip Flop for operation. The simulated out put waveform is as shown in below Figure 10a.

Scan Flip Flops

The Scan Flip Flop uses a D-Flip Flop with Two 2 x 1 Multiplexers. When Se_0 = 1 and Se_1 = 1 it sends input *Si* to output *So* as shown in Figure 10b.

Signature Registers

The signature register can be configured to a shift register. The line sge controls the configuration. When *sge* = 1, it works as a signature register. When *sge* = 0, it works as a shift register. The line in is the input of the signature register. During measurement, test responses are sent to in. The line *clk* is clock line. The clock line is controlled by *sck*. The following Figure shows the out put waveforms for Signature Registers.

Figure 10a: Simulation OutPut Waveform of 2-Pulse Generator

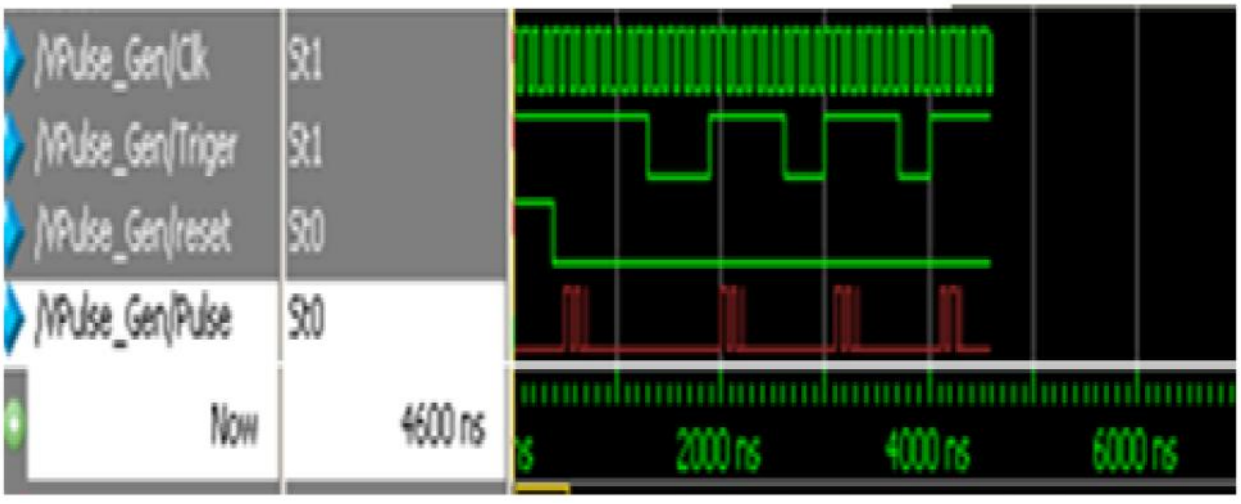


Figure 10b: Simulation OutPut Waveform of Scan Flip Flop

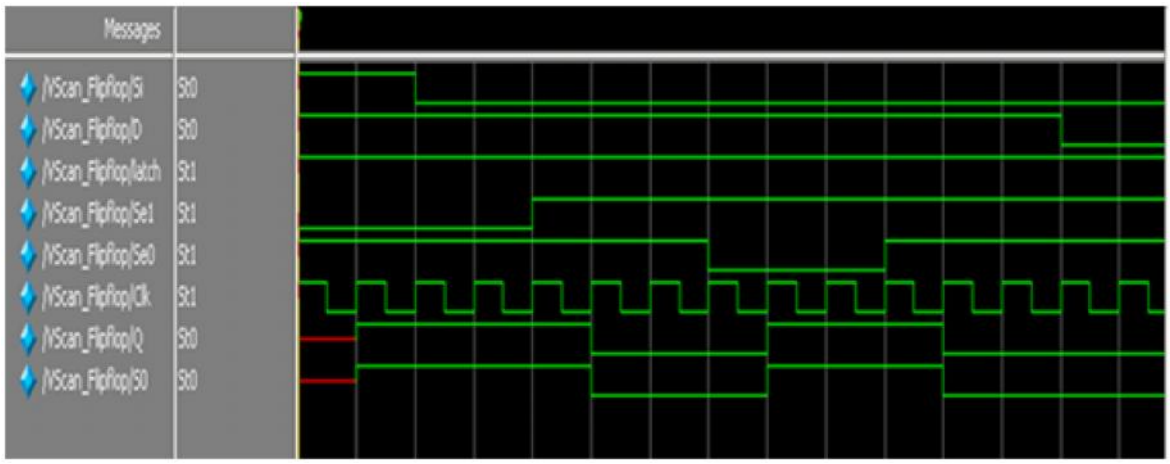
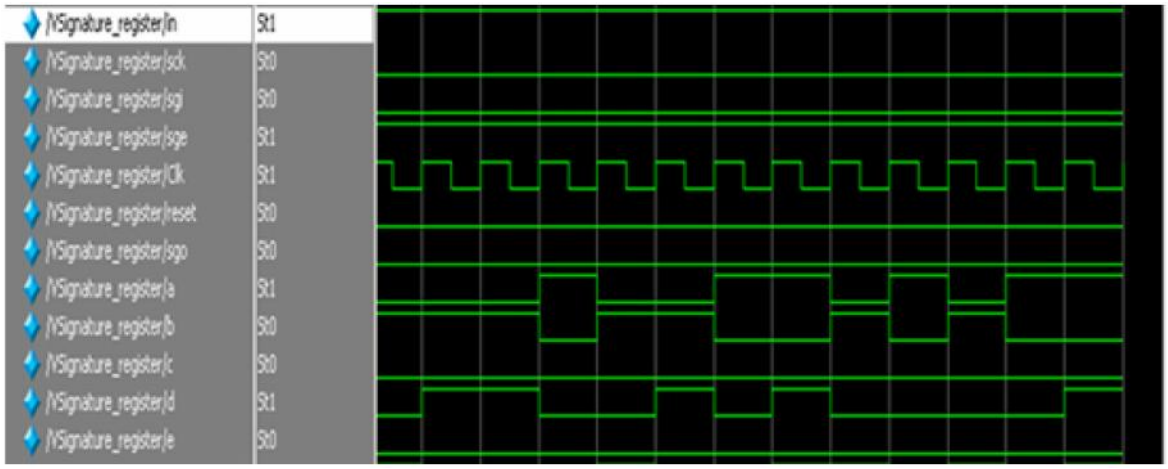


Figure 10c: Simulation OutPut Waveform of Signature Registers



When *sck* = 0, the signature register does not capture the input value. When *sck* = 1, the signature register captures the input value synchronizing with the positive edge of *clk*. By controlling *sck*, the signature registers capture only the target test response.

CONCLUSION

The proposals of this paper are as follows.

- The proposal of the delay measurement method using signature analysis and variable clock generator.
- The proposal of a scan design for the delay measurement of internal paths of *SoC*.

The first proposal can be applied not only *SoC* but also Field Programmable Gate Array (FPGA). Because the process of FPGA is getting extraordinary smaller these days, the small delay defect becomes serious problem in FPGA, too. In this meaning, the application of the proposed method to FPGA is also useful. A future work is the low cost application of the pro posed measurement to FPGA.

When we measure short paths the measurement error can increase for the IR drop induced by higher test clock frequency. It can reduce the test quality. Another future work is the reduction and the avoidance of the measurement error caused by the IR drop.

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