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Research Paper

MODIFIED SSC METHOD FOR DSM BUSES

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The power dissipated by Deep Sub-Micron Technology bus is directly related to the switching activity of the coupling capacitance that exist between the bus lines and also the switching activity of the self capacitance present between the bus interconnect and the ground. When there is an opposite swing in two wires the coupling capacitance between them is doubled and this phenomenon leading to more capacitance is called miller-effect which produces devasting effects in integrated circuits. In Deep Sub-micron Technology the power dissipation due to coupling transitions, is appreciably more (75%) than that due to self transitions (25%), necessitates the need for reducing the number of coupling transitions also. The main aim of the proposed technique in this paper is to save the energy dissipated due to the transitions on data buses.

Keywords: Buffer, Modularity, High Technology Product Producing Factory (HTPPF)

NEED FOR LOW POWER VLSI

Many of the issues in logic design today concern power dissipation. High-speed logic typically implies high power. As gates switch during their logic operations, they consume power. The more gates that switch and the faster they switch, the more power they will consume. Because of the demand for higher and higher speeds, the power dissipation reached unacceptable levels that eventually exceed 100 W. So, there is a need for low power VLSI to minimize the overall power consumed per logic operation (Jan, 2003).

In fact, it is difficult to determine the actual power dissipation of a chip early in the design process. Power for a gate can be computed accurately, but power for an entire chip can only be estimated, since it depends in large part on the activity of the chip. Also, power dissipation varies for logic, memory, clock, analog blocks, etc. Therefore, a variety of methods may be required to have a reasonable estimate of the total power.

The basic power equation is:

$$P = I \times V_{DD} \quad ...(1)$$

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I is the current flowing from V_{DD} to ground. The power dissipation of a logic gate may be broadly categorized into static and dynamic power. Static power involves power dissipation when the gate is not switching operations. The total power is a combination of the static power and dynamic power.

$$P_{total} = P_{static} + P_{dynamic} \quad ...(2)$$

Dynamic power is associated with switching from high-to-low and low-to-high. The power dissipated is a function of the voltage swing, capacitance, and switching frequency.

In Circuit design, we attempt to design high-performance circuits that dissipate low power. However, high-speed implies a large f and requires large transistors with large C. This unfortunately increases the overall power dissipation. Clearly, a power-delay tradeoff exists and we can only hope to balance the desired speed with the maximum allowable power dissipation.

There are many factors effecting dynamic power dissipation. They can be known from the equation of dynamic power. They are supply voltage, load capacitance, clock frequency and transition activity factor. It is well known that the dynamic power dissipation in CMOS VLSI circuits is given by Sainarayanan *et al.* (2006).

$$P_{dynamic} = \Sigma C_{load} f_{clk} (V_{dd})^2 \alpha \quad ...(3)$$

Where C_{load} is the total load capacitance attached to a bus line, V_{dd} is the voltage swing at operation; f_{clk} is the clock frequency and α is the switching factor. Switching activity factor α is related to the self capacitance, coupling capacitance and their switching activities.

There are several methods to achieve low power dissipation such as:

1. Reduction of the power supply voltage.
2. Reduction of voltage swing in all nodes.
3. Reduction of the switching probability (transition factor).
4. Reduction of the load capacitance.

The reduction of these factors to improve the efficiency of VLSI circuits. One of the best ways to reduce power consumption is Reduction of the switching activity factor α by bus encoding techniques.

The power dissipated by DSM bus is directly related to the switching activity of the coupling capacitance that exist between the bus lines and also the switching activity of the self capacitance present between the bus interconnect and the ground. In Deep Sub-micron Technology the power dissipation due to coupling transitions, is appreciably more (75%) than that due to self transitions (25%), necessitates the need for reducing the number of coupling transitions also.

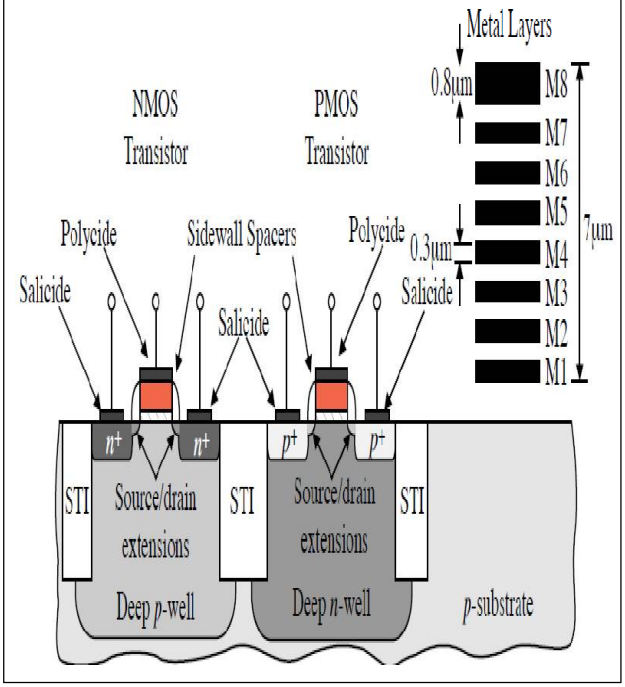
DEEP SUBMICRON TECHNOLOGY (DSM) TECHNOLOGY

Through the 1980s, available technologies were mostly in the 5 µm to 1 µm range. This dimension nominally refers to the channel length of the transistor. It also refers to the minimum resolvable geometry on a given layer of metal in the integrated circuit, specifically, the metal line widths or metal-to-metal spacing (metal pitch). Due to advances in photolithography, the minimum dimension in a technology, eventually led to line widths that were below 1 µm. This was referred to as submicron era, at one time thought unreachable. However, scaling continued

aggressively to the point where 0.5 µm and 0.35 µm line widths were achieved by the mid1990s. Many argued that 0.35 µm technology would be physical limit for photolithography since the wavelength of light is approximately equal to this value. However further advances allowed scaling below this barrier. At this point, the term deep submicron (DSM) was coined to emphasize that we had gone beyond another scaling limit, and well below the 1 µm barrier. So, "DSM technology is that which has typically a minimum channel width between 0.35 µm to 0.13 µm." (Jan, 2003).

Though the DSM Technology has some advantages like decrement in size of transistor, there are some disadvantages also. The wires connecting the transistor began to introduce additional RC delays in the circuit due to increased resistance.

Figure 1: An Illustration of DSM Technology



Furthermore, coupling between lines caused delay variations and noise injection. All these issues were referred to as signal integrity problems and they characterize the deep submicron era. To reduce coupling effects between wires low-k dielectrics were introduced. These technologies go by names Very Deep Submicron (VDSM) and Ultra-Deep Ssubmicron (UDSM).

DSM WIRES IMPACT ON VLSI DESIGN METHODOLOGY

In deep submicron technologies, degraded interconnect performance and high-speed operation reduce system noise immunity and timing budget which in turn result in faults in system operation. A major impact of interconnects on chip design is that they blur the traditional distinctions between logic design, circuit design and physical design. In old design methods, unawareness of accurate interconnect information in logic design causes the timing closure problem in DSM regime.

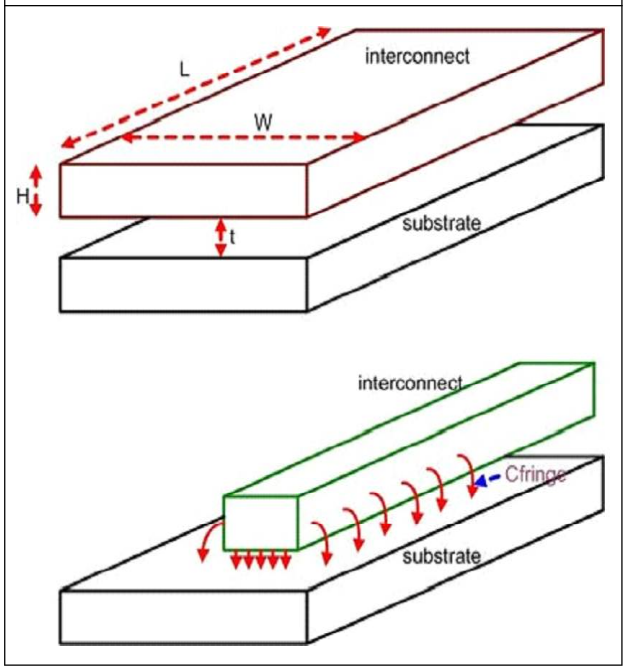
As technology node shrinks (scaling), to minimize resistance of the wires, it is desirable to keep the cross section of the wire (WXH) as large as possible. But this increases area. Small values of W lead to denser wiring and less area overhead. In advanced process W/H ratio has reduced below unity. Under such circumstances parallel plate capacitance model becomes inaccurate. The capacitance between the sidewall of the wires and substrate called fringing capacitance can no longer be ignored and contributes to the overall capacitance.

Inter-wire capacitance become dominant factor in multilayer interconnect structures (Jan,

2003). As interconnect size is scaled down in DSM VLSI, interconnect delay increases significantly. When the cross-coupling capacitance is comparable to or exceeds the loading capacitance on the wires, the delay of such a transition may be twice or more that of a wire transitioning next to a steady signal. We call this delay penalty the "crosstalk delay".

The cross talk delay is mostly caused by the miller-like effects when adjacent wires simultaneously transmit in opposite status (Sotiriadis, Ananth, 2001, 2002 and 2003).

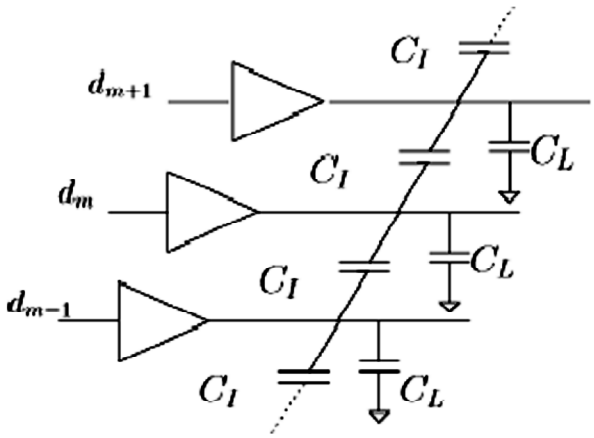
Figure 2: Inter Wire Capacitance



When there is an opposite swing in two wires the coupling capacitance between them is doubled and this phenomenon leading to more capacitance is called miller-effect which produces devasting effects in integrated circuits.

For Example, Consider 3 wires in DSM Technology as shown in Figure 3, in which the middle one is target wire. If the target wire is

Figure 3: On-Chip Bus with Crosstalk



switching in one direction, while the other 2 wires are switching in the opposite direction then the effective coupling capacitance gets doubled compare to the case, when the neighbours are quite. On the other hand if all the 3 wires are switching in the same direction then the coupling capacitance becomes effectively zero.

Since DSM effects can significantly impact the energy consumed and crosstalk delay in interconnects, it is necessary to model the effect of nanometer technologies on interconnect energy dissipation at a high level so that designers can be aware of the energy consumption of their designs.

It is an established fact that reducing switching activity eventually reduces the energy dissipation. Transition activity on the data bus can be reduced by employing bus encoding techniques. Therefore, It is important to minimize the power dissipation and cross talk delay by minimizing the both self transitions and coupling transitions on bus for the fast and safe VLSI circuits. Several bus encoding techniques have been proposed to reduce energy consumption during bus transmission

in literature. The main research work has focused on reducing the dynamic power consumed by reducing the number of change of states on the bus.

EXISTING WORKS ON BUS ENCODING

Bus power reduction has become dominant in advanced technologies. Some of the existing techniques aim at reducing data bus transitions (switching activity) during transmission of data. They attempt to reduce the power dissipation by minimizing the bus transitions.

Among them, Bus Invert method (BINV) introduced by Stan and Burelson (1995), attempts at reducing the power dissipation by minimizing the number of self transitions. According to this method, if the number of bits that change is more than half the width of the bus, then the entire bus is inverted and transmitted. For decoding purpose, an additional bit is transmitted with the original data, it is used to know whether the bus is inverted or not. But in this method only it concentrates on self transitions not in coupling transitions .This is one disadvantage with bus invert method.

Another encoding technique called "Sequence Switch Coding for low-power data transmission" (SSC) (Myungchul, 2004) was proposed by Myungchul Yoon. The SSC technique aims at applications with the stream type data transfer pattern. SSC technique reduces the number of bus transitions by rearranging the transmission sequence of data. An algorithm called lagger algorithm is presented to show the feasibility of Sequence Switch Coding (SSC). In this technique, the number of Self Transitions (ST) of two successive data items is measured at a time with respect to the previously transmitted data on bus. Among them, the data with minimum self transitions is selected for transmission (winner), while the other data item is held as a logger for the next computation of self transitions.

The SSC method, proposed a technique to reduce self switching activity on the buses by rearranging of the data. It is suitable for both random data and stream type of data. It also needs one extra line to send the control information to indicate that the data is present data or the next data. This algorithm reduces around 20% of bus transitions in transmission of the Random Vectors. When a sequence of data moves through a bus, its transmission sequence can be chosen to minimize the number of bus transitions.

The Shift Inver Bus encoding method is proposed by Samala (Jaya and Damu, 2004), which aims to reduce coupling capacitance. The Shift invert is efficient for self transition, but it possesses less reduction rate than Bus Invert and SSC methods.

The techniques of Bus invert (Stan and Burelson, 1995), Sequential Switch Coding (Myungchul, 2004) and Shift Invert method (Jaya and Damu, 2004) are incomplete in the sense that they minimize only the self transitions in reducing the total power dissipation. The technique "Odd/Even bus invert with two phase transfer for buses with coupling" (OE-BI) introduced by Yan *et al.* (2002) finds relevance in this context. It considers reduction of both self and coupling transitions. However it requires more wire

redundancy than Bus Invert and Sequential Switch Coding techniques.

The proposed technique in this paper is modified version of the Sequential Switch Coding given by Myungchul (2004) and the modified procedure is given below to which we have developed and obtained better reduction in energy and delay. The proposed technique requires less wire redundancy than OE-BI technique proposed by Yan *et al.* (2002).

PROPOSED CODING TECHNIQUE

Steps for the proposed algorithm:

- Read a file.
- Measure the total no. of coupling transitions and self transitions of the given file.
- Initialize the status of the 8-bit bus.
- Initialize the control line *S* to '0'.
- Read next 8 bit data.
- Measure the coupling transitions C_t, of the data.
- Measure and note the hamming distance between the data on the bus and the 8 bit data, St (self transitions).
- Measure Total transitions, $Tt_1 = C_t + S_t$.
- Read the next data.
- Measure the coupling transitions, C_t of the data.
- Measure and note the hamming distance between the data on the bus and the 8 bit data, S_t (self transitions).
- Total transitions, $Tt_2 = C_t + S_t$.
- If $Tt_1 < Tt_2$.
- Put new data on the bus, and make $S = 1$ and transmit;
- If $Tt_1 > Tt_2$, put previous data on the bus, and make $S = 0$ and transmit;
- Do steps 5 to 15 till the end of the file.

SIMULATION RESULTS OF THE PROPOSED TECHNIQUE

The main aim of the proposed technique is to save the energy dissipated due to the transitions on data buses. Since coupling transitions are reduced the errors due to crosstalk also reduces. The proposed technique performance is compared with other six existed methods. The above proposed technique is simulated using random function in C language software and tested with 10^5 random vectors. The simulations are performed on 8-bit, 16-bit, 32-bit and 64-bit data buses with three groups of data vectors. Self transitions and Coupling transitions are considered as metric parameters. Self and coupling transitions are separately calculated. This technique is aimed to reduce energy dissipation and achieves 26.4% reduction in energy dissipation and 15.7% reduction in Crosstalk delay in DSM technology inter connects. The main advantage of proposed technique is that its efficiency in reduction of energy dissipation is 7% more than that SSC Technique.

CONCLUSION

Our modifications to the SSC technique results in reducing the coupling transitions better than any other scheme reported so far. In the case of standard one lakh randomly generated data vectors the percentage of reduction in coupling transitions and self transitions is found to be higher than the nearest reported value.

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