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*Research Paper*

# MODIFIED BUS INVERT TECHNIQUE FOR LOW POWER VLSI DESIGN IN DSM TECHNOLOGY

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The two main sources of power dissipation in CMOS circuits are static current, which results from resistive paths between power supply and ground, and dynamic power, which results from switching capacitive loads between different voltage levels. Reducing power dissipation has become an important objective in the design of digital circuits. Because, for every 10 °C increase in operating temperature a component' s failure rate is doubled. In this context, peak power for maximum possible power dissipation is a critical design factor as it determines the thermal and electrical limits of designs, impacts the system cost, size and weight, dictates specific battery type, component and system packaging and heat sinks, and aggravates the resistive and inductive voltage drop problems. It is therefore essential to have the peak power under control. The cross talk is dependent on the data transition patterns on the bus. The fact that power dissipation due to coupling transitions, is appreciably more (75%) than that due to self transitions (25%), necessitates the need for reducing the number of coupling transitions also. This makes the Bus Invert method incomplete in reducing the power dissipation. The simulation results of our work shows that the power dissipation in a bus is reduced about 28.02% with the proposed bus encoding technique.

***Keywords:*** DSM, VLSI, Self transitions, Coupling transitions, CODEC

## INTRODUCTION

Power dissipation has been considered as one of the very critical issues in the performance of the high speed VLSI circuits because of rapid growth of portable wireless applications and battery powered devices (Pedram, 1996). There are several methods to achieve low power dissipation such as reducing the supply voltage, the voltage swing, the load capacitance and switching activity (Pedram, 1996). Although these methods try to minimize the power dissipation, still all the energy down from the dc power supply is completely dissipated in the circuit (Denker, 1994). Power dissipation in the data bus can be reduced by reducing the transition activity

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on interconnects, which in turn reduces crosstalk. Various coding techniques have been proposed by several authors to reduce the Deep Submicron model and the energy model used in the power dissipation in integrated circuits.

## ENERGY AND DELAY IN CMOS CIRCUITS

The two main sources of power dissipation in CMOS circuits are static current, which results from resistive paths between power supply and ground, and dynamic power, which results from switching capacitive loads between different voltage levels. There is a third source of power dissipation in CMOS circuits, short-circuit current, which results from both transistors in a CMOS inverter being on at the same time while the input switches. The short-circuit component is small, therefore we ignore it throughout this paper. Static power is due to current sources and to leakage current when a transistor is nominally off.

The average power dissipation on the bus is given by

$$P_{ave} = ½ \times (\alpha_c C_s + \alpha_c C_c) f_{clk} VDD^2 \quad ...(1)$$

And average power consumption on the bus is given by

$$P_{con} = (\alpha_c C_s + \alpha_c C_c) f_{clk} VDD^2 \quad ...(2)$$

Power consumption on a bus takes place only during the transitions from 0 to 1 at the output, where as power dissipation on a bus occurs in both transitions, i.e., from 0 to 1 and 1 to 0.

It is well known that the dynamic power dissipation in CMOS VLSI circuits is given by

$$P_{dynamic} = \Sigma C_{load} f_{clk} (V_{dd})^2 \alpha \quad ...(3)$$

where $C_{load}$ is the total load capacitance attached to a bus line, $V_{dd}$ is the voltage swing at operation; $f_{clk}$ is the clock frequency and $\alpha$ is the switching factor. Switching activity factor $\alpha$ is related to the self capacitance, coupling capacitance and their switching activities.

## PREVIOUS WORK ON BUS ENCODING

Bus power reduction has become dominant in advanced technologies. Some of the existing techniques aim at reducing data bus transitions (switching activity) during transmission of data. They attempt to reduce the power dissipation by minimizing the bus transitions. Among them, Bus Invert method (BINV) introduced by Stan and Burleson (1995), attempts at reducing the power dissipation by minimizing the number of self transitions. In this, the Hamming Distance (HD) between the present data on the bus and previous encoded data is measured. If HD is more than half of the bus width, the data is inverted before being sent on the bus. It needs one extra line to send the coding information to the decoder. In deep sub micron technology, coupling transitions also affect the power dissipation predominantly. This is due to the presence of the coupling capacitance. The fact that power dissipation due to coupling transitions, is appreciably more (75%) than that due to self transitions, (25%) (Bakoglu, 1990), necessitates the need for reducing the number of coupling transitions also. This makes the Bus Invert method incomplete in reducing the power dissipation.

Another technique introduced by Ravindra *et al.* (1990) also aims to reduce the total number of transitions.

Another similar technique introduced by Natesan and RadhaKrishnan (2004) also suffers with the same limitation. Many techniques have been later developed to reduce coupling activity along with the self activity. Yan *et al.* (2002) introduced a new technique which considers reduction of both self and coupling transitions. The authors claim a reduction of 10% in coupling transition. But, the main drawbacks of this technique are

- Firstly, encoding is done only when the number of transitions of the data word is more than half the word length.
- Secondly, the author has not considered the original self-transitions of the un-encoded data.

For 25% of combinations of data ranging from 20 to 28 and 25% of any randomly generated data has the probability to have Original Coupling Transitions (OCT) as half the word length. But, for those data's the author Naveen (2004) not offering any encoding process and simply passing as it is.

Another important observation is that, the data that has OCT equal to half word length is simply passes in its original form, though it has maximum number of self- transitions. From this observation it is clear that there are possibilities to increase the self-transitions. But, due to this flaw, the efficiency of this technique is not fully extended to all the possible conditions.

In our paper, we develop a new technique with only one wire redundancy, irrespective of data width, to get better coupling transition reduction rate than the existing techniques followed by simulation results and conclusions.

## ALGORITHM FOR PROPOSED TECHNIQUE

*B = Bus width; N = Number of data items to be transmitted;*

*C = 0; // Case 0; only odd items of the data are inverted and the even data items are kept as it is and transmitted as encoded data //*

*C = 1; // Case 1; only even items of the data are inverted and odd data items are kept as it is and transmitted as encoded data //*

*K = 1 to N;*

$D_0$ *= First data item (assumed as either "00000000"or "11111111")*

$D_K$ *= Next data item.*

$ODST(D_K)$ *= Self-transitions of odd data items.*

$EVST(D_K)$ *= Self-transitions of even data items.*

$D_K^{11}$ *= Encoded form of data* $D_K$.

$D_K^{1}$ *= Encoded form of data with inverted odd data items.*

$D_K^{2}$ *= Encoded form of data with inverted even data items.*

**Start:** *Compute ODST and EVST of* $D_K$

*If* $ODST(D_K) \geq EVST(D_K)$ *then*

*//Case 0//*

$D_K^{11} = D_K^{10}$

$Bus \leftarrow D_K^{11}$

$D_{K-1} \leftarrow D_K^{11}$

$K = K + 1;$

*If* $K \leq N$, *go to Start*

*else*

*end*

*else*

$D_K^{11} = D_K^{21}$

$Bus \leftarrow D_K^{11}$

*//Case 1//*

$D_{K-1} \leftarrow D_K^{11}$

$K = K + 1;$

*If* $K \leq N$, *go to Start*

else

*End*

## SIMULATION RESULTS:

Performance of this technique is evaluated for $10^6$ random data vectors of 8 bit width and the proposed coding scheme has been implemented using Verilog and simulated using MODELSIM for 16 and 32 bit bus. It is found from our simulation results that the power saved using the proposed method is high, when compared to other methods which employ more than one wire redundancy. The proposed encoding scheme reduces 28.02% of energy and 16.02% of Crosstalk delay. Thus the proposed bus encoding scheme is suitable for reducing the power dissipation and cross talk delay in VLSI circuits. However, both complexity and overhead depend strongly on the particular technology, as well as the specific circuit implementation that will be used.

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