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Research Paper

BUS AFFECTS IN DEEP SUB-MICRON TECHNOLOGY AND METHODS TO REDUCE COUPLING EFFECTS

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Power dissipation is a problem of increasing concern to designers of VLSI circuits. To increase the performance and reliability of highly integrated circuits like DSP processors, Microprocessors and SoCs, transistors sizes are continues to scale towards Deep Submicron and Very Deep Submicron dimensions. The inter-wire spacing in a VLSI chip becomes closer as the VLSI fabrication technology rapidly evolves. It is important to minimize the crosstalk for the fast and safe VLSI circuits. As more and more transistors are packed on the chip to increase the functionality more metal layers are being added to the integrated chips. Bus encoding technique is the promising method to reduce the both energy dissipation and crosstalk delay in integrated circuits like DSP processors, Microprocessors and SoCs. With the proposed bus encoding technique in this paper, both energy and crosstalk delay have been minimized with reference to coded and un-coded bus for different widths.

Keywords: DSM, VLSI, Self transitions, Coupling transitions, Crosstalk delay

INTRODUCTION

Moore's Law is a phenomenological observation that the number of transistors on integrated circuits doubles every two years, as shown in Figure 1 (www.en.wikipedia.org). Numerous innovations by a large number of scientists and engineers have been significant factors in the sustenance of Moore's law since the beginning of the Integrated Circuit (IC) era.

The observation made in 1965 by Gordon Moore, co-founder of Intel, that the number of transistors per square inch on integrated circuitshad doubled every year since the integrated circuit was invented. Moore predicted that this trend would continue for the foreseeable future. In subsequent years, the pace slowed down a bit, but data density has doubled approximately every 18 months, and this is the current definition of Moore's

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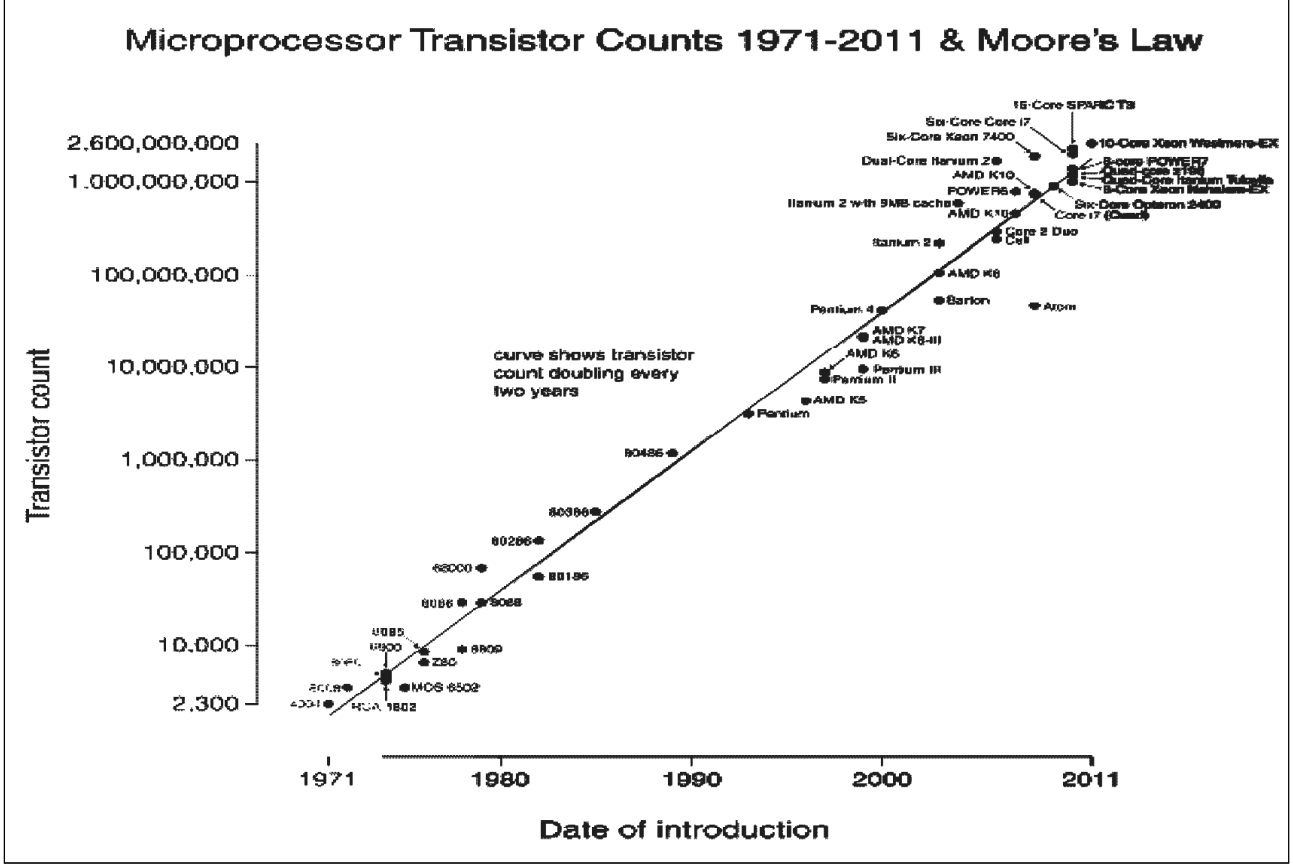
Figure 1: Moore's Law



Law, which Moore himself has blessed. Most experts, including Moore himself, expect Moore's Law to hold for at least another two decades. If we look into the processor speeds from the 1970's to 2009 and then again in 2010, one may think that the law has reached its limit or is nearing the limit.

In the 1970's processor speeds ranged from 740 KHz to 8MHz; notice that the 740 is KHz, which is Kilo Hertz—while the 8 is MHz, which is Mega Hertz. From 2000-2013 there has not really been much of a speed difference as the speeds range from 1.3 GHz to 3 GHz, which suggests that the speeds have barely doubled within a 10 year span. This is because we are looking at the speeds and not the number of transistors; in 2000 the number of transistors in the CPU numbered 37.5 million, while in 2013 the number went up to an outstanding more than 1000 million; this is why it is more accurate to apply the Moore's Law to the modern VLSI designs. Moore's Law, essentially described the basic business model for the semiconductor industry. Continuing Moore's Law means the rate of progress in the semiconductor industry. This trend has continued for more than half a century. Several Researchers in 2005 expected it to continue until at least 2015 or 2020.

It is well known that the dynamic power dissipation in CMOS VLSI circuits is given by Stan and Burleson (1995).

$$P_{dynamic} = \Sigma C_{load} f_{clk} (V_{dd})^2 \alpha \quad ...(1)$$

where C_{load} is the total load capacitance attached to a bus line, V_{dd} is the voltage swing at operation; f_{clk} is the clock frequency and á is the switching factor. Switching activity factor α is related to the self capacitance, coupling capacitance and their switching activities.

According to Moore's law, transistor dimensions are scaled by 30% (0.7x) every technology generation, thus reducing their area by 50%. This reduces the delay (0.7x) and therefore increases operating frequency by about 40% (1.4x). Finally, to keep electric field constant, voltage is reduced by 30%, reducing energy by 65% and power (at 1.4x frequency) by 50%, since active power = CV^2f. Therefore, in every technology generation transistor density doubles, circuit becomes 40% faster, while power consumption (with twice the number of transistors) stays the same. (www.en.wikipedia.org, Shekhar and Andrew, 2011).

If chip architects simply add more cores as transistor-integration capacity becomes available and operate the chips at the highest frequency the transistors and designs can achieve, then the power consumption of the chips would be prohibitive. Chip architects must limit frequency and number of cores to keep power within reasonable bounds, but doing so severely limits improvement in microprocessor performance. Therefore, the power consumption will be the key limiter of performance. However, as the channel length is reduced, the performance improves, the power per switching event decreases, and the density improves. But the power density, total circuits per chip, and the total chip power consumption has been increasing.

TECHNOLOGY SCALING IMPACT ON POWER CONSUMPTION

Transistor scaling is the primary factor in achieving high-performance microprocessors and memories. Each 30% reduction in CMOS IC technology node scaling has (Shahidi, 2000; and Nassif, 2000:

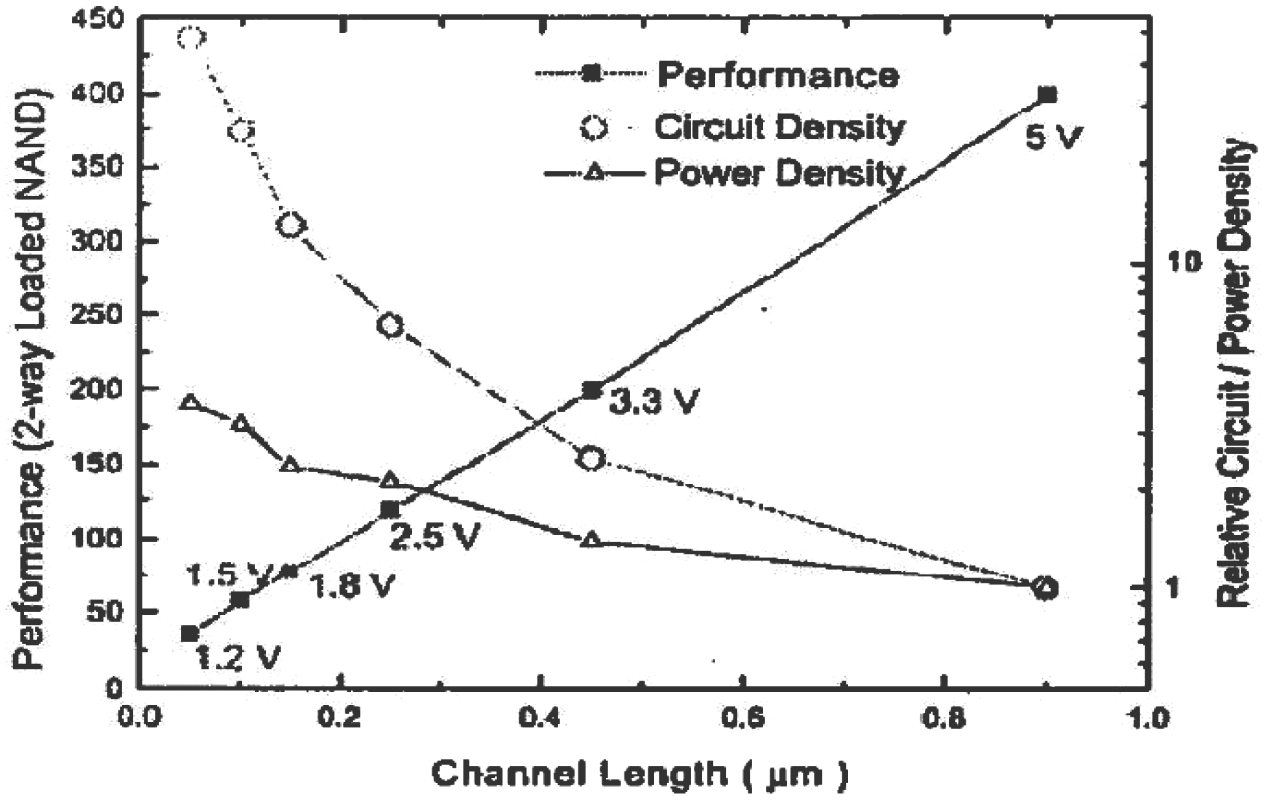
- Reduced the gate delay by 30% allowing an increase in maximum clock frequency of 43%;
- Doubled the device density;
- Reduced the parasitic capacitance by 30%; and
- Reduced energy and active power per transition by 65% and 50%, respectively.

Figure 2 shows CMOS performance, power density and circuit density trends, indicating a linear circuit performance as a result of technology scaling.

Dynamic power and leakage current are the major sources of power consumption in CMOS circuits. Leakage related power consumption has become more significant as threshold voltage scales with technology.

Figure 2 (Viswanath *et al.*, 2000) illustrates how the dynamic and leakage power consumption vary across technologies, where Pact is the dynamic power consumption and Pleak is the leakage power consumption. The estimates have only captured the influence of sub-threshold currents since they are the dominant leakage mechanism. For sub-100

Figure 2: CMOS Performance, Power Density and Circuit Density Trends



nm technologies, temperature has a much greater impact on the leakage power consumption than the active power consumption for the same technology. With continuing aggressive technology scaling, it is increasingly difficult to sustain supply and threshold voltage scaling to provide the required performance increase, limit energy consumption, control power dissipation, and maintain reliability.

DSM WIRES IMPACT ON VLSI DESIGN METHODOLOGY

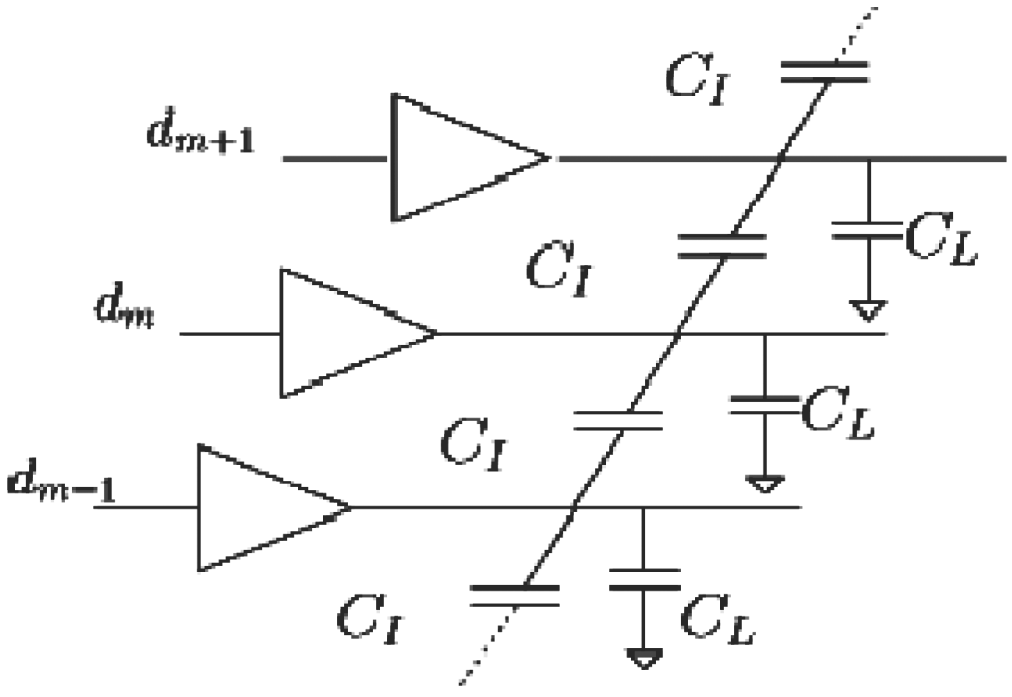
In deep submicron technologies, degraded interconnect performance and high-speed operation reduce system noise immunity and timing budget which in turn result in faults in system operation. A major impact of interconnects on chip design is that they blur the traditional distinctions between logic design, circuit design and physical design. In old design methods, unawareness of accurate interconnect information in logic design causes the timing closure problem in DSM regime.

As interconnect size is scaled down in DSM VLSI, interconnect delay increases significantly. When the cross-coupling capacitance is comparable to or exceeds the loading capacitance on the wires, the delay of such a transition may be twice or more that of a wire transitioning next to a steady signal. We call this delay penalty the “crosstalk delay”.

The cross talk delay is mostly caused by the miller-like effects when adjacent wires simultaneously transmit in opposite status (Sotiriadis and Anantha, 2001, 2002 and 2003). When there is an opposite swing in two wires the coupling capacitance between them is doubled and this phenomenon leading to more capacitance is called miller-effect which produces devasting effects in integrated circuits. For Example, Consider 3 wires in DSM Technology as shown in Figure 3, in which the middle one is target wire. If the target wire is switching in one direction, while the other 2 wires are switching in the opposite direction then the effective coupling capacitance gets doubled compare to the case, when the neighbours are quite. On the other hand if all the 3 wires are switching in the same direction then the coupling capacitance becomes.

Effectively zero. Since DSM effects can significantly impact the energy consumed and crosstalk delay in interconnects, it is necessary to model the effect of nanometer technologies on interconnect energy dissipation at a high level so that designers can be aware of the energy consumption of their designs.

Figure 3: On-Chip Bus with Crosstalk



In some high-speed designs where crosstalk delay would have limited the clock speed, the technique of shielding was used. This involves putting a grounded wire between every signal wire on the bus. Although this certainly is effective in preventing crosstalk within the bus, it has the effect of doubling the wiring area.

Different approaches have been proposed for crosstalk reduction in the context of bus interconnects. Some schemes focus on reducing the energy consumption, some focus

on minimizing the delay and other schemes address both.

BUS ENCODING TECHNIQUES TO MINIMIZE COUPLING EFFECT

In deep sub micron technologies, the coupling capacitances are becoming dominant for the total energy dissipation on buses. Various techniques have been proposed to reduce the power dissipation due to switching activity on bus. Thus, the power on bus can be reduced by reducing the transition activity on buses.

The Intrinsic capacitances of the bus lines, a sufficient amount of power is required at I/O lines of system when data travelled on the bus. Power has become an important design criterion in battery operated systems. There are many encoding schemes in the literature gives how to reduce the power consumption on buses.

An encoding scheme called T0 coding (Benini *et al.*, 1997) was proposed for the instruction address bus. This coding uses an extra bit line, an increment bit-line along with the address bus, which is set when the addresses on the bus are sequential, in which case the data on the address bus is not altered. When the addresses are not sequential, the actual address is put on the address bus.

Bus-Invert (BI) coding (Stan and Burleson, 1995) is proposed for reducing the number of transitions on a bus. In this scheme, before the data is put on the bus, the number of transitions that might occur with respect to the previously transmitted data is computed. If the transition count is more than half the bus width, the data is inverted and put on the bus. An extra bit line is used to signal the inversion on the bus. Variants of T0, T0_BI, Dual T0, and Dual T0_BI (Stan and Burleson, 1997) are proposed which combines T0 coding with Bus-Invert coding. Ramprasad *et al.* (1999) described a generic encoder-decoder architecture, which can be customized to obtain an entire class of coding schemes for reducing transitions. The same authors proposed INC-XOR coding, which reduces the transitions on the instruction address bus better than any other existing technique.

An adaptive encoding method is also proposed by Ramprasad *et al.* (1999), but with huge hardware overhead. This scheme uses a RAM to keep track of the input data probabilities, which are used to code the data. Another adaptive encoding scheme is proposed by Benini *et al.* (2000), which does encoding based on the analysis of previous N data samples. This again has huge computational overhead. Musoll *et al.* (1998) propose a Working Zone Encoding (WZE) technique, which works on the principle of locality. Although this technique gives good results for data address buses, there is a huge delay and hardware overhead involved in encoding and decoding. Moreover this technique requires more extra bit lines leading to redundancy in space.

There are so many techniques have been proposed to reduce the coupling activity along with the self-switching activity. Initially, Bus invert method (Stan and Burleson, 1995) can be applied to encode buses without prior knowledge of data statistics.

Another encoding technique called "Sequence Switch Coding for low-power data transmission" (SSC) was proposed by Myungchul (2004). In this technique, the

number of Self Transitions (ST) of two successive data items is measured at a time with respect to the previously transmitted data on bus. Among them, the data with minimum self transitions is selected for transmission (winner), while the other data item is held as a logger for the next computation of self transitions.

Among the Bus Invert method and Sequence Switch Coding, the Bus Invert method has gained popularity because of its better energy reduction (upto 25.45%). Both techniques need one extra wire (one wire redundancy) to send the coding information to the decoder. They reduce only self transitions and do not consider the effect of coupling transitions.

The sequence switch coding (Myungchul, 2004) method, proposed a technique to reduce self switching activity on the buses by rearranging of the data. It is suitable for both random data and stream type of data. It also needs one extra line to send the control information to indicate that the data is present data or the next data. In another method called Shift Invert coding for Low Power VLSI (Jaya and Damu, 2004), for each data, its inverted value, shift left equivalent value, shift right equivalent value are considered. This technique did not concentrate on coupling activity.

The techniques of Bus invert (Stan and Burleson, 1995), Sequential Switch Coding (Myungchul, 2004) and Shift Invert method (Jaya and Damu, 2004) are incomplete in the sense that they minimize only the self transitions in reducing the total power dissipation. The technique "Odd/Even bus invert with two phase transfer for buses with coupling," (OE-BI) introduced by Yan Zhang *et al.* (2002) finds relevance in this context. It considers reduction of both self and coupling transitions. However it requires more wire redundancy than Bus Invert and Sequential Switch Coding techniques.

The proposed techniques in this paper are modified version of the Sequential Switch Coding given by Myungchul (2004) and the modified procedure is given below to which we have developed and obtained better reduction in energy and delay.

EIGHT-BIT PARTITIONED APPROACH

In this approach, the wider bus is partitioned into sub buses of each 8 bit. Then, the following coding scheme is applied to individual sub buses.

Proposed Coding Technique

Steps for the proposed algorithm:

- Read a file.
- Partition the wider bus into sub buses of each 8 bit bus.
- Initialize the status of the 8-bit.
- Initialize the control line S to '0'.
- Measure the number of Coupling Transitions (Ct_1) of the first cycle.
- Read next sub-bus cycle.
- Measure the coupling transitions, Ct_2 of the data.
- If $Ct_{t1} < Ct_{t2}$,

  Put new data on the bus, and make $S = 1$ and transmit;

  else

put the previous data on the bus, and make $S = 0$ and transmit;

- Do steps 3 to 8 to all sub-buses of each 8-bit width.

SIMULATION RESULTS

The above proposed technique is simulated using random function in C language software and tested with 10^5 random vectors. This technique is aimed to reduce energy dissipation and achieves 25% reduction in energy dissipation and 16% reduction in Crosstalk delay in DSM technology inter connects. It is observed that the energy due to the coupling transitions and delay play a major role when technology shrinks.

CONCLUSION AND FUTURE WORK

A new transition reduction scheme is proposed in this paper. It considers both self and coupling transitions. Our future work is to test various ways to switch a data sequence, and to develop efficient ways for their implementation. The modifications done in our work to the Sequential Switch Coding given by Myungchul (2004) performs well in reducing the power consumption and cross talk delay, which are the two important sources need to be considered in low power VLSI design.

Given a specific bus structure and estimating or measuring the distribution of the data, the proposed algorithm provide coding scheme that, in theory, can result in significant energy reduction. For practical applications of a specific scheme, further work will be required to estimate the complexity and the energy overhead of the encoder and decoder. Both complexity and overhead depend strongly on the particular technology, as well as the specific circuit implementation that will be used.

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