International Journal of Electrical and Electronic Engineering & Telecommunications

ISSN 2319 – 2518 www.ijeetc.com
Vol. 1, No. 1, October 2012

Research Paper

AN ECONOMICAL APPROACH OF DESIGNING A THREE PHASE GRID TIED INVERTER FOR SOLAR APPLICATIONS

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Solar power is undoubtedly substitute for conventional energy as the fossil fuels are getting depleted. As the magnitude of solar power extraction is meager, paves the way to get connected to common grid. In order to bridge the gap between the nature of output of solar power (DC) and common grid (AC) the necessity of three phase inverter arises. The solar grid tied system comprises of a Photo Voltaic (PV) array, DC to DC boost converter, three phase inverter, low pass filter and isolation transformer. The three phase inverter acts as a backbone of the system. An attempt is made in this paper to demonstrate the economization of designing a SPWM by replacing a analog transformer by digital counters. The internal architecture of three phase inverter includes Gate driver, Sinusoidal Pulse Width Modulation (SPWM), Phase locked loop(PLL) ,low pass filter, snubber circuit. As the PLL topology is matched, the synchronization of inverter with grid is virtually realized. The three phase inverter output is observed by CRO and also validated by simulation using MATLAB simulink.

Keywords: Inverter, SPWM, PLL, Low pass filter

INTRODUCTION

One of the main issues of power system engineering is how to realize smart grid technologies, which power system that is capable of handling distribution resources, providing more economical service to end-is the users, and maintaining its conditions. Renewable energy sources are get in more attention as distributed generations in a smart grid.

Because energy resources and their utilization will be a prominent issue of this century, the problems of natural resource depletion, environmental impacts, and the

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rising demand for new energy resources have been discussed fervently in recent years. Several forms of renewable zero-pollution energy resources, including wind, solar, bio, geothermal have gained more prominence (Faete Filho and Yue Cao, 2010).

Solar energy is a kind of renewable energy, which utilize the solar photovoltaic power generation technology to convert solar radiation into electrical energy.

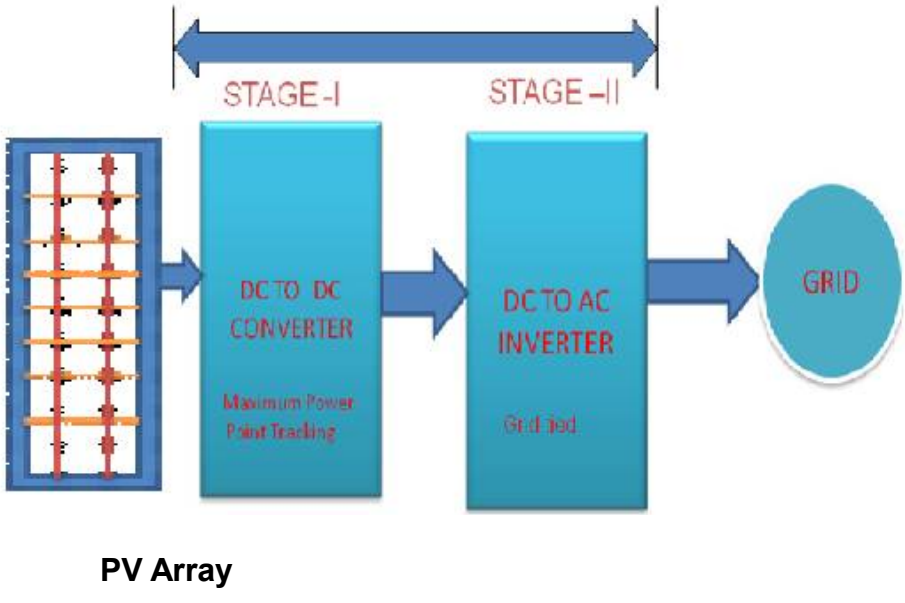
The PV system connected to grid is called Grid Connected PV system. Grid connected PV systems have become very popular because of their applications in distributed generation and for effectively using the PV array power. Grid connected systems does not need battery back-ups to ensure maximum power point tracking (MPPT (Potter *et al*., 2009)).

The Figure 1 shows a grid connected PV system with two stages to process PV power and feed into grid.

The first stage is used to boost the PV array voltage and track the maximum solar power. The second stage inverts this DC power into high quality AC power Therefore inverter research has also become important topic for a rational use of new energy.

Due to uneven or non-linear loads. grid voltage can be unbalanced including severe adverse effects such as reduced efficiency and decreased life of the system. For the unbalanced grid voltage condition, a three phase four wire configuration is required. Low pass filter designed to attenuate harmonics.

Figure 1: Block Diagram Of Two Stage Grid Tied System



DESIGNING DATASHEET

Input voltage	(V_i)	=	950 V
Output voltage	(V_0)	=	485 V
Output power (P_o) =			30 KW
Output current (I_0) =			37.1 A
Input current	(I_i)	=	31.5 A
Input power	(P_i)	=	30.13 KVA
IGBT rating		=	1200 V/70 A

Grid Voltages

For 3 phase Grid voltage = 430 V

Grid frequency = 50 Hz.

INVERTER CONTROL

Inverter circuit at workplace is as shown in Figure 2. A single-phase control method is expanded in a three-phase grid-tied inverter system with duplicating three individual phases with 120° apart .

Figure 3 shows the proposed three single phase grid-tie inverters with four-wire configuration Two renewable energy voltage sources, $1/2V_{dc}$, provide power and the middle point of two dc link capacitors, C_{dc}, is connected to the neutral point of the grid phase voltage source.

Low pass filter inductor(L_f), and output filter capacitor(C_f), make the square signals into smooth sinusoidal signals.

SPWM is used to control the inverter output voltage by comparing the reference low frequency with high frequency carrier wave.

Gate driver is used to isolated switching of 1200V/70A IGBTS. The SPWM output is given as input to the gate driver circuit, whose output is helpful for sequential switching of IGBTS.

Three phase grid voltages, v_{gan}, v_{gbn}, v_{gcn}, can be supplied through the isolation transformer, L_g and the capacitor voltages, v_{ga}, v_{gb}, v_{gc} are the voltages at the grid connection point. Synchronization between inverter and grid means that both will have the same phase angle, frequency and amplitude.

This can be done noise proof with respect to the grid by sensing the grid voltage in a Phase Locked Loop (PLL).Contactor is de-energizes the inverter when an external fault occurred by grid contribution.

Figure 2: Inverter Circuit Setup at Work Place

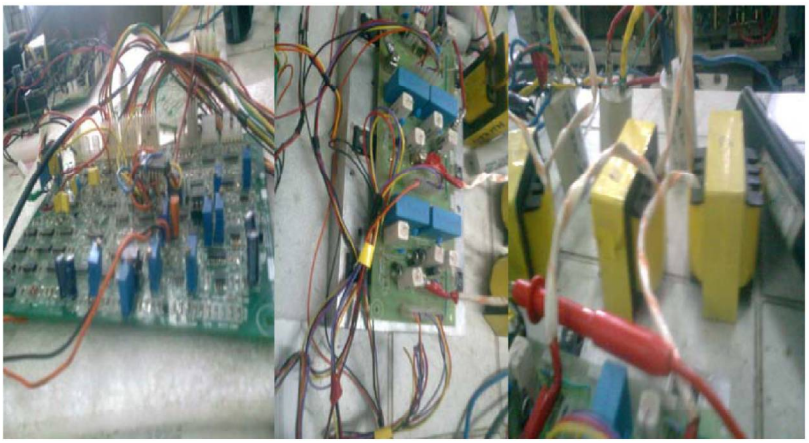
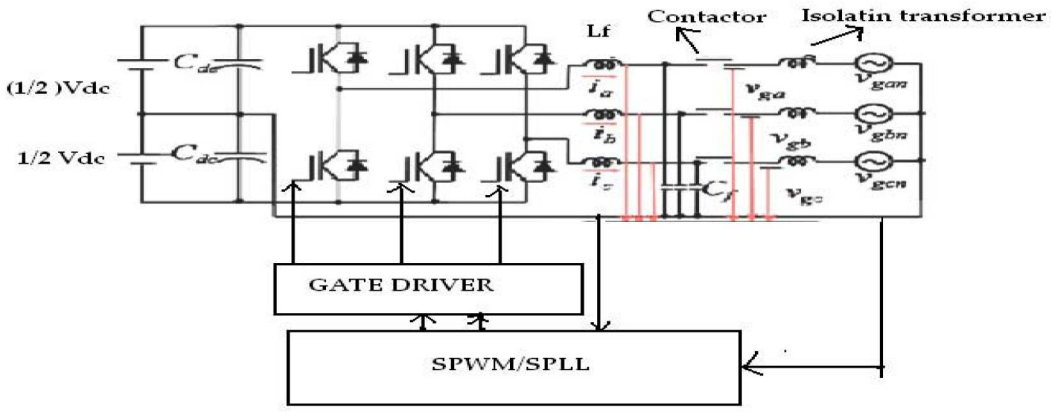
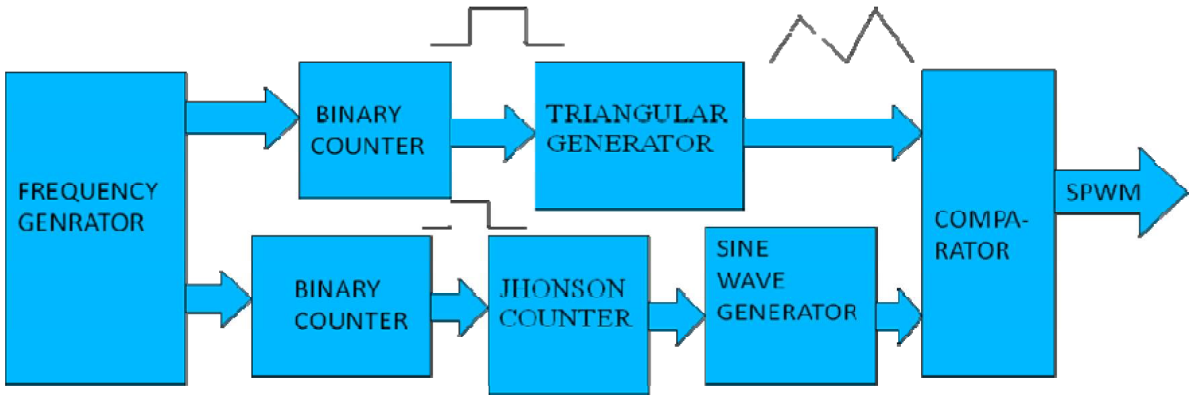


Figure 3: Three Phase Inverter Control Diagram



The main function of the PWM is to produce near sine-wave supply current with very low amplitude high frequency harmonic contents. Simple filters can easily remove such low amplitude high frequency harmonic contents Zhou Hai-feng and Wang Rong-jie (2009). In the case of sinusoidal PWM (SPWM) scheme, the control signal is generated by comparing a sinusoidal reference signal and a triangular carrier. In this implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative DC bus voltage is applied at the output. Over the period of one triangle wave, the average voltage applied to the load is proportional to the amplitude of the signal during this period. Block diagram of SPWM control of inverter is shown in Figure 4. From frequency generator a 5 MHz frequency signal is generated. This high frequency signal should be given to the binary counter (Frede Blaabjerg, 1997).

Figure 4: Blockdiagram of SPWM Circuit



SINUSOIDAL PULSE WIDTH MODULATION

The high frequency signal is divided in the form of square wave at desired frequency 20.35 KHz by using 14-stage binary counters. Then the square pulses are converted into triangular wave by triangular wave generator (Abdul Karewm *et al*.). The generated 20 K Hz triangular wave as shown in the Figure 5.

The digital controlled sine wave generator is proposed. From the frequency generator 5MHz frequency is generated. This high frequency should be given to the binary counter. By using binary counter and Johnson counter the high frequency signal is divided in the form of square wave at desired frequency 50 Hz .

This square pulses are converted into sine wave by using sine wave generator. At final carrier and sine waves are compared and the desired SPWM pulses are generated. The generated 50 Hz sine wave as shown in the Figure 6. The generated SPWM pulses are as shown in the Figure 7.

Feed Back Circuit

Block diagram of feedback circuit is as shown in Figure 8. Rectifier converts the inverter

Figure 5: Carrier wave of 20 KHz Frequency

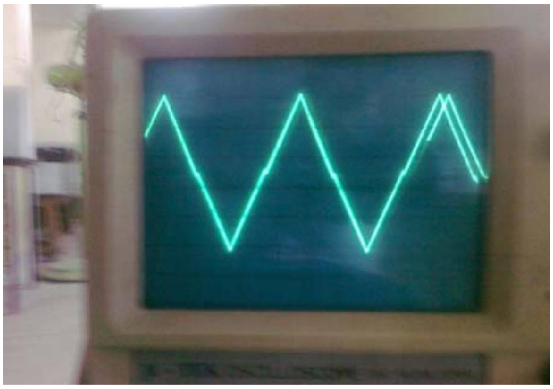


Figure 6: Sine Wave of 50 Hz Frequency

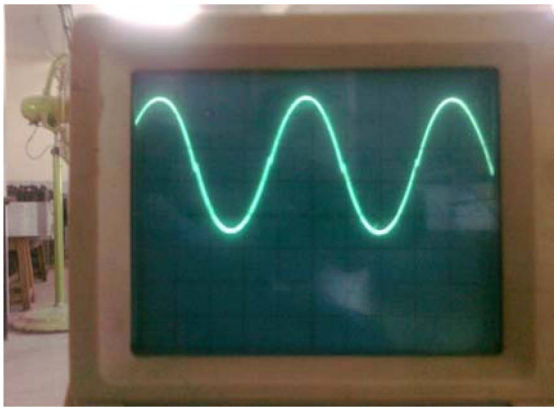
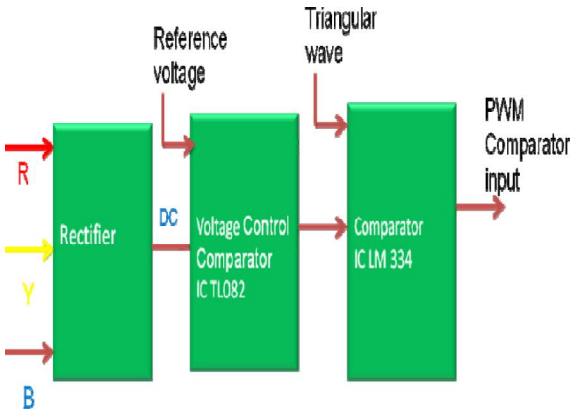


Figure 7: SPWM Output Pulses

Figure 8: Block Diagram of Feedback



output from(AC) to (DC). Rectifier output is compared with the reference voltage from IC TL082. The output of IC TLo82 is compared with the high frequency carrier wave so the resultant magnitude of carrier wave is controlled. This magnified carrier wave is compared with reference sine wave at SPWM comparator. In this for 3 phases SPWM 3 sine waves generators generate Sine-R, Sine-Y, Sine-B individual controlled blocks are developed. These 3 sine waves are compared with high frequency triangular wave and generates SPWM-R, SPWM-Y,SPWM-B with 120 Ω phase shift apart.

RCD SNUBBER DESIGN

The IGBT with RCD snubber circuit is as shown in Figure 9. In addition to peak voltage limiting, the circuit can reduce the total circuit loss, including both switching and snubber losses. Much better load lines can be achieved, allowing the load line to pass well within the SOA. For a given value of C_s, the total losses will be less. The shunt capacitance across the switch (C_s) is a useful part of the snubber (Abhijit D Pathak, 2001).

Capacitor Selection

Snubber capacitors are subjected to high peak and RMS currents and high d[V]/dt. CDE has several types of capacitors which are particularly well suited to snubber applications.

Diode Selection

The diode in an RCD snubber has to be rated for at least the peak voltage which appears on C_s. The peak current should be the basis for selecting the diode. The diode reverse recovery time (t_{rr}) can affect the snubber action and fast or ultra-fast diodes with t_{rr} < 100 ns are normally used. The performance of the diode should be verified in the circuit to be sure the snubber is performing as expected. Faster recovery diodes are generally used for high voltage rating. The forward recovery time (t_{fr}) may become a consideration. This is because the initial voltage drop across the diode, in the forward direction, can be much higher than the steady state conduction value for several hundred nano seconds. This problem is exacerbated by the very high d[I]/dt of typical snubber current waveforms.

Figure 9: IGBT with RCD Snubber

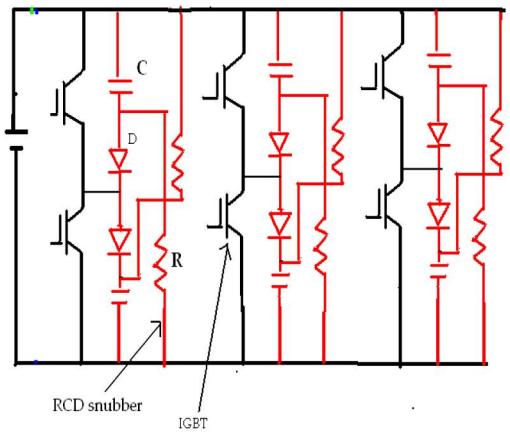


Figure 10: Inverter Output

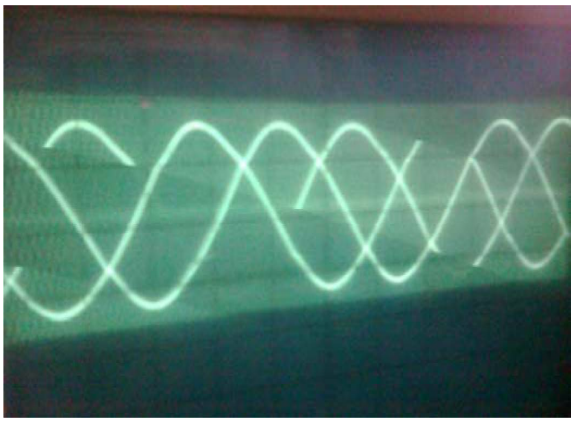


Table 1: 3-Φ inverter V_{phase},V_{line} Theoretical and Practical Calculations								
Theoretical			Practical					
V_S	$V_1 = 0.8165\ V_S$	$V_P = 0.4714\ V_S$	V_R	V_Y	V_B	V_{RY}	V_{YB}	V_{BR}
50	40.8	23.5	13.5	13.7	13.5	24.2	24.3	23.9
100	81.65	47.14	27.5	28.4	28.1	48.2	47.5	47.3
150	122.4	70.71	41.9	42.1	42	71.5	71.5	70.9
200	163.3	94.28	53.5	55.2	54.3	93	93.7	93.3
250	204.1	117.8	67.9	70.4	69	114.2	114.8	113.9
300	244.95	141.4	80.1	82.5	82.1	135.2	136	136
350	285.7	164.9	96.7	100	101	157.1	157.6	157.7
400	326.6	188.5	111.2	114.5	113.2	177.9	178.5	178.6
500	408.25	235.7	134.1	139.2	136.2	221.2	222.2	221.6
600	489.9	282.8	166.8	170.2	168.2	264.5	264.9	264.9
700	571.55	329.9	188.7	193.6	190.5	308.6	309.2	309.7
800	653.2	373.1	220.1	225.7	223.2	351.4	351.9	352.6
900	734.85	424.2	241.7	246.5	244.1	398.4	399.2	398.7
950	775.6	471.4	278.1	283.5	282.7	430.6	431.2	430.8

Resistor Selection

It is important that R_s have low self inductance. Inductance in R_s will increase the peak voltage (E_1) and tend to defeat the purpose of the snubber. Low inductance is also desirable for R_s in an RCD snubber but is not as critical since the effect of a small amount of inductance is to slightly increase the reset time of C_s and reduce the peak current in the switch at turn-on. The normal choice for R_s is usually carbon composition or metal film. For higher power levels low inductance wire wound resistors, can be used with some care to verify the actual residual inductance and its effect on the snubber action. In this wire wound resistor $R_s = 10\ \Omega$ can be used. In this snubber design $I_o = 35$ A and $E_o = 1200$ V.As C_s is made larger the peak power and the switching loss will be lower. However, larger C_s means greater loss in R_s when the switch turns on and C_s is discharged through R_s and the switch. Depending on the size of C_s the switch voltage may reach E_o before, at the same time, or after the switch current reaches zero. The case where $E = E_o$ at the instant that I_0 is defined as a "normal" snubber.

where,

$$C_s = \frac{I_0 * t_s}{2 * E_0}$$

where t_s the fall time of the switch current is assumed as 10 μs. $C_s = (35 * 10 * 10^{(-6)})/(2 * 1200)$ $C_s = 1.5$ nF. Size of the snubber circuit depends upon the value of C_s. When a small snubber is used (C_s) the switching loss drops quickly. As C_s is made larger, switch losses are increases.

Phase locked loop (PLL) is the one which generate an output signal whose phase is related to the phase of the input "reference" signal. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. The signal from the phase detector is used to control the oscillator voltage. Keeping the input and output phase in lock step implies keeping the input and output frequencies in lock step.

PLL consists of three blocks as shown in Figure 11. They are phase detector, Low pass filter, Voltage Controlled Oscillator(VCO).The signal must be capacitively coupled to itself-basing amplifier at the signal input in case of smaller swings. Phase comparator-1 is an EXCLUSIVE-OR network. The signal and the comparator input frequencies must have 50% duty factor to obtain the maximum lock range. Phase to Output response characteristics are shown in Figure 12.

The average output voltage of the phase comparator is equal to ½ V_{DD} when there is no signal or the noise at the signal input.The average voltage to the VCO is supplied by the low-pass filter connected to the output of the phase-comparator 1. This also causes the VCO to oscillate at the centre frequency (f_o).

The frequency capture range(2 f_c) is defined as the frequency range of input signals on which the PLL will lock if it was initially out of lock. The frequency lock range (2 f_L) is defined as the frequency range of the input signals on which the loop will stay locked if it was initially in lock.

The capture range is smaller or equal to the lock range. With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal.

Block diagram of phase locked loop is shown in Figure 13. A typical behavior of this type of phase-comparator is that it may lock

Figure 11: PLL Block Diagram

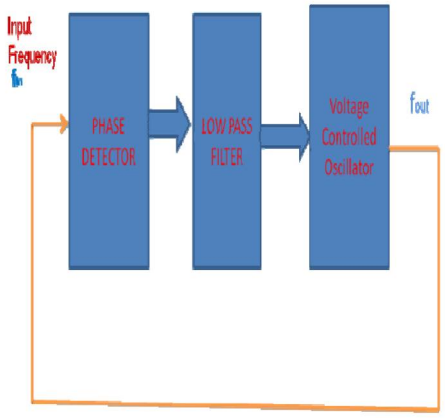


Figure 12: Phase to Output Response Characteristic

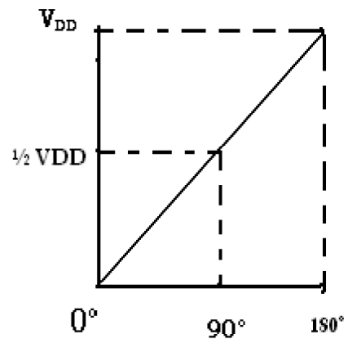
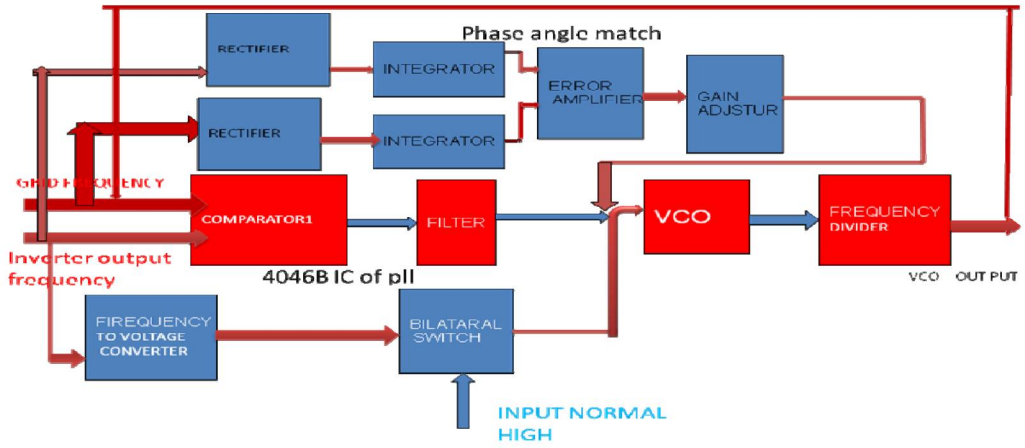


Figure 13: Block Diagram of Phase Locked Loop Control



on to input frequencies that are close to the harmonics of the VCO centre frequency. Another typical behavior is that the phase angle between the signal and the comparator input varies between 0^0 and 180^0 and is 90^0 at the centre frequency.

The VCO requires one external capacitor (C1) and one or two external resistors (R1 OR R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enable the VCO to have a frequency off-set is required. The high input impedance the VCO simplifies the design to low-pass filters, it permits the designer a wide choice of resistor/capacitor ranges. The VCO output (pin 4) can either be connected directly to the comparator input (pin 3) or via a frequency divider.. Low pass filter It controls the dynamic characteristics like lock range frequency and capture range frequency of PLL. It can attenuates the high frequency harmonics of comparator output The inverter and grid frequencies are synchronized and two wave forms are lock setup at 4046B PLL IC are shown in Figure 14.

PLLSupply Voltage V_{DD}=15 V

VCO input Voltage = $\frac{V_{DD}}{2} = \frac{15}{2} = 7.5V$

Conventional gain $K_p = \frac{V_{DD}}{\pi} = \frac{15}{\pi} = 4.7$

Center frequency of the PLL at R_1=10KΩ, C_1=390pf

f_{out}= 1.2/(4* 10000*390*10^{-12}) = 76.9 KHz

Lock range frequency

$$f_L = \frac{8 * f_{out}}{V} = 41.02\text{KHz}$$

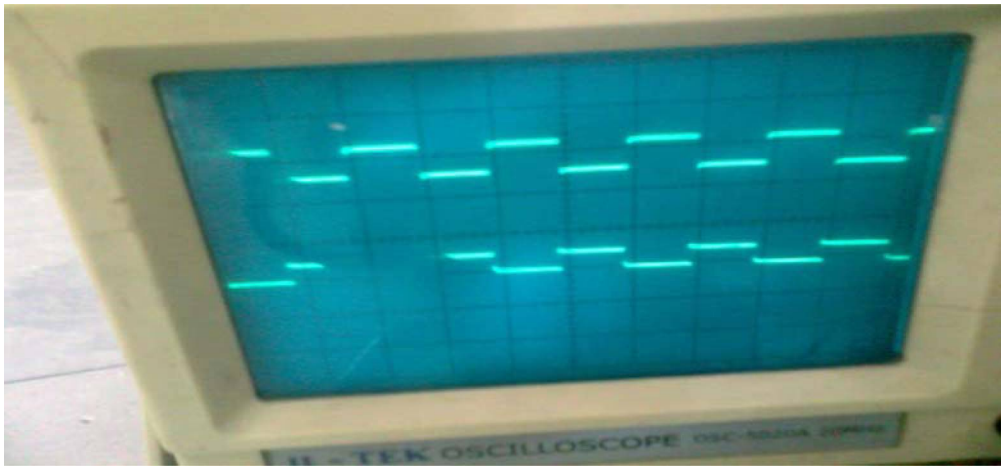
Capture range frequency

$$f_c = \pm\sqrt{\frac{1}{2\pi * C_1 * R_1}}$$

$$f_c = \pm\sqrt{[41025.6]/[2 * \pi * 10000 * 390 * 10^{-9}]}$$

$$= 40.9\text{KHz}$$

Figure 14: Synchronized PLL in Lock Setup at IC 4046B



LOW PASS FILTER

A low pass filer is a filter that passes low frequency signals but attenuates signals with frequencies higher than cut off frequency**.** This attenuates the higher order harmonics of the inverter output. This shunt component must be selected to produce low reactance at the switching frequency. But within the control frequency range, this element must present a high magnitude impedance.

The LC low pass filter is able to attenuate most lower order harmonics in the output voltage waveform. To minimize distortion, for linear or non linear loads, the inverter output impedance must be minimized. Therefore the capacitance should be maximized and the inductance minimized when specifying the cut-off frequency. This decreases the overall cost, weight, volume .But by increasing the capacitance, the inverter power rating will be increased due to the reactive power increase due to the filter [7].

The Dc links Voltage and switching frequency are constant. Inverter Dc link Voltage is 1200 V, SPWM switching frequency is 20 KHz. The inductor determines the ripple in the inductor current and reduces the low frequency harmonic components.

Assume that the output voltage V_{ga} varies slowly relatively to the switching frequency. Then the voltage across the inductor is:

$$V_L = V_{la} - V_{ga}$$

To determine the maximum inductor ripple current, thevalues of V_{la} and V_{ga} are as in equations and . The phase voltage duty cycle at maximum output is 75%.

$$V_{la} = (2/3) * V_{dc,}\ V_{ga} = (1/2) * V_{dc}$$

$$V_L = [(2/3) * V_{dc}] - [(1/2) * V_{dc}]$$

$$V_{la} = (2*1200)/3 = 800\ V$$

$$V_{ga} = (1/2) * 1200 = 600\ V$$

$$V_L = 800\text{-}600 = 200\ V$$

Assume $\Delta I_L = 1$ AAccording to the harmonic standard, 15-20% of the rated current is allowable, 20% is assumed. The ripple current depends on the DC link voltage, inductance, and the switching frequency.

The DC link voltage and switching frequency are constant, thus the inductance can be calculated from equation.

$$L = \frac{1}{8} * \frac{V_{DC}}{\Delta I_L F_S}$$

L=(1/8)* 1200/[1 * 20000] =7.5mH

where V_L = inductor voltage,

f_s = switching frequency,

V_{DC} = DC link voltage,

L = filter inductor

The high frequency components have to be eliminated from the inductor current when connected to the grid. This must be performed by the shunt impedance which is low at high frequencies. Capacitor selection is a tradeoff between inductor and capacitor reactive power. In a grid connected mode, the harmonic current injected into the grid network is the main issue. In the island connected mode, the DG unit is the source of power and voltage harmonics, which are the main concerns. The DG unit is connected to the grid through an isolation transformer. The inverter is considered a current source injecting currents into the grid. Assume that $V * I$ is the inverter output voltage, V_c is the capacitor voltage and I_o, I_{L1} are the inverter output current and inductor current, respectively.The inductor becomes active at the resonant frequency. The damping harmonic filter is chosen to reduce the effect of resonance on the system. If the C_d is maintained constant, with C_d = 10 μF.

$$L_d = \frac{1}{\omega_0^2 C_d}$$

$$f_0 = \frac{1}{2\pi} \frac{1}{\sqrt{(L * C)}}$$

$f_0 = 1/[2 * \pi * \sqrt{(7.5*10*10^{-6}]} f_{0=581.1}$ Hz

SIMULATION RESULTS

Simulation of the Hybrid Three Phase Grid-tied inverter system using MATLAB/SIMULINK is shown in below Figure 15.The various output waveforms of the Hybrid Three phase Grid-tied inverter system using MATLAB DC to DC boost converter output and inverter output shown in Figure 16, and Figure 17 respectively.

Figure 15: Simulink Diagram of Three Phase Grid Tied Inverter

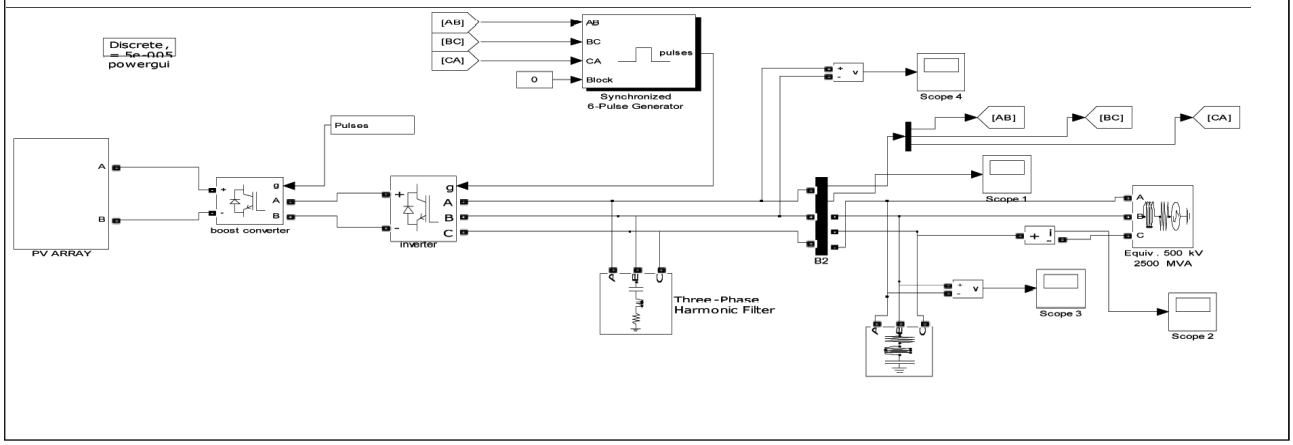


Figure 16: 400/950 V DC to DC Boost Converter Output

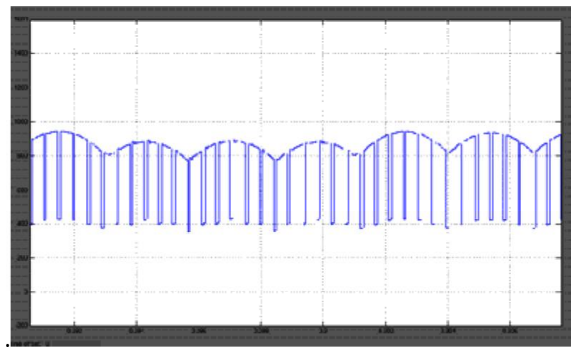
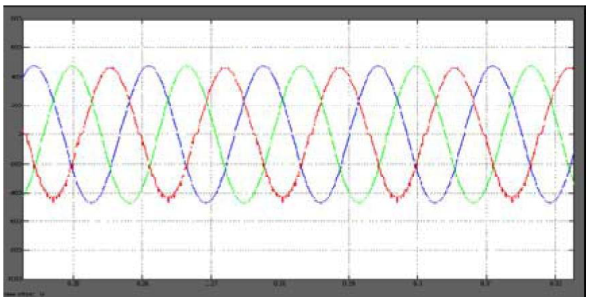


Figure 17: Three phase Inverter Output



CONCLUSION

A system with Three-phase grid-tied inverters with four-wire configuration has been proposed and developed for renewable energy applications. In addition, the proposed method can be utilized, not only to transfer power, but also help unevenly loaded phase conditions. Single-phase control method was expanded in a three-phase inverter by duplicating three individual phases with 120° apart. As the PLL topology is matched, the inverter has been successfully synchronized to the grid .Inverter provides a constant power to the utility grid according to three-phase grid voltage conditions. Inverters are capable of stopping delivery of power when the grid is in fault condition. Experimental results confirmed the mathematical design and simulation results.

FUTURE SCOPE

This prototype model developed in the Lab can be commercialized by performing reliability studies of the system. The system can be made more efficient by increasing the Inverter stages.

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