Broadband High-Efficiency Millimeter-Wave Power Amplifiers in 22-nm CMOS FD-SOI with Fixed and Adaptive Biasing

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***Abstract*—The design of broadband highly-efficient millimeter-wave (mm-Wave) Power Amplifiers (PA) in 22-nm CMOS FD-SOI (fully depleted silicon-on-insulator) is discussed. One design uses fixed biasing while the other utilizes an adaptive biasing network to improve its Power-Added-Efficiency (PAE) in power backoff. These designs aim to cover the key Fifth-Generation (5G) FR2 (Frequency Range 2) band (e.g., from 24.25 GHz to 43.5 GHz). In measurement, the PAs obtain very broadband 3-dB BW, ranging from 19.1 GHz to 46.5 GHz for the fixed-bias design and 18.8 GHz to 41.9 GHz for the adaptively biased design. The adaptively biased design is able to achieve enhanced output 1-dB compression point (OP_{1dB}) and PAE@P_{1dB} because of its adaptive biasing network. Measurements on the fixed-biased PA at 24/28/37/39 GHz yield max. PAE of 22.2/22.4/19.7/19.8%, and $P_{OUT,SAT}$ of 14.9/15.3/14.7/14.7 dBm, with OP_{1dB} of 11.8/11.6/12/11.6 dBm, and PAE@P_{1dB} of 14.1/13.4/14.5/13.5%. Measurements on the adaptively biased PA at 24/28/37/39 GHz yield max. PAE of 20.1/15.2/10.3/7.9%, and $P_{OUT,SAT}$ of 14.6/14.2/12.5/11.2 dBm, with improved OP_{1dB} of 13.1/12.3/12.1/11.2 dBm, and PAE@P_{1dB} of 19.1/14.4/10.3/7.9%. Data from body bias voltage V_B on the PA performance is also presented. These measurement results are compared with post-layout parasitic-extraction (PEX) simulations, and also against other novel silicon broadband mm-Wave PAs in literature.**

***Index Terms*—5G, Adaptive biasing, broadband Power Amplifier (PA), CMOS SOI, FR2, millimeter-wave (mm-wave), power backoff**

I. Introduction

With 6G (sixth-generation) mobile technologies now under development, and 5G (fifth-generation) rolling out worldwide taking the place of 4G, there is a very strong demand for highly power-efficient broadband radio-frequency (RF) and millimeter-wave (mm-Wave) circuits and systems for both commercial and DoD (Department of Defense) applications. In particular, frequencies in the commercial 5G FR2 (Frequency Range 2) band (24.25-52.6 GHz) can help deliver data rates of greater than 10 Gb/s for enhanced mobile broadband (eMBB) and sub-1mS delay time for UR/LL (ultra-reliable, low-latency) for 5G applications [1]. One major technical challenge in these low-power broadband RF systems is the design of the mm-Wave PAs, as it is often the most power-hungry part of a RF/mm-Wave Front-End Module (FEM) within a phased array system. Making these PAs efficient is extremely important to the success of mm-Wave technologies because there will be higher path-loss and may require additional phased array channels that utilize Multiple Input, Multiple Output (MIMO) antennas. If the PAs are inefficient, excessive amounts of heat could be produced and reliability issues may also arise. Additionally, very broadband PAs can enable large BW (bandwidth) operation to cover the key FR2 band (~20 GHz), which can be attractive for other potential applications. For example, these broadband PAs would enable considerably fewer RF FEMs in phased arrays, drastically reducing the system cost and form factor, especially if they can be made to be reconfigurable [2].

II. PA Design Considerations

All PAs use the identical one-stage differential cascode core design with ESD-protection (electrostatic discharge) as can be seen in Fig. 1 to Fig. 3. Since a Common-Gate (CG) amplifier is intrinsically more broadband than a Common-Source (CS) amplifier, we expect the cascode topology may be more broadband than a stacked-FET (field effect transistor) topology where two common-source amplifiers are in cascade for the same output matching [3]. Instead of a classic cascode topology where the gate node of the CG FET has a large capacitance to ground to provide excellent RF ground, a smaller gate capacitor is used in our design (~ 427 fF), making this more of a quasi-cascode PA design to provide the optimal broadband performance on output power and PAE (power added efficiency). RC feedback is used to stabilize the PA and increase the BW [4], and neutralization capacitors are used to cancel out the Miller capacitance (i.e., C_{GD}), increasing the maximum stable gain and improving reverse isolation [5]. The output matching network was designed using load-pull simulations and has an integrated on-chip balun, and a 1st

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order input matching network was used at the input. Our differential PA's output is combined with an on-chip balun for improved broadband matching at mm-Wave for medium-power applications. However, for high power applications, a Wilkinson combiner could be used combine two single-stage RF amplifiers in parallel to achieve good output power and isolation between the two parallel PAs, as demonstrated in [6] for L-band operation.

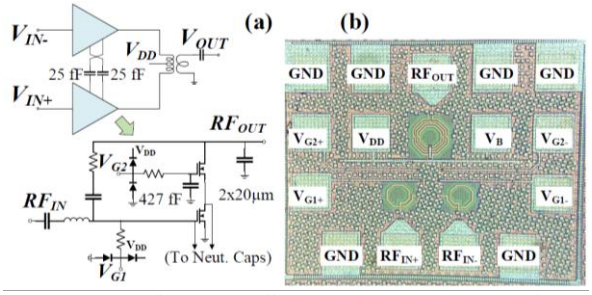

Fig. 1. For the fix-biased differential CMOS PA: (a) simplified schematic; (b) die micrograph.

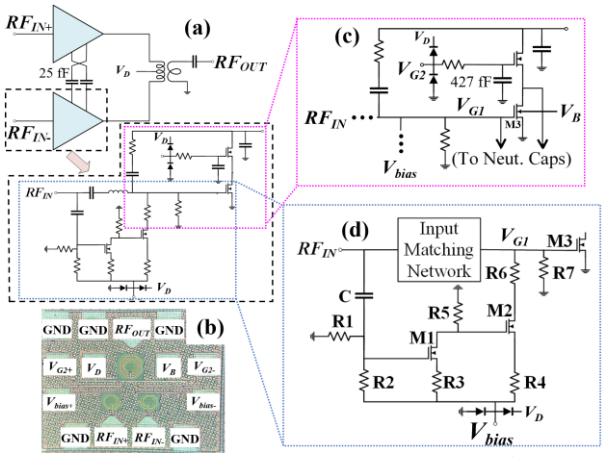

Fig. 2. For the adaptively biased CMOS PA: (a) a simplified circuit schematic; (b) the die micrograph; (c) a close-up schematic of the quasi-cascode PA; and (d) a close-up schematic of the adaptive biasing network of the PA.

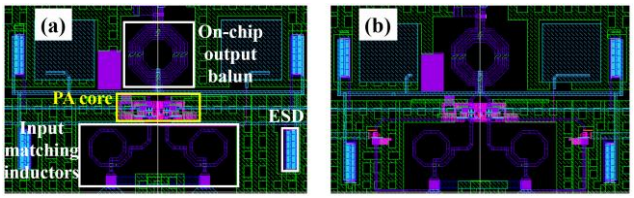

Fig. 3. Layouts of the (a) fixed-biased PA and (b) the adaptively biased PA.

The adaptive biasing network shown in Fig. 2 (c) should improve the PA's PAE at power backoff, which can be characterized at its P_{1dB}, and thus improving the PA's "linear PAE". Transistors M1 and M2 are designed to operate in the sub-threshold region (i.e., $V_{GS} < V_t$) to allow an exponential increase in the drain current (I_D) when a positive change in voltage occurs at their gates, and to minimize the amount of bias current consumed by the adaptive biasing network [7]. Using transistors biased in the sub-threshold region for adaptive-biased mm-Wave PAs was not attempted in [8]-[12]; it was common to see these transistors biased in the triode region instead. The biasing on the gate of transistor M1 is determined by the resistors R1 and R2 and P_{IN}. As P_{IN} increases, there is larger average current seen at the drain of M1, causing larger voltage drops to be seen over R3 and R5, and thus increasing the gate voltage at M2. This in turn increases the current through M2 and the voltage drops increase over the resistors R4, R6 and R7. The result of this is that as P_{IN} increases, we see an increase to the gate voltage of the CS device M3 (V_{G1}) in the quasi-cascode PA circuit. Two stages were used in the adaptive biasing network because more power was needed to drive the current required to produce the desired voltages at the gate of M3 to drive the PA. The main concerns of PA design are higher linearity, efficiency, bandwidth, lower manufacturing cost, etc., as discussed in [13]. Our PA is designed to operate closer to Class A mode when P_{IN} is high, and more in the Class B region when P_{IN} is low; and this is why we expect to see an improvement in its efficiency at power backoff.

III. Simulation and Measurement Results

The 22-nm FD-SOI CMOS technology used to design the PAs presented in this paper is provided by Global Foundries (GF), and it has very good cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) [14]. We have obtained f_T and f_{max} in simulations after post-layout parasitics between all metal layers were extracted using Mentor Graphic's Calibre R+C+CC xACT [15], and the results are plotted in Fig. 4. Here 2×20-µm wide and 22-nm long super low threshold voltage (V_t) n-FET (SLVTNFET) devices are used because of their superior RF performance, achieving simulated peak f_T of ~350 GHz and peak f_{max} of ~260 GHz.

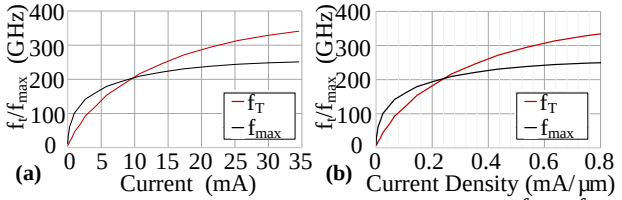

Fig. 4. Post-layout parasitic-extracted (PEX) simulation of f_T and f_{max} versus (a) current and (b) current density of a 2×20-µm×22-nm NMOS FD-SOI device.

All PEX simulations shown in this paper were performed using Mentor Graphic's Calibre R+C+CC xACT extraction, which has shown to be reasonably accurate when compared with EM (electromagentic) simulations from our measurement data, and it is much faster to obtain simulation results so we are presenting PEX simulations here.

The adaptive PA operates in a deep Class A/B mode around its threshold V_t when V_{G1} = 0.3 V, which happens when V_{BIAS} is set to 1.3 V (cf. Fig. 5 (b)); and in the Class A mode around V_{G1} = 0.5 V, when V_{BIAS} is set to 1.7 V. Since the V_{G1} node is internal on-chip and thus cannot be directly measured, the relationship between V_{BIAS} and V_{G1} found in simulation was used to represent measured V_{BIAS} as V_{G1}. As the RF continuous-wave (CW) signal power P_{IN} increases, V_{G1} increases in the ranges depicted on the measured *I-V* curve in Fig. 5 (d) for a given V_{BIAS}: i.e., when V_{BIAS} is set to 1.4 V and P_{IN} increases from –14 dBm to 2 dBm, V_{G1} increases from ~ 0.36 V to 0.65 V.

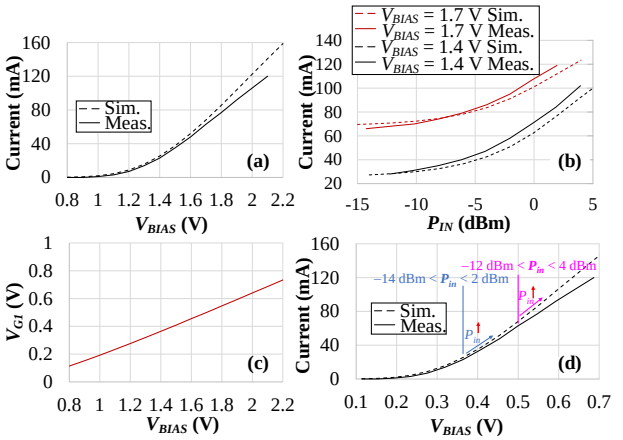

Fig. 5. (a) PEX simulated and measured *I-V* curves vs. changing V_{BIAS} on the adaptive-biased PA (Fig. 3) with no RF input, (b) PEX simulated and measured current consumption of the adaptively biased PA with RF input at 37 GHz, (c) PEX simulated relationship between V_{BIAS} and V_{G1} at the gate of M3, without RF input, and (d) the effects of adaptive biasing on the PA. I_D vs. V_{G1}, and when the RF CW P_{IN} to the PA at 37 GHz increases, I_D and V_{G1} increase along the *I-V* curve as shown (V_D = 1.8 V, V_{G2} = 1.4 V, V_B = 0 V).

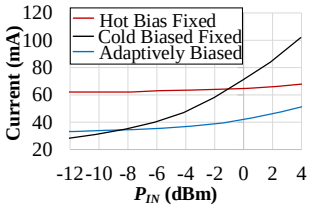

Fig. 6. Comparison of measured drain currents of the adaptively biased PA (V_{BIAS} = 1.4 V) and the "hot" and "cold" fix-biased PAs (i.e., V_{G1} = 0.5 and 0.4 V, respectively). RF CW P_{IN} at 37 GHz with V_D = 1.8 V, V_{G2} = 1.4 V, V_B = 0 V.

In Fig. 6, the current consumption of the adaptively biased PA is plotted along with that of the fix-biased PA. The fix-biased PA was biased at V_{G1} = 0.4 V and 0.5 V, corresponding with the cold and hot biasing curves shown, respectively. It is clear to see that the adaptively biased PA can operate with lower current consumption than the "hot-biased" PA at 6 dB to 12 dB power backoff, and thus increasing its efficiency at backoff, while also improves linearity-efficiency trade-off at various P_{IN} vs. fix-biased PAs.

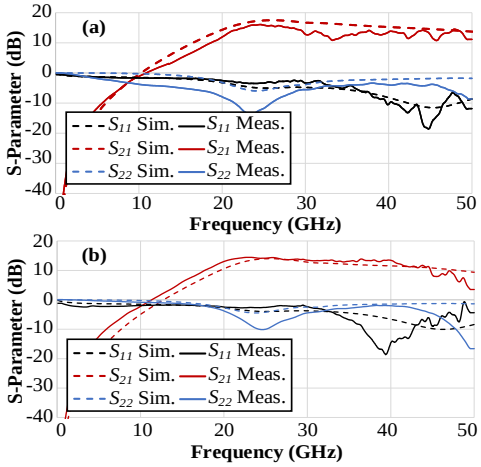

Fig. 7. Measured and PEX simulated S-Parameters of the (a) fix-biased PA with V_{G1} = 0.5 V, and (b) the adaptively biased PA with V_{BIAS} = 1.4 V (i.e., V_{G1} = 0.36 V); both at V_{G2} = 1.4 V, V_D = 1.8 V, and V_B = 0 V.

The S-parameter data in Fig. 7 shows reasonable agreement between PEX simulations and measurements. At these biased conditions, the fix-biased PA achieves max. S_{21} of 17.1 dB and 3-dB BW from 19.1 GHz to 46.5 GHz, while the adaptively biased PA achieves max. S_{21} of 13.4 dB and 3-dB BW from 18.8 GHz to 41.9 GHz.

After taking PA measurement data with no RF input, PEX simulations were re-run to find the DC bias levels that produce the same measured DC drain currents without RF input to make a fair comparison of measured vs. simulation PA large-signal data. The PA's DC current consumption, shown in Fig. 8, also reveals that as P_{IN} and frequency increase, the difference between the simulated and measured data increases.

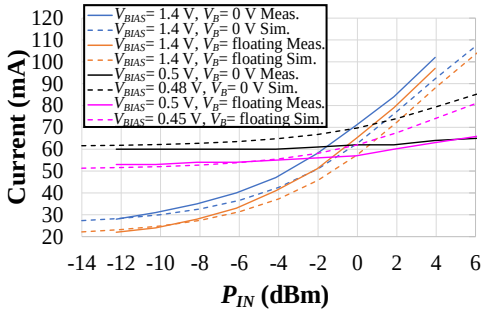

Fig. 8. Measured and PEX simulated currents of the fixed and adaptively biased PAs with V_D = 1.8 V and V_{G2} = 1.4 V and RF CW P_{IN} inputted to the PA at 37 GHz

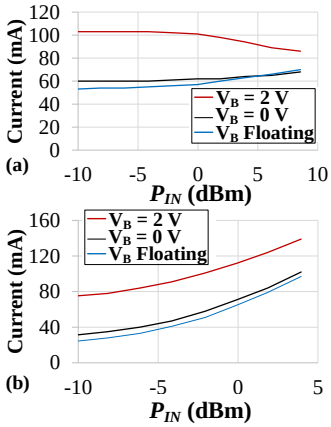

Fig. 9. Current consumption dependence on the body bias V_B at 0, 2V, and floating for the (a) fix-biased PA with V_{G1} = 0.5 V and (b) the adaptively biased PA with V_{BIAS} = 1.4 V (V_D = 1.8 V, V_{G2} = 1.4 V RF CW P_{IN} at 37 GHz).

The current consumption of both the fixed and adaptively biased designs were measured when the FETs' body node's biasing V_B was connected to ground, 2 V, or left floating, as shown in Fig. 9. Note there is an observable drop in current consumption when the body is left floating (likely due to higher V_t), so the large signal data was also measured under each of these body biasing conditions to be shown next. The body biasing can be changed to affect the PA's operational mode; if V_B were increased to 2 V, its V_t would drop by around 160 mV, causing the PA to behave more as a Class A amplifier [16]. The body biasing was only altered on the CS FET in the cascode topology, all other devices' V_B nodes were connected to the chip's ground.

Measured large signal PA data shown in Fig. 10 to Fig. 13 are consistently indicating some degradation in the measured gain vs. those in the PEX simulations (~< 2 dB). This might be due to the loss of the RF probes since we did not calibrate their loss out with our current set-up. Our probe manufacturer indicated that the probes could have ~1 dB of loss each, so that would match up reasonably well with the 0 dB to 2 dB loss seen here. Also, the PAs seem to compress a little earlier in measurement than in simulation.

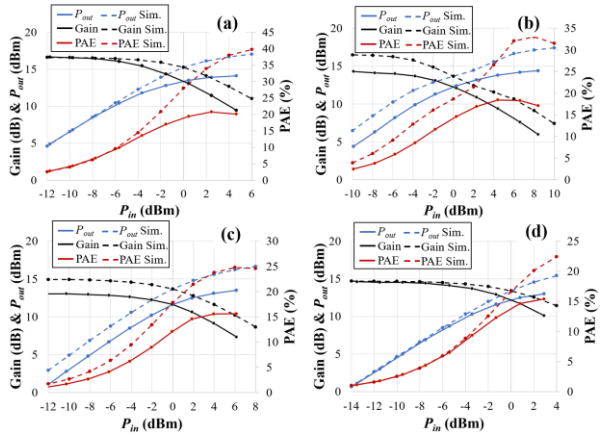

Fig. 10. Large signal measurements and PEX simulations of the fix-biased PA at 24, 28, 37, and 39 GHz ((a) to (d)) with V_{G1} = 0.5 V (0.48 V in sim.), V_{G2} = 1.4 V, V_D = 1.8 V, and V_B = 0 V.

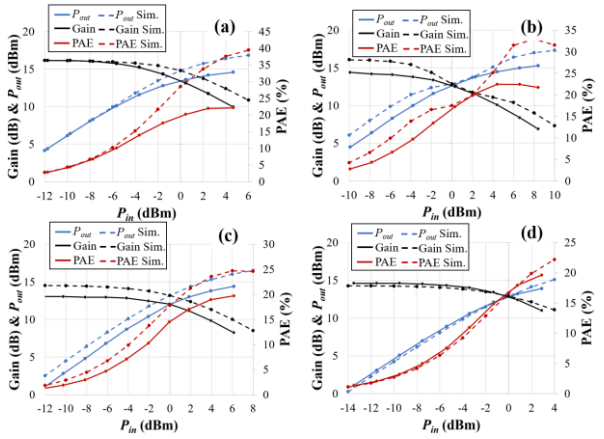

Fig. 11. Large signal measurements and PEX simulations of the fix-biased PA at 24, 28, 37, and 39 GHz ((a) to (d)) with V_{G1} = 0.5 V (0.45 V in sim.), V_{G2} = 1.4 V, V_D = 1.8 V, and V_B floating.

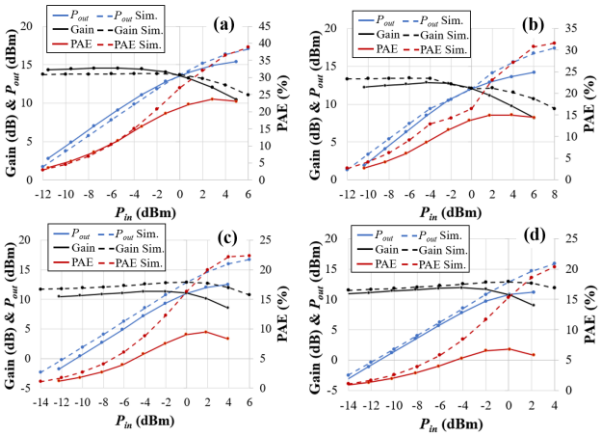

Fig. 12. Large signal measurements and PEX simulations of the adaptively biased PA at 24, 28, 37, and 39 GHz ((a) to (d)) with V_{BIAS} = 1.4 V (1.35 V in sim.), V_{G2} = 1.4 V, V_D = 1.8 V, and V_B = 0 V.

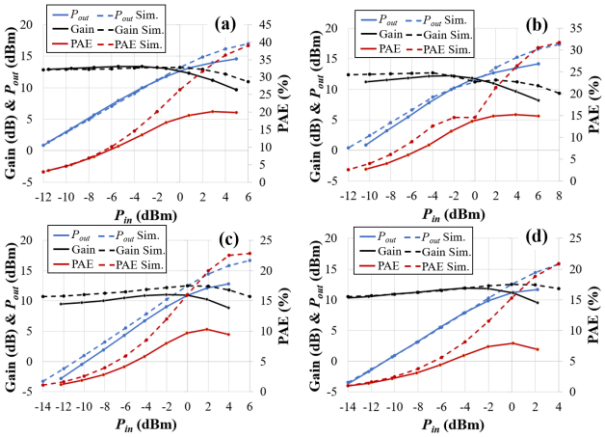

Fig. 13. Large signal measurements and PEX simulations of the adaptively biased PA at 24, 28, 37, and 39 GHz ((a) to (d)) with V_{BIAS} = 1.4 V (1.35 V in sim.), V_{G2} = 1.4 V, V_D = 1.8 V, and V_B floating.

From the results shown in Fig. 11, where V_B is left floating, the large signal performance $P_{OUT,SAT}$ of the fixed biased PAs is found to be slightly better than those in Fig. 10, where V_B is tied to ground (by 0.6 dB to 1.4 dB). This might be due to the floating body diode cannot be turned on during large transients, and/or V_B affected the PA output matching, etc. It is important to note that for the adaptively biased PA, the measured max. PAE are consistently very close to its PAE@P_{1dB}, within ~2% of across the entire 24 GHz to 39 GHz BW, suggesting the adaptive biasing effectively enhancing PAE at power backoff. However, more linearity and PAE data will be collected using 5G NR modulated signal and presented later. The measured data collected on each PA with their bodies grounded or left floating (NC) for the CS FET only is shown in Table I. Having the body of the CS FET floating causes its V_t to drop slightly compared to when it is grounded, meaning that it is essentially biased "colder", or that it is operating more as a Class A/B amplifier than a Class A amplifier. Thus, we expect to see a drop in the gain and $P_{OUT,SAT}$ and an improvement to its PAE when the body is floating. Since we see some improvement in the $P_{OUT,SAT}$ when the FET's body is floating for the fix-biased PA but not the adaptive-biased one, we suspect the change to the body biasing is causing the interstage matching of the PA to be better matched for power in one case but not the other, as the CS FETs are biased under two different gate overdrive conditions.

IV. Conclusion

A fix-biased and an adaptively biased broadband mm-Wave CMOS PA have been designed, measured, and reported in this paper. The adaptive biasing network allows the PA to operate in Class AB mode when the output power is backed off from its peak, and in Class A mode at high P_{OUT}, allowing for more efficient operation for PAE@P_{1dB}. The PAs obtained very broadband 3-dB BW, ranging from 19.1 GHz to 46.5 GHz for the fix-biased design and 18.8 GHz to 41.9 GHz for the adaptively biased design in measurement. When compared with other works in literature as summarized in Table II, both PAs achieved the highest 3-dB BW while also with very small die sizes. Comparing the fixed-bias

vs. the adaptively biased PAs, the adaptively biased PA was able to achieve higher PAE@P_{1dB} and OP_{1dB} at the lower frequencies of 24 GHz to 28 GHz where the $P_{OUT,SAT}$ was not degraded as in the case at above 37 GHz, suggesting the adaptive biasing is working effectively at least at 24 GHz to 28 GHz in improving PA linearity. More measured linearity and PAE data using broadband mm-Wave 5G NR modulated waveforms is needed to verify the PAs' expected attractiveness for broadband highly-efficient mm-Wave applications.

TABLE I: COMPARISON BETWEEN CW MEASURED DATA OF OUR FIXED AND ADAPTIVELY BIASED 22NM CMOS-SOI PAS

Measurement data	Biasing voltage V_{BIAS}/V_{G1} (V)	Body voltage V_B (V)	Supply voltage V_D (V)	Freq. (GHz)	$P_{OUT,SAT}$ (dBm)	OP_{1dB} (dBm)	Peak PAE (%)	PAE@ P_{1dB} (%)	Gain (dB)
Fixed-biased PA	0.5	0	1.8	24	14.3	11.3	**20.8**	12.4	15.9
				28	14.4	10.8	**18.4**	10.6	15.1
				37	13.6	10.6	**15.6**	9.7	13.5
				39	13.3	10.4	**15.4**	9.5	12.6
Fixed-biased PA	0.5	0, NC on CS FET only	1.8	24	14.9	11.8	**22.2**	14.1	16.3
				28	15.3	11.6	**22.4**	13.4	15.7
				37	14.7	12	**19.7**	14.5	14.9
				39	14.7	11.6	**19.8**	13.5	13.8
Adaptively biased PA	1.4	0	1.8	24	15.7	**13.6**	**23.7**	**22**	14.2
				28	14.2	**12.2**	**15**	**14.1**	13.7
				37	12.5	**11.8**	**9.5**	**9.3**	13.4
				39	11.2	**10.6**	**6.8**	**6.6**	13.3
Adaptively biased PA	1.4	0, NC on CS FET only	1.8	24	14.6	**13.1**	**20.1**	**19.1**	13.2
				28	14.2	**12.3**	**15.2**	**14.4**	12.7
				37	12.5	**12.1**	**10.3**	**10.3**	12.3
				39	11.2	**11.2**	**7.9**	**7.9**	12.3

TABLE II: COMPARISON OF MEASUREMENTS WITH RECENT STATE-OF-THE-ART MM-WAVE CMOS PA DESIGNS IN LITERATURE

Ref.	Tech.	Design	Supply voltage (V)	3-dB BW (GHz)	Freq. (GHz)	$P_{OUT,SAT}$ (dBm)	OP_{1dB} (dBm)	Peak PAE (%)	PAE@ P_{1dB} (%)	Gain (dB)	Core size (mm^2)
[10]	90-nm CMOS	2-stage cascode w/ adaptive bias	2.4	Narrow band	21	20.4	18.5	17.3	13.3	26.9	0.5*
[11]	0.13-μm CMOS	2-stage w/ adaptive bias	1.2	Narrow band	24	16.0	13.3	17.7	15.6	15.6	0.36*
		2-stage w/ fixed-bias				15.2	12.1	18.5	11.7	17.2	
[12]	65-nm CMOS	Cascode w/ adaptive bias and dynamic feedback	2	24.25–27.5 (12.6%)	24.25	N/A	18.7	37.2	30*	15.3	0.19
[17]	90-nm CMOS	3-stage w/ adaptive bias and combing linearizer	1.2	Narrow band	28	17.7	16.7	23.6	21.4	21.3	0.49
[18]	28-nm CMOS	Stacked PA w/ new adaptive bias method	2	18–37.5 (70%)	24	16.8	15.6	41	36.5	10	0.11
[19]	65-nm CMOS	Multi-port load-pulling fixed-bias	1.1	26–42 (47.1%)	28	19	19	21	21.0*	15	1.35
					37	19.6	16	21.9	21.9*	16	
					39	19.2	18.1	21.7	21*	16	
[20]	130-nm SiGe	2-stage Doherty fixed-bias	1.5	23.3–39.7 (52.1%)	28	16.8	15.2	20.3	19.5	18.7	1.76
					37	17.1	15.5	22.6	21.6	18	
					39	17.0	15.4	21.4	20.7	15.6	
[21]	45-nm SOI CMOS	Continuous Hybrid Class F/F^{-1}; fixed-bias	2	25.9–43.7 (51.1%)	28	18.6	16.6	45.7	42*	11.4	0.14
					37	18.6	16.3	40.2	35*	10.7	
					39	18.5	16.3	41.2	35*	10.5	
[22]	22-nm FD-SOI	Differential quasi-cascode; fix-biased; Die #1; $V_B = 0$	1.8	**19.1–46.5 (83.5%)**	24	14.6	11.5	**26.1**	17.9	15.7	0.07
					28	14	9.2	**19.9**	11.1	14.5	
					37	13.6	9.5	**18.5**	12.2	15.4	
					39	12.9	9.6	**15.2**	11.6	14.7	
This work	22-nm FD-SOI	Differential quasi-cascode; fix-biased; Die #2; $V_B = 0$	1.8	**19.2–44.8 (80%)**	24	14.3	11.3	**20.8**	12.4	15.9	0.07
					28	14.4	10.8	**18.4**	10.6	15.1	
					37	13.6	10.6	**15.6**	9.7	13.5	
					39	13.3	10.4	**15.4**	9.5	12.6	
This work	22-nm FD-SOI	Differential quasi-cascode; adaptive bias; $V_B = 0$	1.8	18.8–41.9 (76.1%)	24	15.7	**13.6**	**23.7**	**22**	14.2	0.11
					28	14.2	**12.2**	**15**	**14.1**	13.7	
					37	12.5	**11.8**	**9.5**	**9.3**	13.4	
					39	11.2	**10.6**	**6.8**	**6.6**	13.3	

*Estimated from figures

CONFLICT OF INTEREST

The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

AUTHOR CONTRIBUTIONS

J. Mayeda and D. Lie conceptualized the work; J. Mayeda designed the PAs; J. Mayeda and C. Sweeney conducted the testing; J. Mayeda, C. Sweeney and D. Lie analyzed the data; C. Sweeney wrote the paper; J. Mayeda, C. Sweeney, D. Lie and J. Lopez reviewed and edited the paper; D. Lie and J. Lopez gathered resources; all authors had approved the final version.

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