Studies on Phase Noise Profiles of Proportional-Integral-Derivative Controlled PLL

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***Abstract*—Phase noise in a phase-locked loop is originated from reference oscillator, phase detector, loop filter, voltage controlled oscillator and frequency divider which make the system unstable by generating high phase noise at the output spectrum. In this work, a mathematical linear phase noise model is therefore developed to investigate the effect of reference noise, phase detector noise, voltage controlled oscillator noise, frequency divider noise and specifically the loop filter noise. For this purpose, the conventional active or passive low pass filter of the phase locked loop is replaced by a proportional-integral-derivative controller during acquisition. The noise problem of each component is formulated as a transfer function derived from linear analysis of the proposed mathematical noise model. The simulation results show that the effect of noise attenuation of voltage controlled oscillator is -40dB/decade while the noise attenuation of the reference noise, phase detector noise, proportional integral derivative controller noise and frequency divider noise are approximately –20dB/decade each. The 6.21GHz proposed proportional-integral-derivative controlled phase-locked loop is also highly stable with fast switching speed of 0.238nS at damping factor of 0.625 and phase margin of 92° for minimum phase noise.**

***Index Terms*—Phase noise, Noise attenuation, noise characteristics, noise transfer function, PID controlled PLL, lock time**

I. Introduction

Starting from computing to communication, Phase-Locked Loop (PLL) systems are significantly used in many modern electronics and telecommunication applications. A PLL is a feedback control system which is a combination of Phase Detector (PD), Loop Filter (LF), Voltage Control Oscillator (VCO) and Frequency Divider (FD) so connected that the oscillator maintains a constant phase angle relative to a reference signal [1]-[4]. A PD compares the phase difference between the input frequency and the output feedback frequency and provides a DC voltage which is passed on to a LF. The high frequency components are filtered out by the LF. The VCO is adjusted by the loop until the phase difference between the reference signal and the divider output is constant. PLL performance is decided by its various parameters such as Phase Noise (PN), lock range, Lock Time (LT), capture range, loop bandwidth (BW) etc. Each parameter has its importance depending upon various applications but two of the most important parameters are PN and LT. PN decides the stability of the system while LT [5]-[9] is important from data security point of view. PN is the frequency domain representation of rapid, short term fluctuations in the phase caused by time domain instabilities i.e. jitter [10]-[15]. LT is the frequency lock time of a PLL and the time spent in locking reduces the effectiveness of data rate achievement. To design a PLL with low PN and faster LT is very difficult as both PN and LT of a PLL have various tradeoffs amongst themselves and the other parameters. PN issues are more significant in high frequency usage, as PN of a PLL oscillator for a given frequency generally increases proportionately to the frequency of the carrier [3], [6], [16]. This underlines the importance of PN characteristics study as the same affects the performance of a PLL system. V. Kroupa [1] investigated major additive noise sources in PLL systems and how these noises added up to the reference noise. Major guideline rules were discussed for reducing the additive noises in complicated PLL systems or Frequency Synthesizers (FS).

Many literatures available which provide valuable insights in optimizing PN and LT characteristics were reviewed. Mehrotra [10] presented a technique for noise analysis wherein the noise problem was considered a stochastic differential equation and methods to obtain asymptotic solution for the equation were discussed. He derived the equations using a nonlinear analysis of the VCO in feedback loop instead of using traditional linear or PN analysis of open loop oscillators. He concluded that without using the more expensive transient simulation of entire PLL, the PLL output spectrum can be computed using only the analysis of the basic components of a PLL system. The drawback as identified by the author is that only white noise sources can be handled by the proposed model.

Osmany *et al.* [13] presented an analytical PN model for fractional-N PLLs emphasizing on GHz range integrated Radio Frequency (RF) synthesizers. Nyquist equation generalization was used to describe filter noise which contributes to the overall noise to a great extent. It was concluded that the rms phase jitters can be reduced to a great extent by correction in phase error by processing digital baseband in Orthogonal Frequency-Division Multiplexing (OFDM) systems when the carrier spacing is greater than the loop BW.

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Ryu and Lee [17] designed a digital hybrid PLL (DH-PLL) considering the input reference noise, VCO noise and digital-to-analog (D/A) converter noise. The PN output was more than a conventional PLL due to addition of D/A converter noise and hence various mathematical models of the considered noises were derived and analyzed to minimize the output PN and the same were compared with practical devices. The model achieved a boundary line PN of around −120dBc/Hz at a switching speed of around 0.3 ms in a closed loop BW of 1-3 kHz.

Yin *et al*. [18] designed and simulated a 24GHz PLL frequency source model and analyzed the TF characteristics of every noise source. The author concluded that the low PN can also be achieved from a high frequency single PLL circuit without using a Direct Digital Synthesizer (DDS) or its combination.

L. Jia *et al*. [19] presented an approach of deriving the noise Transfer Functions (TF) of the input, the LF and the VCO in z-domain rather than s-domain using 3rd order LF for noise distribution in the PLL synthesizer. Through the simulation of the behavioural model it was also found that the LF is unable to reject a noise peak that exists when the loop BW is similar to the reference frequency however a stability limit of the wide loop BW FS had been analyzed and extracted from the model.

Limkumnerd and Eungdamrong [20] studied the role of LF in PN. The authors compared the 2nd order passive and active Low Pass Filters (LPF) and concluded that the passive LPF is more efficient at low offset frequency for a PLL.

Amornchai *et al*. [21] used a regenerative divider in the feedback loop of a PLL instead of the main divider to improve the PN of a PLL. The simulation of the model was carried out in MATLAB to predict the output PN by calculating the relation between input power spectral density (PSD) & TF. However, for the proposed system PN increases with increase in frequency.

Kalita and Bezboruah [22] described an analytical PN model of PLL-FS by deriving noise TFs in s-domain and provided a detailed analysis on modeling and simulations in MATLAB. Two different LFs, active lag-lead filter (ALLF) and Standard Feedback Approach (SFA) were used for noise simulation and concluded that noise peak exist with the ALLF in the loop whereas the system with SFA in the loop does not show any peak. However, in low pass responses, peaks showed up.

Chen *et al*. [23] designed the current steering charge pump and the output differential buffer unit to stabilize the VCO output waveform for reducing the PN of PLL based on the 0.13μm Complementary Metal-Oxide Semiconductor (CMOS) 1P4M technology with 1.5V supply voltage. The designed PLL with the analog signal to digital wave converted optimized VCO improves the LT to 1.8μs and achieves a PN of −146dB/Hz at 1GHz.

Peng *et al*. [24] developed a low noise 2.4GHz fractional-N FS with a 17ns Self-Injection Locking (SIL) loop which reduces the PN of the Injection-Locked Oscillator (ILO) along with the reduction in quantization noise of the delta–sigma modulator and the PN of the reference signal. The developed synthesizer displayed good noise reduction at offset frequencies in the range of MHz along with fast switching time of 39 μs.

From the various literature reviewed it can be seen that a detailed analysis and simulation of noise contributions of each noise source to the output spectrum of a PLL is necessary to reduce PN. Though low PN is achieved through the various analysis or models discussed in literature, but it is seen that usage of passive or active LFs limits the achievement of faster LT. The major scope of this paper is to develop a linear PN mathematical model with low LT using a Proportional-Integral-Derivative (PID) controller as a LF instead of the conventional active or passive LPF. The noise TFs of the reference, the PD, the PID controller, the VCO and the FD derived from the model are analyzed and simulated in MATLAB to obtain the desired output.

II. Phase Noise Model

Designing a low noise and fast LT PLL with stable LF is very challenging as the dynamic characteristics of the whole circuit is controlled by the LF. In PLL, LF removes the high frequency components as well as the high frequency noise generated from the PD. Therefore, in the proposed mathematical model, a PID controller is used replacing a conventional LF. A PID controller is a widely used control loop feedback system in industrial applications that is a combinations of three individual controller like proportional (P), integral (I) and derivative (D) controller. It responds faster and more accurately than conventional fuzzy logic controllers by calculating an error response based on the current error (P term), the past error (D term) and the rate of the error change (I term). The proportional controller with the proportional gain K_P reduces the Rise Time (RT). The integral controller with integral gain K_I guarantees that the Steady-State Error (SSE) is zero, i.e., the desired output of the controlled system is equal to the input in steady-state. The derivative controller with derivative gain K_D reduces the system overshoot (OS) and LT [25], [26]. The combination of these three controllers can provide very stable and accurate results. Due to these properties, the PID controller works as an efficient filter in PLL which not only makes the system more stable but also reduces noise levels with faster LT. Though having useful properties, the derivative term of PID controller amplifies noise. But the elimination of derivative controller is not practical as even a little change in the proportional gain constant can make the system unstable [27]-[32]. Therefore, the proper tuning of derivative controller is important during simulation to control the PN.

The TF of the PID controller is given by:

$$F_{PID}(s) = K_P + \frac{K_I}{s} + sK_D \tag{1}$$

By adjusting the weighting proportional, integral and derivative constants, K_P, K_I and K_D in (1), the PID controller filter can be set to give the desired performance of the proposed system.

Each component of a PLL generates some noise leading to the total PN of the proposed circuit. In this paper we will be investigating the roles of each source in PN contribution through mathematical models and

simulations. The various noise sources which can be added to the system are denoted as Θ_{REF}, Θ_{PD}, Θ_{PID}, Θ_{VCO} and Θ_{FD} for reference, PD, PID controller, VCO and FD respectively. PLL TFs can be derived by the classical control loop theory. $G(s)$ is the open Loop Gain (LG) and is defined as the gain from the input of the PD to the output of the PLL. The open LG is comprised of the PD gain constant, K_d; the PID controller TF, $F_{PID}(s)$ and the VCO input voltage to phase relationship K_0/s, where, s is a complex frequency. The feedback path is $1/N$ (N being the division ratio of FD) which we will now simply refer to as H, to align with standard control theory notation for feedback.

$$G(s) = K_d F_{PID}(s) \frac{K_0}{s} \tag{2}$$

$$H(s) = H = \frac{1}{N} \tag{3}$$

To derive the noise TF, a summation block at each point of interest has been inserted and solved for the ratio of the output noise to the input noise in a closed loop condition as shown in Fig. 1.

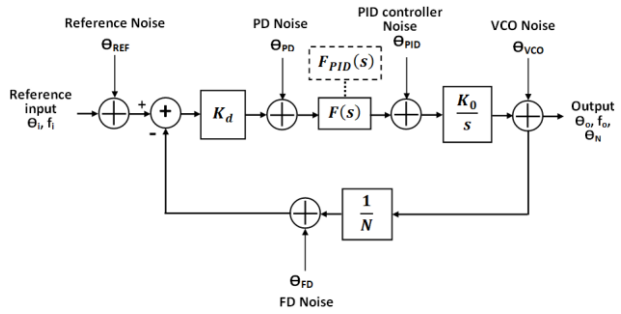

Fig. 1. Mathematical PN model of the proposed system.

A. Reference Noise

The reference noise appears at the input of PD and is amplified by the division factor N. Even if the PN characteristic of the reference is typically lower in magnitude than PN characteristics of VCO, by tuning N we can compare both the PN characteristics. The TF for the reference noise is:

$$T_{REF}(s) = \frac{\theta_o(s)}{\theta_{REF}(s)} = \frac{G(s)}{1 + G(s).H} \tag{4}$$

The required reference noise TF of the system is therefore derived by substituting (1), (2) and (3) in (4) and assuming $(K_d K_0/N)=K$ as:

$$T_{REF}(s) = \frac{K(s^2 K_D + sK_P + K_I)}{s^2(1 + KK_D) + sKK_P + KK_I} \tag{5}$$

B. Phase Detector Noise

Generally PD is not a major source of noise in PLLs. However, the PD detects the phase difference between the VCO and the reference phase divided down by N; therefore, any random variation in the input phase makes the PD to produce undesired output, which when transferred through the PID controller and will result in faulty VCO output. To avoid the effect of PD noise, the required TF is derived as:

$$T_{PD}(s) = \frac{\theta_o(s)}{\theta_{PD}(s)} = \frac{1}{K_d} \frac{G(s)}{1 + G(s).H} \tag{6}$$

The required PD noise TF of the system is therefore derived by substituting (1), (2) and (3) in (6) as:

$$T_{PD}(s) = \frac{K_0(s^2 K_D + sK_P + K_I)}{s^2(1 + KK_D) + sK_P K + KK_I} \tag{7}$$

C. PID Controller Noise

LFs generate noises depending upon the various types and orders. If the signal from PD is not properly filtered by the LF, noisy signal will cause derivative action to be ineffective due to erratic movement of the LF output. Also, improper filtering causes disturbances to other loop components. Adding a PID controller to the system not only reduces the noise level but also smoothens out the system response to dynamic behavior. The PID controller noise TF of the system is given by:

$$T_{PID}(s) = \frac{\theta_o(s)}{\theta_{PID}(s)} = \frac{K_0/s}{1 + G(s)H} \tag{8}$$

Therefore, the required PID controller noise TF is derived by substituting (1), (2) and (3) in (8) as:

$$T_{PID}(s) = \frac{sK_0}{s^2(1 + KK_D) + sKK_P + KK_I} \tag{9}$$

D. VCO Noise

In a PLL-FS, most of the output noises are due to the VCO, mainly because the noise in oscillators amplifies closer to their frequency of oscillation. In our model, the noise generated by the VCO is passed through the FD which appears at the input of PD and then passes through the PID controller. The PID controller allows only those frequencies which are below the cutoff frequency which then appear at the input of the VCO to reduce the output noise. The VCO noise TF of the system is given by:

$$T_{VCO}(s) = \frac{\theta_o(s)}{\theta_{VCO}(s)} = \frac{1}{1 + G(s)H} \tag{10}$$

The required noise TF of VCO is derived by substituting (1), (2) and (3) in (10) as:

$$T_{VCO}(s) = \frac{s^2}{s^2(1 + KK_D) + sKK_P + KK_I} \tag{11}$$

E. Frequency Divider Noise

In PLLs, FD is employed within the loop to reduce the reference frequency. The FD divides the VCO output frequency by a factor N and feeds it to the PD. The FD noise directly appears at the input of the PD. Therefore, it can affect the system noise performance, especially if a high N is used. The FD noise TF of the system is:

$$T_{FD}(s) = \frac{\theta_o(s)}{\theta_{FD}(s)} = \frac{G(s)}{1+G(s)H} \quad (12)$$

Equation (13) provides the required noise TF of FD, which is derived by substituting (1), (2) and (3) in (12):

$$T_{FD}(s) = \frac{2\pi}{K_d} \frac{K_0(s^2K_D + sK_P + K_I)}{s^2(1+KK_D) + sKK_P + KK_I} \quad (13)$$

TABLE I: SIMULATION PARAMETERS

K_d (V/rad)	K_0 (MHz/V)	N	PM (degree)	DF	K_P (10^3)	K_I (10^{12})	K_D (10^{-12})
30	3.3333	10	92.0781	0.625	2.5	40	0.05
35	2.5	11	91.9458	0.631	3	45	
40	2	12	91.8594	0.639	3.5	50	
45	1.6667	13	91.7873	0.648	4	55	
50	1.4286	14	91.7204	0.656	4.5	60	

III. SIMULATION

Table I shows the simulation parameters. Each parameter of the system is chosen in such a way so as to achieve minimum VCO output noise and PN within the loop BW. However, the input reference frequency is kept larger than the loop BW to keep the loop stable and suppress the spurs at the output due to the reference leakage signal. Five different test cases are simulated by using MATLAB program with different phase-margin (PM) and damping factor (DF) to investigate the effect of noise characteristics to have minimum PN contribution within the standard stability limit [4], [22] of the system. The range of PM is chosen from 91.7° to 92° and for DF, the range is from 0.656 to 0.625. This range makes the system more stable with fast switching speed. Beyond this limits, the system undergoes sluggish response leading to unstability. Any noise input through the PD is inversely proportional to the gain K_d. The K_d is therefore chosen in the range of 30-50V/rad to minimize the noise contributions. Reference noise and FD noise are minimized by keeping N small. The PID controller components are chosen to give the required fall in LG at the unity gain point for the loop so that the loop can become stable. If the K_P of the PID controller is set too high, the control loop oscillates and become unstable and on the other hand if K_P is set too low, the system will not achieve the desired control response. For our proposed system, the value of K_P is kept in the range of (2.5×10^3)-(4.5×10^3) in order to achieve the desired noise response. During simulation, it has been found that for $K_P < (2.5\times10^3)$, the system results in OS > 80% with PM < 30^0. For $K_P > (4.5\times10^3)$, the system provides OS < 0.5 with PM > 94^0. The controller response will be sluggish if the integral time of the PID controller is set high. In addition, the system will be unstable and the control loop will oscillate, if K_I is set too low as the integral itself serve as a filter. Therefore, K_I values are set in the range of (40×10^{12}) to (60×10^{12}). For $K_I < (40\times10^{12})$, the system results in PM > 95° with high noise. For $K_I > (60\times10^{12})$, the system results in OS > 55% with DF < 2.5. If K_D is increased too much then oscillations will occur and the control loop will turn unstable as well. The tuning of K_D of PID controller is therefore set to be constant as (0.05×10^{-12}) to reduce the noise level of the system as shown in Table I. If we increase or decrease the value of K_D, the system response time becomes sluggish with large OS and high peaking.

The flowchart of the system for the simulation program developed in MATLAB is given in Fig. 2. The notations h_1, h_2, h_3 and h_4 represent the TF of each block of PLL such as: PD, PID controller, VCO and FD respectively. The notation L gives the forward LG of the system while G gives the closed LG. The notation T provides the overall TF of the system. $T_{REF}(s)$, $T_{PD}(s)$, $T_{PID}(s)$, $T_{VCO}(s)$ and $T_{FD}(s)$ represent the noise TF of reference, PD, PID controller, VCO and FD respectively. The magnitude curve of each PN source is determined by using Bode function to calculate the noise attenuation in dB. First the parameters are initialized to evaluate the TF of all the loop components one by one and then calculate the forward gain (FG) and the LG of the system. After successfully running these steps, the noise TF of all the loop components are evaluated and then simulated to show the magnitude response by using Bode plot.

A. Simulation for Reference Noise

Fig. 3 shows the frequency response of reference noise characteristics of the system. The simulation of reference noise is done by considering (5) using Bode magnitude plot. The x-axis is the offset frequency in Hz whereas the y-axis is the gain in dB. Simulation shows that the reference noise acts as a low pass filter (LPF) characteristics that attenuates signals higher than the cut-off frequencies with a gain of 20log(N), where N is the division factor. The attenuation decreases to zero at a slope of –20.26dB/decade below the cut-off point.

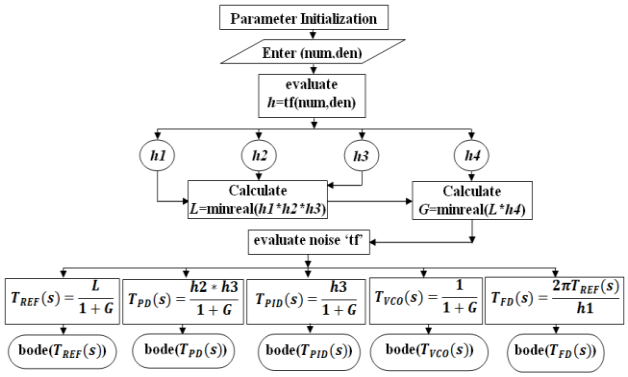

Fig. 2. Flow-chart.

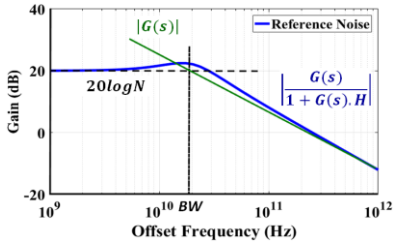

Fig. 3. Reference noise characteristics.

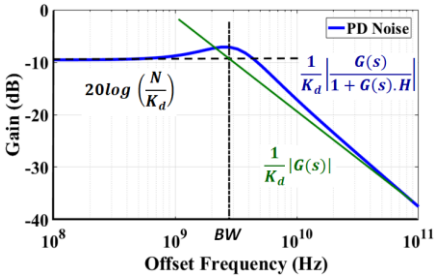

Fig. 4. PD noise characteristics.

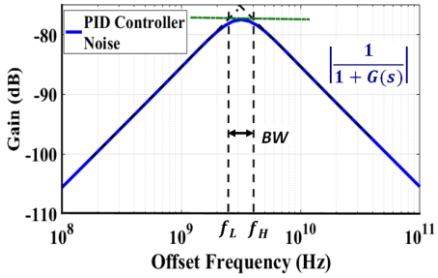

Fig. 5. PID Controller noise characteristics.

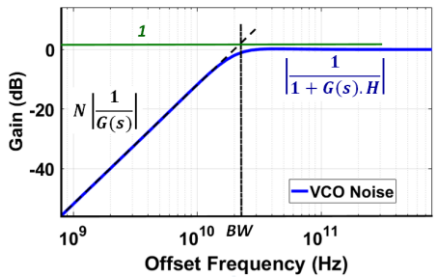

Fig. 6. VCO noise characteristics.

B. Simulation for PD Noise

Fig. 4 shows the simulation results of PD noise by considering (7). For the PD, note the factor of $1/K_d$. Increasing the PD gain provides less PN as it inversely proportional to the input noise. The closed-loop PD noise behaves as a LPF that attenuates high frequencies. The attenuation decreases at a rate of -20.4dB/decade below the cut-off point. A noise peak is observed in the magnitude curve due to the small DF of 0.625.

C. Simulation for PID Controller Noise

Fig. 5 shows the contribution of PID controller noise to the total PN of the PLL system by considering (9). The characteristics of PID controller noise TF acts as a Band-Pass Filter (BPF) that passes one frequency band and attenuates frequencies above and below that band. The attenuation at low noise frequencies increases at a slope of +21dB/decade until the frequency researches the lower cut-off point, f_L and decreases at a rate of -20.6dB/decade below the upper cut-off point, f_H attenuating any high frequency signals. The attenuation at low frequency is higher while at high frequency, the attenuation is lower. A steeper noise peak is observed in magnitude curve due to the small DF of 0.625.

D. Simulation for VCO Noise

Fig. 6 shows the simulation response of the VCO noise TF by considering (11). The closed-loop TF of VCO noise acts as a High Pass Filter (HPF) with only components having high frequency are allowed to pass and the rest are suppressed. The noise TF of the VCO increases at a uniform rate till it attains a constant level for N over the open loop gain for frequencies well inside the loop BW and for the frequencies well outside the loop BW it is at a uniform level as shown in Fig. 6. The attenuation at low frequencies increases at +40.2dB/decade until it researches the cut-off point. A noise peak observed in the noise magnitude curve is due to the small DF of 0.625.

E. Simulation for FD Noise

The simulation of FD noise is done by using (13).The closed-loop TF of FD noise behaves as a LPF characteristics as shown in Fig. 7 which attenuates signals with frequencies higher than the cut-off frequencies. The FD reduces the PN from the VCO by a factor of *N* before it shows up at the PD. Due to the properties of the closed loop system; the PLL in band noise will be effectively multiplied by 20log*N*. For example, an *N*-counter value of 10 translates to 20dB gain of in-band noise with a steeper noise peak. The division ratio, *N* is increased by one from 10-14 to decrease the optimal closed loop BW as higher divide values reduce the noise at the output.

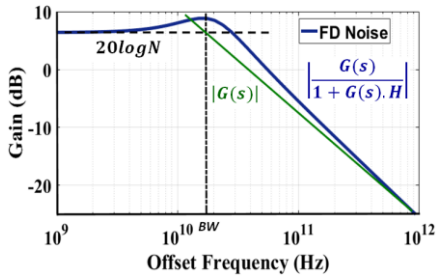

Fig. 7. FD noise characteristics.

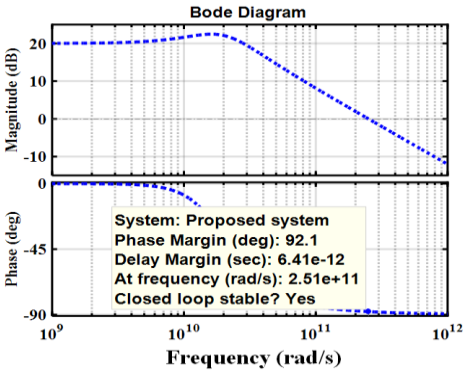

Fig. 8. Bode response.

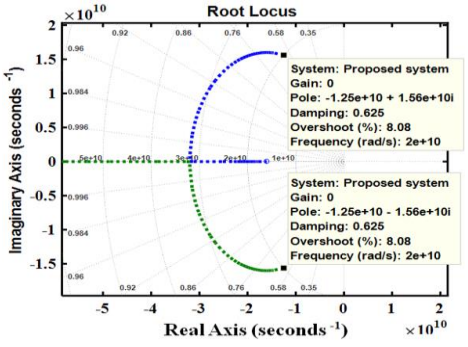

Fig. 9. Root-locus response.

IV. Stability and LT

The system stability is one of the most important factors in PLL. The stability of the proposed system depends on the LG, the PM and the reference frequency. The system stability is explained mathematically using the Bode plot as well as the root locus analysis. Fig. 8 and Fig. 9 shows the bode-plot and root-locus analysis of the system. Since the PM of the system is positive as shown in Fig. 8, the proposed system is highly stable. Also, the proposed system is stable as its poles lie in the left s-plane of root-locus as shown in Fig. 9.

Fig. 10 shows the stability limit of the system. The x-axis is the PM in degrees whereas the y-axis is the DF. In the design of PLL system for optimally integrated PN, it is important to try to minimize the peaking in the PN near the loop BW. For this, the optimal choice of PM should be higher, as high PM provides more stable system [23]. This causes the TF to be more flat at the expense of LT. It also increases the VCO noise suppression near the loop BW making the system more stable. From Fig. 10, it is seen that the proposed system remains stable with increasing PM from 91.7° to 92° regardless of the exponentially decreasing values of DF from 0.656 to 0.625.

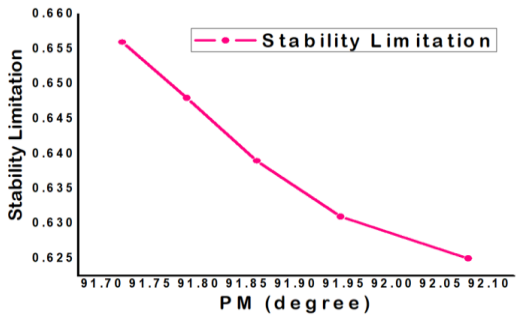

Fig. 10. Stability limit in terms of PM.

Another important aspect of PLL is the switching speed. Fig. 11 shows the impact of loop BW on the LT of the proposed system. The PLL loop BW is not set by the PID controller alone. Changing any of these parameters, K_0, K_d and N also influences the closed loop BW. When closed loop BW is 6.21GHz for minimum PN, the switching speed of the system has its highest LT of 0.238ns. It means that the system can achieve minimum PN and high-speed FS at the same time. The switching speed of the system is inversely proportional to the loop BW. The loop BW of 5.54GHz provides the LT of 0.275ns which is 13.3% slower than the highest switching speed of the proposed system.

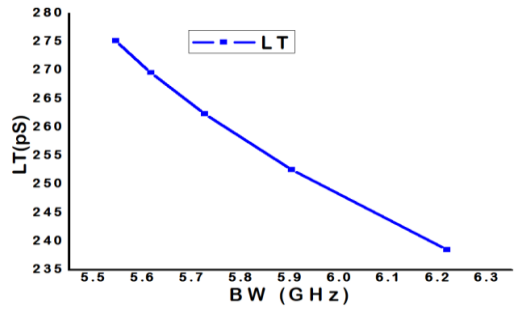

Fig. 11. LT in terms of loop BW.

V. Results and Discussions

Table II shows the simulation results of each source of noise attenuation measured in dB/decade from Bode magnitude plot. The attenuation of each noise source can be determined from bode plot analysis of the respective noise TF. The comparative analysis of the simulated results of the proposed work with previously reported work is shown in Table III. It is observed that the noise attenuation of all the sources of the proposed system is lower than the earlier relevant works.

Table II: Noise Simulation Results

Sl no.	Source	Characteristics	Attenuation (dB/decade)
1	$T_{PD}(s)$	Low- pass	-20.4
2			-20.3
3			-20.2
4			-20.3
5			-20.4
1	$T_{PID}(s)$	Band- pass	-21
2			-20
3			-20
4			-20
5			-20
1	$T_{FD}(s)$	Low- pass	-20.4
2			-20.5
3			-20.04
4			-20.13
5			-20.1
1	$T_{REF}(s)$	Low- pass	-20.26
2			-20.56
3			-20.26
4			-20.31
5			-20.18
1	$T_{VCO}(s)$	High- pass	-40.3
2			-40
3			-40
4			-40
5			-40

Table III: Comparison with Previous Work

Source	Attenuation (dB/decade)				
	This work	Ref. [10]	Ref. [13]	Ref. [21]	Ref. [22]
$T_{PD}(s)$	-20.2 to -20.4	NA	NA	NA	-38
$T_{PID}(s)$	-20 to -21	NA	≈-65	≥-20	-20
$T_{FD}(s)$	-20.04 to -20.5	NA	NA	NA	-38
$T_{REF}(s)$	-20.18 to -20.56	-40	≈-50	-30 to -40	-38
$T_{VCO}(s)$	-40 to -40.3	-40	≈-28	≈-40	-40
Type of LF	PID Controller	2nd order PLPF	3rd order PLPF	2nd order ALPF	ALLF & SFA

The noise contributions of the reference noise, PD noise, PID controller noise and FD noise are shown together in Fig. 12. The x-axis is the frequency in GHz whereas the y-axis is the noise attenuation in dB per decade. The effect of VCO PN attenuation is high as compared to other noise sources as shown in Fig. 12. The attenuation of PD decreases from −20.2dB/decade to −20.4dB/decade, below the crossover frequency. The attenuation of PID controller LF decreases from −20dB/decade to −21dB/decade, below the crossover frequency. The attenuation of FD decreases from −20.04dB/decade to −20.5dB/decade, below the crossover frequency. The attenuation of reference

decreases from −20.18dB/decade to −20.56dB/decade, below the crossover frequency. For VCO, the attenuation decreases from −40db/decade to −40.3dB/decade, below the crossover frequency.

Fig. 13 shows the impact of LT on the noise attenuation. For the reference, PD and FD noise, the attenuation increases slowly as LT increases. For the VCO noise, the attenuation decreases with increasing LT. For the PID controller, the attenuation remains constant at LT between 0.238nS to 0.252nS and then slowly decreases and remains constant at LT between 0.262nS to 0.269nS and then increases again.

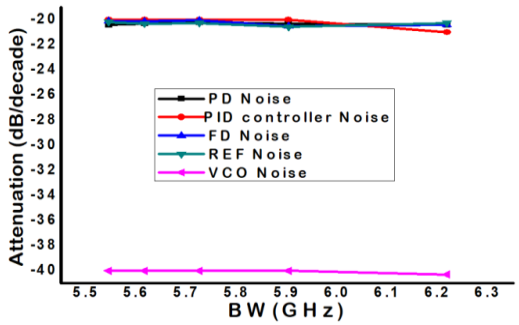

Fig. 12. Effect of loop BW on noise.

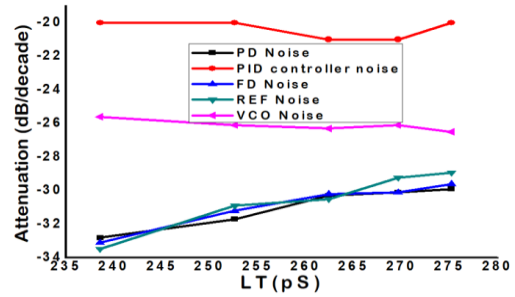

Fig. 13. Effect of LT on noise

VI. Conclusion

The PN mathematical model is designed and simulation of the PN spectrum of the proposed PLL including derivation of noise TF of all the loop components of the system such as the reference noise, the VCO noise, the LF noise and the FD noise are being presented. The PN of the filter contribution is determined in terms of the PID controller. Each noise source affects the total output differently. The reference noise affects the total noise at frequencies lower than the loop BW, while for higher frequencies, the effect is negligible. VCO noise affects the frequency higher than the loop BW. From bode magnitude response; it is observed that the noise TF response of each noise source has a noise peak due to the small DF of 0.625. The noise attenuation value of reference, PD, PID controller and FD are approximately −20dB/decade each while it is −40dB/decade for VCO. Also, the proposed noise model provides high switching speed of 0.238nS at 6.21GHz. As such, we can conclude that the proposed PN model of the PLL with low PN and high LT may be suitable for synthesizer design by accurately tracking the noise contributions of each source.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

G. Konwar initiated the study, prepared the literature and wrote the manuscript before submission; T. Bezboruah revised the manuscript and prepared it for submission; all authors had approved the final version.

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