Overhead and Performance Comparison of SET Fault Tolerant Circuits Used in Flash-based FPGAs

Farouk Smith
Mechatronics, Nelson Mandela University, Port Elizabeth, South Africa
Email: Farouk.smith@mandela.ac.za

***Abstract*—The aim of alternative fault tolerant techniques used in flash-based FPGAs, such as Single Event Transient (SET) filters, is to provide a resource savings advantage when compared to Triple Modular Redundancy (TMR). The purpose of this paper is to quantify, in terms of particular circuit characteristics, what the savings will be. The results suggest that the most important circuit characteristic to determine the gate count increase is the ratio of the number of primary outputs to the original circuit gate count, when considering a combinational circuit. When considering a sequential circuit, the most important circuit characteristic is the ratio of the number of Register Logic (RL) vs. Combinational Logic (CL) in the datapath. The theoretical study found that the DMR and delay element Guard Gate (GG) SET filter technique used in sequential circuits, proved more costly than TMR in terms of resource increase, when the ratio of the number of RL vs. CL is greater than 10% and 28% respectively. Chip-level synthesis of circuits using these filter techniques with one family of flash-based FPGAs shows no gate count cost benefit compared to TMR when the ratio of the number of RL vs. CL is greater than 13% and 15% respectively.**

***Index Terms*—Double Modular Redundancy (DMR), Field Programmable Gate Array (FPGA), Single Event Transient (SET), Single Event Upset (SEU), Triple Modular Redundancy (TMR)**

I. Introduction

The reconfigurable nature of Field Programmable Gate Arrays (FPGAs), together with their relatively low cost and ease of implementation, provided the space industry with an attractive solution for high level computer systems applications. Unfortunately, FPGAs are susceptible to Single Event Effects (SEEs) such as Single Event Transients (SETs) and Single Event Upsets (SEUs).

SETs are caused by charged particles depositing charge on circuit elements through ionization. These deposited charges causes elevated local voltage levels in the circuit elements, which leads to incorrect logic values [1].

In a Combinational Logic (CL) element, the charge will leak away (over several hundreds of picoseconds) and the element, and consequently the system, will return to a consistent state. However, when synchronous logic is disturbed by a SET on a clock edge, the temporary incorrect logic value is latched into the register. This incorrect value can then propagate through the rest of the system compromising its functional integrity. SETs that are erroneously latched by a register are called SEUs. High energetic particle strikes through a memory element such as the configuration memory of an FPGA, causing a bit flip, are also called SEUs.

The response of a particular family of FPGAs to SEUs, is a function of its configuration memory [2]. For example, SRAM FPGAs are a family of FPGAs which have configuration memory that consists of SRAM cells. It has been shown that the configuration memory of SRAM based FPGAs is sensitive to SEUs, which causes a bit flip, when struck by an energetically charged particle [2], [3]. This could cause a change in functionality.

Flash-based FPGAs, on the other hand, have configuration memory that consists of flash-based memory cells, which have been shown to be resistant to SEUs [4], [5]. However, previous tests have shown that flash-based FPGAs are sensitive to soft errors, or SETs, in the combinational user logic, and to SEUs in the sequential logic elements [6].

The focus of this paper is on the SET mitigation schemes used in flash-based FPGAs. In order to use flash-based FPGAs in a radiation environment, the mitigation must be applied to the user logic, as well as the memory elements.

A well-known and common mitigation scheme for correcting the SET and SEU errors in FPGAs is Triple Modular Redundancy (TMR) [7]. The main disadvantage of TMR is the excessive area overhead. The hardened design has at least three times more area and power consumption than the original circuit, excluding TMR overhead. When the TMR hardened designs are implemented with a hardware description language or via the manufacturer's software tools, it instantiates redundant triplicate circuits in the user design as well as voting circuits [8]. This method of implementing TMR results in four [9] to seven times [10] resource increase, which limits its usage to reliability-critical applications.

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Corresponding author: Farouk Smith (email: Farouk.smith@mandela.ac.za).

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Another common mitigation method, however, to mitigate SETs in the user CL of flash-based FPGAs, is to use a SET filter at the inputs of each sequential element [6], [11], [12]. If SEU hardened latches are used in the circuit's sequential logic, SETs in CL can become the primary source of observable errors, if captured by a memory cell [6], [11], [12]. To avoid SET capture by any memory element, the SET filter technique could be used [6], [13].

The generally accepted advantage of using the filter technique in flash-based FPGAs is to provide a gate count and power savings advantage with respect to TMR. Since SET filters are placed at the inputs of the sequential elements only, there is no need to provide triple redundancy in the user logic, and it is therefore, assumed that there will be a resource savings with respect to TMR.

The purpose of this study is to quantify, in terms of particular circuit characteristics, what the savings will be. To facilitate this, the Muller C element SET filtering techniques used in flash-based FPGAs, [6], [11]-[13], will be compared to TMR. We will examine the resource overhead cost benefit of various implementations of the SET filter techniques compared to TMR in order to do a gate count savings analysis. Based on the analysis, we will be able to ascertain whether the savings is a function of a particular circuit characteristic, and whether the assumption always holds true that a gate count savings will be obtained with respect to TMR, by making use of SET filtering techniques.

The Muller C element SET filtering technique used in flash-based FPGAs is well-known and have been the study of several different efforts [6], [11]–[13].

II. Background

A. Description of the Guard Gate SET Filter

A SET filtering technique for CL was previously proposed using Guard Gates [6], [11]–[12]. The guard-gate, Fig. 1 (a), is a circuit consisting of a combination of four Field Effect Transistors (FETs) with two inputs and one output. If the two inputs differ, the output floats in the high impedance state. In this case, the output voltage will maintain its value until leakage current degrades it. However, with the two inputs identical, the Guard Gate (GG) acts like an AND gate.

Fig. 1 (b) illustrates an alternative implementation of the GG. In an FPGA implementation, the guard gate cell (Fig. 1 (a)) is replaced by Look Up Tables (LUTs) that performs the same logic function. Fig. 1 (b) shows the logic implementation on the gate level, a NAND C-element [12]. The C-element, also called a GG, described in [12], is an asynchronous logic component. The output of the C-element reflects the inputs when the states of all inputs match. The output remains in this state until both inputs transition to the other state.

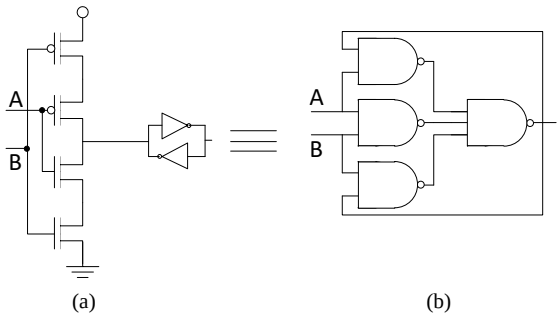

Fig. 1. Alternative implementations of the GG cell [6].

The method proposed in [6], [11]-[13], was to use the GG with a delay in the signal issued from the CL cells with a delay higher than the SET pulse width. Thus, if an SET occurs at the output of the combinational circuit, it will be available immediately at the one input of the GG, but will be delayed by the delay element before it reaches the other input. The delay results in a differing value between the two GG inputs, and hence the output will maintain its value. This will only be valid if the delay in the GG input path is longer than the SET pulse width. If the SET pulse width is longer than the delay, there will be an overlap of the erroneous signals at the inputs of the GG resulting in an erroneous output.

The efficiency of using the delay element will depend on the maximum SET pulse width, since the wider the allowable SET pulse, the lower the maximum allowed frequency of the mitigated design. This results in a performance penalty.

Instead of using an SET filter with a delay element, the CL between two sequential elements could be duplicated and the outputs of these two CL paths will be the GG-inputs [6], [11]-[13]. The timing performance of using a dual redundancy implementation is much improved when compared to the delay element solution. However, the area overhead is at least twice that of the delay element solution.

B. Description of TMR

TMR is a simple method where the circuit is replicated three times. Three signal value outputs are compared by means of a voting circuit, where the output is equal to the two inputs that agree.

Fig. 2 illustrates local TMR (LTMR). Only the sequential elements are tripled. This method of implementing TMR will protect against single errors directly in the sequential elements only. It does not cater for the following: 1) SETs occurring in the combinational circuits (A), which could filter through to the inputs of the sequential elements. If this happens, the SET can be latched if it arrives within the sequential elements' setup and hold time. 2) Transients occurring on the global signals such as the clock, enable and clear lines can cause a SEU. 3) A direct strike to the voter circuit can cause a SET to filter through to the next circuit stage.

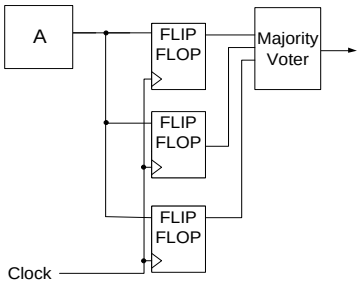

Fig. 2. Local TMR Hardened circuit [6].

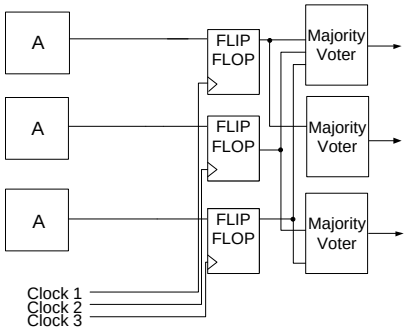

Fig. 3. Full global TMR hardened circuit [6]

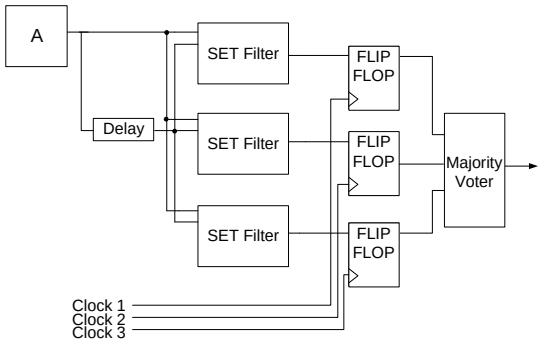

Fig. 4. Hardened delay Element GG circuits with LTMR [6]

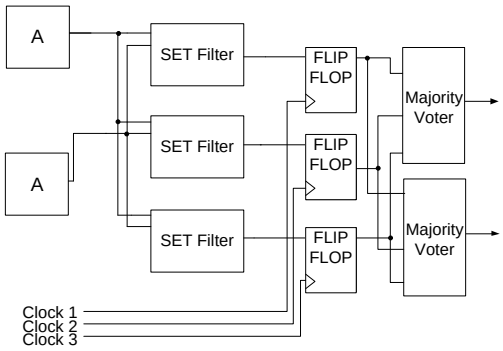

Fig. 5. Hardened DMR circuits with LTMR [6].

In order to mitigate for the previous three failure modes, the circuit in Fig. 3, which illustrates the well known full global TMR, could be used. The user logic, the sequential elements, as well as the voter circuits are tripled.

The SET filtering technique for CL using the GG, in combination with a variation of Global TMR, was previously proposed by Rezqui, *et al*. [6]. The first method makes use of the delay element SET filter, as illustrated in Fig. 4. Using the second method, as mentioned in section A, the CL between two sequential elements could be duplicated and the outputs of these two CL paths will be the GG-inputs, as shown in Fig. 5.

The aim of the GG approach is to save device resources compared to TMR. Therefore, the techniques described above will be compared with TMR, in terms of circuit overhead with respect to the original, for flash-based FPGAs.

III. Overhead Calculation for Combinational Circuits

This section calculates the gate count increase with respect to the original, for a purely combinational hardened circuit, i.e. without any sequential elements. This will aid in understanding the gate count increase in a sequential circuit.

The calculation of the gate count of the hardened circuits can be approached by first listing the general characteristics of the circuit as follows.

Let R be the number of redundant circuits, then, R = 1 for the delay element SET filter hardened circuits, R =2 for the DMR SET filter hardened circuits, and R =3 for the TMR hardened circuits. G_o is the gate count of the original circuit. G_f (or G_v) is the gate count of the filter circuit (or the gate count of the TMR voter), depending on which method is used.

The GG consists of 5 gates (the last stage of the GG is split into 2 gates), the TMR voter circuit consists of 5 gates, and the minimum amount of gates required for the delay element is taken as 2 inverters. The exact number of inverters depend on the amount of delay required.

Therefore, F = 7 for the delay element SET filters (5 gates for the filter plus 2 inverter gates), F = 5 for the DMR SET filters, and F = 5 for the TMR majority voter (3 AND gates and 2 OR gates).

We are only interested in SETs that filter to the outputs of the combinational circuits, therefore, the SET filters, or the TMR voters are inserted at the primary outputs only. As a consequence, the gate count of the hardened circuits is a function of the number of circuit outputs.

Let P be the number of circuit primary outputs. Using the above variables, and A_h represents the area of the hardened circuit, we have

$$A_h = RG_o + G_f P, \text{ or } A_h = RG_o + G_v P \tag{1}$$

Let X stand for the ratio of the number of circuit primary outputs to the original circuit gate count, then,

$$X = \frac{P}{G_o} \tag{2}$$

Therefore, the gate count increase of the hardened circuits with respect to (w.r.t.) the original, G_i, is obtained by

$$G_i = R + G_f X, \text{ or } G_i = R + G_v X \tag{3}$$

Let G_{sdsf} be the gate count savings of the DMR SET filter circuit w.r.t. the TMR circuit, G_v the gate count of TMR vector, and G_{df} the gate count of delay filter, we have

$$G_{\text{sdsf}} = \frac{G_v - G_{\text{df}}}{G_v} = \frac{1}{3}\left(\frac{1}{1+(5/3)(P/G_o)}\right) \tag{4}$$

Let G_{sdesf} be the gate count savings of the delay element SET filter circuit w.r.t. the TMR circuit, A_T the area of TMR, and A_D the area of DMR GG, we have

$$G_{\text{sdesf}} = \frac{A_T - A_D}{A_T} = \frac{2}{3}\left(1-\frac{P}{G_o}\right)\Big/\left(1+\frac{5}{3}\frac{P}{G_o}\right) \tag{5}$$

Fig. 6 is a plot of (2) for the filter and TMR hardened circuits. The TMR implementation in a combinational circuit results in three to eight times resource increase. However, 3 times resource increase is the lower limit and

will only be reached if the number of primary outputs is zero, which is not a valid circuit. The eight times resource increase is the upper limit for TMR in a combinational circuit, and is an extreme case where the number of circuit primary outputs is equal to the number of gates in the original circuit.

The DMR implementations for both the GG filter circuits result in two to seven times resource increase. However, for the same reasons as with TMR, the lower limit will never be reached, and the upper limit of seven times resource increase represents an extreme case. The delay element technique results in one to eight times resource increase, and again, the lower limit will never be reached, and the upper limit represents an extreme case.

These results suggests that the most important variable for determining the resource increase of the hardened circuits w.r.t. the original for a particular redundancy method, is the ratio of the number of primary outputs to the original circuit gate count. This is significant, as can be seen from Fig. 6, that the delay element filter method is worse in terms of resource increase, compared to the DMR filter method, when X is greater than 50%. This is because the area of the delay element SET filter is greater than the area of the DMR SET filter. The slope of (2) is determined by the value of *F*. Thus, the area of the SET filter or voter, which is greatest for the delay element filter, determines the rate of area increase.

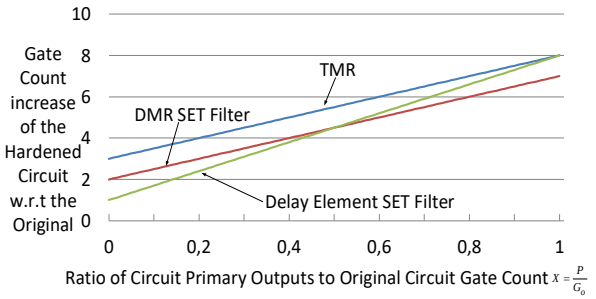

Fig. 6. Gate count increase of the hardened circuits as a function of the ratio of the number of primary outputs to original circuit gate count.

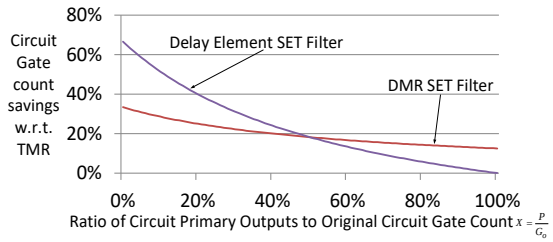

Fig. 7. Area savings w.r.t. TMR, equations (3) and (4).

It is therefore, apparent that the type of redundancy used is not the only deciding factor that determines gate count savings in the hardened circuit; the ratio of primary outputs to original circuit gate count also needs to be considered. This can also be seen by comparing the area savings w.r.t. TMR for the filter techniques. Fig. 7 is a plot of (3) and (4).

The area savings of the delay element SET filter hardened circuit over the TMR hardened circuit is between 0 and 67%. However, the 67% savings is the upper limit and will only be reached if the number of primary outputs are zero, which, again, is not a valid circuit. The 0% saving is the lower limit and is an extreme case where the number of circuit primary outputs is equal to the number of gates in the original circuit.

The area savings of the DMR SET filter hardened circuit over the TMR hardened circuit is between 12.5% and 33.3%. For the same reason as with the delay element filter, these represent upper and lower limits.

IV. Overhead Calculation for Sequential Circuits

The results of the previous section represent the area increase w.r.t. the original, and gate count savings of the SET filter methods w.r.t. TMR, when a purely combinational circuit is hardened. However, a combinational circuit is almost never used alone, and is normally part of a sequential circuit. This section performs the same gate count calculations, however, taking into consideration the effects that sequential elements will have on the circuit gate count increase.

When using global TMR in combination with the DMR SET filter and delay element SET filter, Fig. 4 and Fig. 5, the calculation of the gate count of the hardened circuits, for sequential circuits, can be approached as follows.

The SET filters and primary outputs are triplicated; therefore, the second term of (1) and (2) should be multiplied by 3. In the context of sequential circuits, the number of primary outputs used in Section III should be replaced with the number of sequential elements in the circuit. However, when global TMR is applied together with the SET filter techniques, voter circuits are required at the outputs of the sequential elements, as illustrated in Fig. 4 and Fig. 5. By considering these diagrams, the number of TMR voter circuits required depends on the number of redundant circuits. For example, TMR requires three TMR voters, DMR requires two TMR voters, and the delay element technique requires one TMR voter.

The following calculation does not include the number of sequential elements, which will always be 3 times more than the original for TMR. Therefore, we only consider the gate count increase of the circuit in the datapath.

Let *S* represents the number of sequential elements in the original circuit and G_h represents the gate count of the hardened circuits with global TMR of the SET filters and TMR voter. Using the rest of the variable symbols in Section III, we have

$$G_h = RG_o + 3G_f S + RSG_v \tag{6}$$

Let *Y* stand for the ratio of the number of sequential elements to the original circuit data path gate count, then,

$$Y = S/G_o \tag{7}$$

Let the gate count of the Hardened Circuits with Full GTMR (Fig. 3), be represented by G_{FTMR}, then

$$G_{\text{FTMR}} = 3(G_o + SG_v) \tag{8}$$

Therefore, the gate count increase of the hardened circuits with respect to (w.r.t.) the original, G_{iFTMR}, is obtained by

$$G_{\text{iFTMR}} = 3(1+YG_v) \quad (9)$$

Further, the gate count increase of the hardened DMR filter circuit, with local TMR of the sequential elements (Fig. 5), w.r.t. the original, can be represented by G_{iLTMR} as

$$G_{\text{iLTMR}} = R + 3G_f Y + RYG_v \quad (10)$$

or

$$G_{\text{iLTMR}} = 2(1+YG_v) + 3G_v \quad (11)$$

Additionally, the gate count increase of the hardened delay element filter circuit, with local TMR of the sequential elements (Fig. 4), w.r.t. the original, can represented by G_{iDETMR} as

$$G_{\text{iDETMR}} = R + 3YG_o + RYG_v \quad (12)$$

or

$$G_{\text{iDETMR}} = 1 + 3YG_o + YG_v + YG_f \quad (13)$$

The gate count of the delay element is counted only once in (13), according to Fig. 4, and $G_o = 5$.

Fig. 8 is a plot of (9), (11), and (13). The use of full global TMR results in three to eighteen times resource increase. As before, 3 times resource increase is the lower limit and will never be reached.

The eighteen times resource increase is the upper limit for full global TMR and is an extreme case where the number of circuit sequential elements is equal to the number of gates in the data path of the original circuit. This resource increase is significant when compared to TMR in a purely combinational circuit.

The method of implementing the DMR SET filter methods with local TMR of the filter and voter circuits, results in two to twenty seven times resource increase. Again, for the same reasons as with full global TMR, the lower limit will never be reached, and the upper limit of twenty seven times resource increase represents an extreme case.

The method of implementing the delay element SET filter techniques results in one to twenty three times resource increase, and again, the lower limit will never be reached, and the upper limit represents an extreme case.

The results of this section suggests that the most important variable for determining the resource increase of the hardened sequential circuits, w.r.t. the original, for a particular redundancy method, is the ratio of the number of sequential elements to the original circuit datapath gate count. This is significant, as can be seen from Fig. 8, that the DMR SET filter methods are worse in terms of resource increase, compared to the full global TMR, when Y is greater than 10%. On the other hand, the delay element SET filter methods are worse in terms of gate count increase, compared to full global TMR, when Y is greater than 28%.

In the calculations, the area of the delay element was taken as 2 gates; however, this value could be greater, depending on the amount of delay required. A higher gate count in the delay element will result in greater resource increase w.r.t. the original, compared to using only the 2 inverter gates. For example, by making use of 4 gates in the delay element, the delay element filter methods will be worse than full global TMR in terms of gate count increase, when Y is greater than 22%.

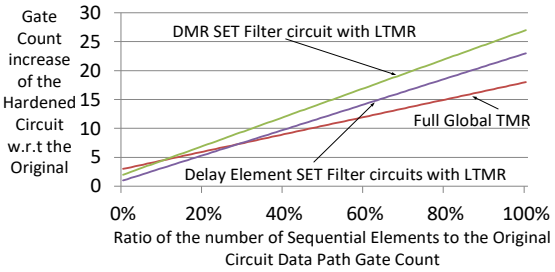

Fig. 8. Gate count increase of the hardened circuits for a sequential circuit.

V. Quantifying Overhead Using Chip-Level Benchmark Simulations

The theoretical gate count and performance of the fault tolerant circuits described in section IV were tested on the sequential circuits of the ITC99 benchmark suite [14], as well as a selection of shift register (SR) circuits.

The benchmark and shift register circuits were chosen so that the gate count and performance could be tested for a wide range of different ratios of CL versus register logic (RL).

The ITC99 netlists which were in Electronic Design Interchange Format (EDIF) were converted into structural VHDL format (gate level netlist). The RTL for the shift registers were also converted into a VHDL gate level netlist. This ensured that the generated VHDL file could be fed into the manufacturer design software to accurately map the designs onto the relevant FPGAs.

An algorithm for generating the sequential circuit structure of Fig. 3, Fig. 4 and Fig. 5 were created to convert the generated VHDL netlist into the functionally equivalent structural VHDL code of the fault tolerant circuits.

The designs were tested using the Microsemi ProASIC3E A3PE600 208 PQFP FPGA and were synthesized with the Synplify Pro E-2010 compiler. All designs were physically mapped onto the A3PE600 using the Microsemi Place and Route Designer V.91 SP3.

The Synplify compiler was prevented from pruning the redundant logic using the appropriate VHDL commands. Timing performance was obtained from the place and route timing report in Microsemi Smart-time analyser.

The normalized gate count and performance results for the designs are summarized in Table I and Table II.

Table I: Gate Count Overhead Comparison

ITC'99	Number of RL	Number of CL	Ratio of RL to CL (%)	DMR GG circuits	Delay Element GG circuits	TMR circuits
SR1	50	503	9.94	3.18	3.10	3.58
SR2	50	403	12.41	3.48	3.35	3.72
b10	17	114	14.91	3.61	3.43	3.43
b07	49	289	16.96	3.71	3.60	3.39
b12	121	620	19.52	4.10	4.04	3.70
b01	5	23	21.74	4.26	4.48	3.48
b04	66	276	23.91	4.66	4.92	3.82
b08	21	66	31.82	5.48	6.17	3.98
b09	28	86	32.56	5.74	6.29	3.91
b02	4	11	36.36	6.00	6.82	4.09
b13	53	139	38.13	5.91	7.16	4.21
b03	30	75	40.00	4.73	7.32	4.08
b06	9	20	45.00	6.75	7.55	4.75

TABLE II: PERFORMANCE COMPARISON

ITC'99	Original cycle time	DMR GG cycle time	Delay element GG cycle time	TMR cycle time
b01	1	1.51	1.54	1.12
b02	1	1.66	1.76	1.30
b03	1	1.28	1.33	1.12
b04	1	1.39	1.46	1.21
b06	1	1.59	1.68	1.25
b07	1	1.15	1.16	1.03
b08	1	1.34	1.37	1.08
b09	1	1.13	1.20	1.04
b10	1	1.26	1.31	1.07
b12	1	1.16	1.36	1.04
b13	1	1.29	1.34	1.25
SR1	1	1.57	1.65	1.27
SR2	1	1.59	1.66	1.22

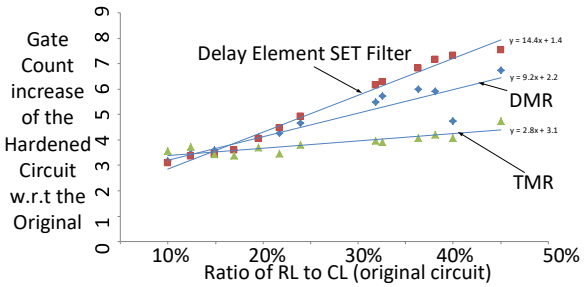

Fig. 9. A plot of the gate count increase versus the ratio of RL to CL (for the original circuit)

A plot of the gate count increase versus the ratio of RL to CL (for the original circuit) as listed in Table I is given in Fig. 9. The red square, blue square and triangle markers represent the gate count increase versus the ratio of RL to CL for the delay element SET filter, DMR SET filter and TMR designs respectively.

The results confirm the theoretical results of section IV, that the overhead efficiency of the delay element SET filter, DMR SET filter and TMR designs are directly dependent on the ratio of RL to CL.

The DMR SET filter method is worse in terms of resource increase, compared to the full global TMR, when the RL/CL ratio is greater than 13%. On the other hand, the delay element SET filter method is worse in terms of gate count increase, compared to full global TMR, when RL/CL ratio is greater than 15%.

The performance of the various sequential circuits are dependent on the maximum delay between registers for a particular design. The majority gate is added for all three fault tolerant implementations as indicated in Fig. 3, Fig. 4, and Fig. 5. However, in addition to the majority gate, the DMR SET filter implementation has an extra component in that the SET filter is added to the datapath, thereby adding an extra constraint and increasing the cycle time. On the other hand, the delay element SET filter implementation has, in addition to the SET filter in the datapath, another delay that depends on the required SET length. This will directly affect an increase in the cycle time.

It is clear from Table II that the DMR and the delay Element method is a performance compromise compared to TMR.

VI. DISCUSSION

The gate count overhead calculation methods developed in this paper only covers mitigation schemes where SETs occur in the user logic and is therefore only applicable to non-volatile FPGAs, such as flash-based FPGAs. Where a different architecture is used, a different method of developing the theoretical formulae of Section III and Section IV needs to be considered. However, in principle, the methods can be used on any programmable logic circuit.

The results showed that the type of redundancy method used is not the only deciding factor to consider when choosing to use a particular mitigation scheme, if the aim is to save device resources.

The results further showed that the gate count of the circuits are not important when determining resource increase w.r.t. the original. The most important determining characteristic of a particular circuit to calculate the gate count increase is the ratio of the number of primary outputs to the number of combinational gates, when considering a purely combinational circuit, and the ratio of the number of RL vs. CL, when considering a sequential circuit.

The gate count increase of the theoretical development and the chip level synthesis are somewhat different. The structures of the fault tolerant circuits used for the theoretical development assumes the use of generic logic gates rather than actual flash-based FPGA resources as used in the chip level synthesis. The manufacturers' synthesis software converts the RTL designs into a physical implementation of the circuit which depends on the architecture of a particular FPGA. However, the results confirm that the efficiency of the fault tolerant circuits depends on the ratio of the number of RL vs. CL of the original circuit.

The results are surprising, and counterintuitive. After all, the main aim of alternative fault tolerant techniques, such as the SET filters used in flash-based FPGAs, is to provide a resource savings advantage when compared to TMR. As both the theoretical and experimental results showed, this is not necessarily the case. The type of redundancy method used is not the only deciding factor to consider when choosing to use a particular mitigation scheme, if the aim is to save device resources.

Circuit designers for radiation environments may take this into consideration when choosing to use a SET filter technique, as opposed to Global TMR. There is no benefit to using the DMR and delay element SET filters for the GG technique when the ratio of the number of sequential elements to the original circuit data path gate count is greater than 13% and 15%, respectively, according to the chip level synthesis and physical mapping to the Microsemi ProASIC3E A3PE600 208 PQFP FPGA. Since there is a performance penalty compared to TMR when using the delay element method, the circuit designer will have to decide at which point the gate count savings is more beneficial than timing performance.

VII. Conclusion

We examined the resource overhead cost benefit and performance of various implementations of the GG SET filter methods compared to TMR. The theoretical as well as experimental results confirm that the efficiency of the fault tolerant circuits depends on the ratio of the number of RL vs. CL for the original circuit.

Based on the theoretical results, there is no resource savings benefit to using the DMR and delay element SET filter techniques in a sequential circuit, compared to TMR, when the RL/CL ratio is greater than 10% and 28%, respectively. At these points, the GG filtering techniques proved to be more costly than TMR.

Based on the experimental results, there appears to be no area cost benefit to using the DMR and delay element SET filter techniques in a sequential circuit when the RL/CL ratio is greater than 13% and 15% respectively. Since there is a performance penalty compared to TMR when using both the DMR and the delay element method for the GG, a critical assessment is necessary for sequential circuits with a high RL/CL ratio to decide which fault tolerant method would be most beneficial.

Conflict of Interest

The author declare no conflict of interest.

Author Contributions

The paper and all work were done by the author who approved the final version.

References

[1] T. Lange, M. Glorieux, D. Alexandrescu, and L. Sterpone, "Functional failure rate due to single-event transients in clock distribution networks," in *Proc. 14th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Mykonos, Greece, 2019, pp. 1-6.

[2] M. Wirthlin, "High-reliability FPGA-based systems: Space, high-energy physics, and beyond," *Proc. of the IEEE*, vol. 103, no. 3, pp. 379-389, March 2015.

[3] K. A. Hoque, O. A. Mohamed, and Y. Savaria, "Formal analysis of SEU mitigation for early dependability and performability analysis of FPGA-based space applications," *Journal of Applied Logic*, vol. 25, pp. 47-68, Dec. 2017.

[4] N. Rezzak, J. J. Wang, M. Traas, *et al.*, "Investigation of TID and dynamic burn-in-induced V_T shift on RTG4 flash-based-based FPGA," *IEEE Trans. on Nuclear Science*, vol. 65, no. 1, pp. 64-70, 2017.

[5] T. S. Nidhin, A. Bhattacharyya, A. Gour, *et al*., "Measurement of radiation absorbed dose effects in SRAM-based FPGAs," *IETE Journal of Research*, Published Online, March 31, 2020.

[6] S. Rezgui, "New methodologies for SET characterization and mitigation in flash-based FPGAs," *IEEE Trans. on Nuclear Science*, vol. 54, no. 6, pp. 2512-2524, Dec. 2007.

[7] J. von Neumann. Probabilistic logics and the synthesis of reliable organisms from unreliable components. 1952. [Online]. Available: www.sns.ias.edu/pitp2/2012files/Probabilistic_Logics.pdf

[8] Y. Li, A. Breitenreiter, M. Andjelkovic, *et al*., "Double cell upsets mitigation through triple modular redundancy," *Microelectronics Journal*, vol. 96, Feb. 2020.

[9] D. R. Gifford and P. M. Parris, "Structures for improving radiation hardness and eliminating latch-up in integrated circuits," U.S. Patent Application 16/183,909, filed May 14, 2020.

[10] K. Morgan, D. McMurtrey, B. Pratt, and M. Wirthlin, "A comparison of TMR with alternative fault-tolerant design techniques for FPGAs," *IEEE Trans. on Nuclear Science*, vol. 54, no. 6, pp. 2065–2072, Dec. 2007.

[11] A. Balasubramanian, B. L. Bhuva, J. D. Black, and L. W. Massengill, "RHBD techniques for mitigating effects of single-event hits using guard-gates," *IEEE Trans. on Nuclear Science*, vol. 52, no. 6, pp. 2531–2535, Dec. 2005.

[12] S. Azimi, B. Du, L. Sterpone, *et al.*, "A new CAD tool for single event transient analysis and mitigation on flash-based FPGAs", *Integration*, vol. 67, pp. 67, 73-81, July 2019.

[13] S. Rezgui, J. J. Wang, Y. Sun, B. Cronquist, and J. McCollum, "Configuration and routing effects on the SET propagation in flash- based FPGAs," *IEEE Trans. on Nuclear Science*, vol. 55, no. 6, pp. 3328-3335, Dec. 2008.

[14] ITC99 Benchmarks. [Online]. Available: http://www.cerc.utexas.edu/itc99-benchmarks/bench.html

Farouk Smith received the Bachelor of Science Degree in physics (1994), the Bachelor of Science in electronics engineering (1996), and the Master of Science in electronics engineering at University of Cape Town (2003). He received the Ph.D. in electronic engineering at the University of Stellenbosch, South Africa, in 2007. He is currently a head of the Department of Mechatronics at Nelson Mandela University. Prof. Smith is also a registered professional engineer with the Engineering Council of South Africa (ECSA) and a Senior Member of the IEEE.