Realization with Fabrication of Double-Gate MOSFET Based Buck Regulator

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***Abstract*—The traditional buck regulator provides the steady output voltage with high efficiency and low power dissipation. Various parameters of this regulator can be improved by the placement of Double-Gate (DG) MOSFET. The double-gate MOSFET provides twice the drain current flow, which improves the various parameters of buck regulator structure and inevitably increases the device performance and efficiency. In this research work, these parameters have been analyzed with implemented DG MOSFET buck regulator and realized the total losses 42.676 mW and efficiency 74.208%. This research work has designed a DG MOSFET based buck regulator with the specification of input voltage 12 V, output voltage 3.3 V, maximum output current 40 mA, switching frequency 100 kHz, ripple current of 10%, and ripple voltage of 1%.**

***Index Terms*—Double-Gate MOSFET, regulator, buck regulator, transistor, microelectronics, VLSI**

I. Introduction

Linear voltage regulators have low power density, efficiency, output voltage, hold-up time, and narrow input range and bulky in size, therefore, it requires the heat sink [1]-[3]. For these reasons, the switch-mode voltage regulators are vital in the electronic field. This topology is highly efficient and offers various advantages over the linear power supply. The 4th Generation (4G) Intel core power architecture using fully integrated voltage regulators provides improvements in mobile computer power, thinner and lighter form factors, and longer battery life [4]. The buck regulator produces a constant DC output voltage, which is lower than the input voltage. The basic structure makes use of inductor and capacitor, due to storing of charge abilities, and diode referred as freewheeling diode [5].

The proposed approach in this research work is based on the switching element i.e. the MOSFET. A novel small-signal averaged model for DC-DC converters operating at variable switching frequency was derived by Priewasser *et al.* [6]. This model yields a linearized small-signal representation of the power conversion circuit, where the ON-time and OFF-time of the Pulse Width Modulation (PWM) signal were treated as distinct control inputs. Reducing the number of large external components, especially inductors, is a very important issue for power management ICs. To meet this requirement Jung *et al.* [7] have designed Single-Inductor Multiple-Output (SIMO) converters. Boscaino *et al.* [8] have introduced an innovative current-sense technique for voltage regulator modules, which is applied to a multiphase buck converter, although the converter topology does not affect the accuracy or effectiveness.

Fu *et al.* [9] have presented a 40 mA buck regulator, which is operating in inherently stable discontinuous conduction mode for the entire load range, which results in compact silicon area, low quiescent current, high efficiency, and robust performance without any calibration. *Shenoy et al.* [10] claim that the experimental results from 12 V to 1.2 V, 10 A, side-by-side comparison reveal up to 12 percentage points higher efficiency at 3 MHz and loss reduction by up to 33% at full load for the series capacitor buck converter. The 10 V output voltage with a maximum 30 A output current was tested by Gu and Zhang [11] with the buck converter using tapped inductor for fast transient response. The rapid advancement in increasing current (above 100 A) requirements of advanced VLSI circuits (e. g. especially microprocessors) with lover voltage than 1 V, transient response of 100 ns, voltage regulation accuracy of lower than 1%, efficiency higher than 90%, motherboard space less than 20 cm^2 has been analyzed by Kinzer [12] with the designing of the DC-DC converter.

Liu *et al.* [13] have implemented a high voltage buck DC-DC converter with 600-nm 40 V CDMOS technology. This bootstrap driver circuit provides 5 V stable bootstrap voltage with a higher drive capability to drive high side switch. Kar *et al.* [14] have presented a 125 MHz fully integrated inductive buck voltage regulator using 11.6 nH wire bond inductance and 3.2 nF on-chip capacitance at 130-nm CMOS technology. The structure of the proposed PWM converter with optimum segmented output stage and mixed load current detector circuits was described by Luo *et al.* [15], which has been implemented at 130-nm CMOS technology and testing results show that the output stages of the PWM converter can self-transit from one segment stage to another according to the load condition. It achieved the maximum efficiency improvement of 15%.

Kilani *et al.* [16] have introduced an efficient reconfigurable multiple voltage gain switched-capacitor DC-DC buck converter for power management unit (for wearable electronics). They have designed and fabricated a switched-capacitor converter in 65-nm low-power

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CMOS technology with an area of 0.493 mm^2. For that design, the peak efficiency was 80% at load current 800 μA and regulated load voltage of 1 V. Faraji *et al.* [17] have presented an integrated synchronous DC-DC buck converter for ultra-low voltage and low power applications with 200 mV to 1 V input and 100 mV to 500 mV output in 45 nm CMOS technology. Krishnamurthy *et al.* [18] have implemented a fully on-die, digitally controlled, 500 MHz switching, 250 mA rated output buck voltage regulator at 22-nm tri-gate CMOS. This system measured a peak efficiency of 68% with an area of 0.6 mm^2 (without output decoupling), a power density of 410 mW/mm^2, and controller bandwidth 43 MHz.

The objective of this present research work is to improve the existing switching voltage regulators by increasing its efficiency with the use of double-gate MOSFET as a basic cell. The improved implementation in buck regulator circuit results in increased efficiency. This is because the DG MOSFET provides double the current compared to that of the single-gate device, and since efficiency is proportional to current, this implies an increased efficiency. The DG MOSFET based buck regulator provides higher current as compared to the traditional MOSFET base buck regulator [19]-[23]. Due to the faster switching of DG MOSFET, the maximum current values are reached in a shorter period of time. In addition, with the use of DG MOSFET the leakage current is minimized compared to traditional MOSFET based structure [2]. This research work designed a DG MOSFET buck regulator with the specification of input voltage 12 V, output voltage 3.3 V, maximum output current 40 mA, switching frequency 100 kHz, ripple current of 10%, and ripple voltage of 1%.

This research paper has been organized as follows. Section II has discussed the basic circuitries, which are used to design this buck regulator. Section III has the modelling of buck regulator with DG MOSFET and its various parameters, and these are simulated in the Section IV. Section V has the fabrication of a buck regulator with DG MOSFET and its testing procedure with results. Finally, Section VI concludes the work and recommends future aspects.

II. Basics of DG MOSFET and Buck Regulator

Here basics of the model (DG MOSFET and buck regulator) used in this research work have been discussed. Since these two models have wide specifications and applications, therefore, authors restrict the discussion related to the specific design. Fig. 1 represents the process of this design.

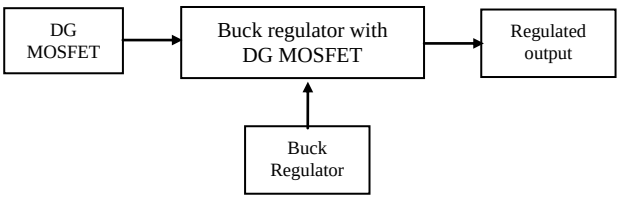


Fig. 1. Process for the design of DG MOSFET based buck regulator.

A. Double-Gate (DG) MOSFET

The DG MOSFET is physically smaller than the conventional MOSFET due to advancements in the fabrication technology [20]-[23]. Gordon Moore made an observation in 1965 that the number of transistors on integrated circuits doubles each year [24]. According to Taur and Ning [25], the main benefit of this structure is shorter channel effects immunity over bulk MOSFETs. Furthermore, the DG MOSFET will be independently driven i.e. the gate terminals will be controlled independently [26]-[28]. According to Cakici and Roy [29], making use of independently driven gates offer benefits, which include help with trade off-switching capacitance or leakage with circuit delay. The DG MOSFET has two gates (front gate and back gate), as shown in Fig. 2.

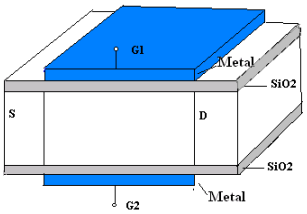


Fig. 2. Schematic of the Double-Gate MOSFET [30], [31]. (S: Source, D: Drain, G1 and G2: Gate-1 and gate-2, SiO2: Silicon dioxide)

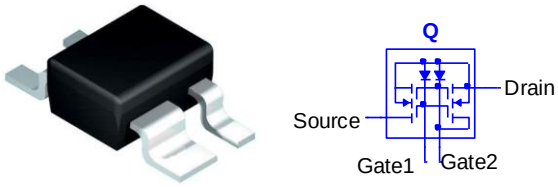
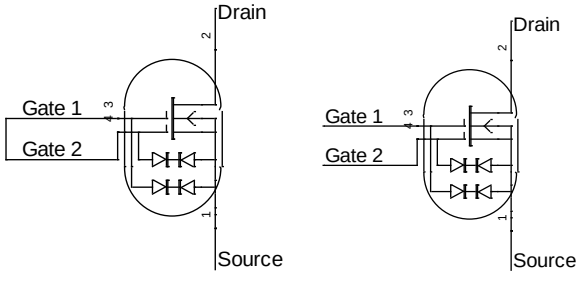


Fig. 3. Double-gate MOSFET structure (BF998) [33].



(a) (b)

Fig. 4. (a) Symmetrical and (b) Independent driven DG MOSFET [33].

Srivastava *et al.* [26], [30]-[32] have performed an inclusive analysis of the low power, high-speed switch with DG MOSFET, and compare it with single-gate MOSFET. This present research work uses the n-channel BF998 DG MOSFET shown in Fig. 3, which is configured in the symmetric mode of operation [33]. This choice is because asymmetric configurations have been proven to have more factors affecting SCE's [34].

When gate-1 (G_1) and gate-2 (G_2) are turned-ON with the same gate voltage (i.e. joined together), the mode of operation is referred as symmetrically driven. If they (G_1 and G_2) don't have a common gate voltage, the mode of operation is referred as independently driven, which are shown in Fig. 4.

B. Buck Regulator

The switching element decides the time durations that the regulator is either in ON-state or OFF-state [3]. For the ON-state, MOSFET connects the input voltage source to the rest of the circuit hence having current flowing through it as part of the ON-state loop. During the OFF-state, the MOSFET disconnects the input voltage supply from the power circuit hence no current flow through it for this duration. The control results in the output voltage are increased when the voltage source decreases or the output voltage decreasing when the input increases. These changes can be sensed by the feedback control circuit, and the control is attained by the switching of the pass element.

The basic functionality of buck regulator is to produce a regulated voltage at the output. This is achieved by the use of energy storage properties of an inductor and capacitor. Fig. 5 consists of a MOSFET, which serves the purpose of the pass element [3], [6], [35]. The gate is connected to a switching control circuit, which consists of an error amplifier, a pulse width modulating circuit, and a current amplifier. The drain is connected to the voltage source and the source is connected to the output filter.

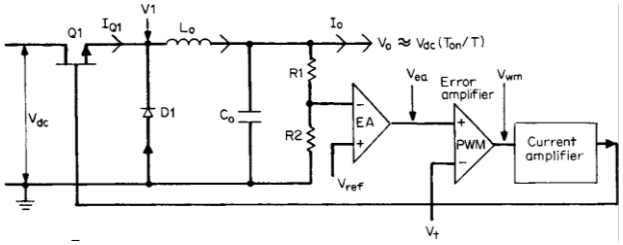


Fig. 5. Buck regulator topology [35].

The stepping down and regulation of the input voltage has been analyzed in [35]. The primary function of a buck regulator is achieved via the inductor L_O, which reduces the voltage produced at the load when connected to the input voltage source by storing energy in a magnetic field. When the inductor is disconnected from the voltage source, it is discharged via the capacitor, which reduces the ripple voltage, and provides current to the load. The switch element is a transistor (Q_1) in this design. This switching frequency is to be chosen carefully as it affects the efficiency and filter component sizes [36], [37].

III. Modeling of Buck Regulator With DG MOSFET and Its Parameters

The proposed DG MOSFET based buck regulator is shown in Fig. 6. The details working procedure has been given by Leeuw and Srivastava in [38]. In this present research work, [38] has been extended further to the fabrication in the following sections. The drain terminal of the DG MOSFET is connected to the inductor and diode whereas the source terminal is connected to the input voltage source. The switching of this transistor helps to maintain the required steady output voltage. Should both gate terminals be functioning, the efficiency of the buck regulator is increased, as explained in the following sections. The ON-state of the buck regulator is achieved when the feedback voltage at the gate terminals is greater than the DG MOSFET cut-off voltage obtained from the data sheet [33].

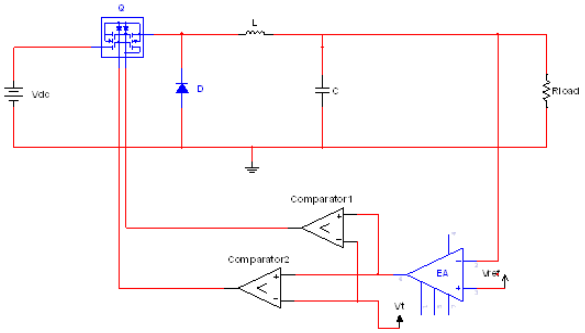


Fig. 6. Block model of proposed buck regulator with DG MOSFET.

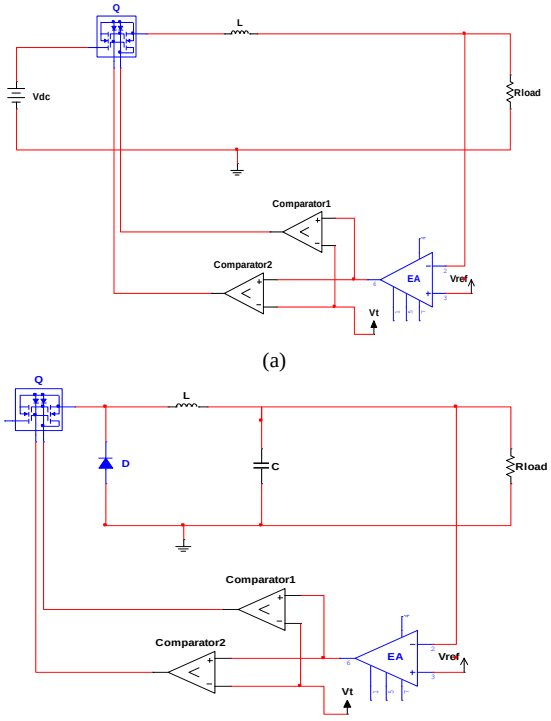


Fig. 7. Buck regulator with DG MOSFET during (a) ON-state, and (b) OFF-state.

During ON-state, the current path is formed from the source through the DG MOSFET to the inductor and to the load, as illustrated in Fig. 7 (a). The voltage across the inductor during this state of operation is V_{dc}–V_{out}. The current through the inductor during this mode of the operation increases linearly until it reaches a maximum value. The diode in the complete model prevents the reverse discharge of the capacitor, only allowing current to flow in the one-loop as illustrated. The charge storing characteristics of both the inductor and capacitor are employed to obtain the functionality of the system. Therefore, the selections of these components are a necessity for specific applications. During ON-state, the current through the inductor causes to build up an electric field which stores charge. This causes the current till it reaches to extreme value (I_{Lmax}). To maintain the output voltage feedback circuit has been connected. This is

achieved by comparing the voltage sensed by the load and sensing resistor with the help of the Error Amplifier (EA). If the input voltage increases, this will result in the switches ON-time decreasing and vice versa [34].

The OFF-state takes place during (t_{off}) when the feedback voltage is less than the cut-off voltage of the MOSFET, as shown in Fig. 7 (b). During this mode of operation, the current loop is through the inductor through the output and via the diode. The input voltage is disconnected from the circuit via the MOSFET and no current flows through it. In this situation, inductor now serves as the power source of the circuit, whilst the voltage across the inductor is reversed due to the fact that the voltage on the output side of the inductor is now higher than that of the voltage on the input side of the inductor. This is as a result of the input source being disconnected from the circuit. The capacitor helps the inductor discharge and provides the current flow to the load. The inductor discharges linearly until it reaches a minimum value (I_{Lmin}).

Rate of charging of inductor is faster using DG MOSFET. The diode is employed to complete the current loop in this mode. The current produced at the output is the mean value of the ramp currents through the inductor during the charging and discharging of the inductor between these two modes of operation [35], [36].

In the event of an increase in the input voltage, the output of the error amplifier decreases. An increase in the output of this error amplifier results in the switches on-time decreasing. This is achieved by comparing the error amplifier voltage to the generated sawtooth wave. This comparison results in the required pulse width modulation waveform required to drive the gate terminals of the MOSFET. Similarly, a decrease in the input voltage results in greater output at the error amplifier, as greater the output of the error amplifier, the greater switch ON time. Again, this is compared to the generated sawtooth wave. In increasing the switch ON time, the voltage produced at the output is increased. It is through this switching action and control that the output voltage is kept constant and steady, and it is all dependent on the switching element, in this case, the DG MOSFET.

In the parametric analysis, the terms t_{on} and t_{off} refer to the switching transition times (not the duty cycle time periods). These switching transition time periods affect the regulator performance with regard to its conduction losses, conduction efficiency, and overall efficiency, amongst others [3], [34], [38]-[41].

A. Inductor Current

For the pass element using (1) of ref. [38]; a linearly increasing induced current (ON-state) across the inductor is [35]:

$$\frac{di}{dt}=\frac{V_{\rm dc}-V_o}{L_o},\ \ I_{L\max}=V_o\left[\frac{1}{R_{\rm load}}+\frac{(1-D)}{2Lf_{\rm sw}}\right] \tag{1}$$

During the OFF-state the discharging inductor current rate is:

$$\frac{di}{dt}=\frac{V_o+1}{L_o},\ \ I_{L\min}=V_o\left[\frac{1}{R}-\frac{(1-D)}{2Lf_{\rm sw}}\right] \tag{2}$$

Since the output current of the regulator is fixed, therefore, whilst the DG MOSFET results in double current flow at its output, the system current will be fixed, but the time period will decrease. In this situation, maximum and minimum inductor currents can be achieved. Therefore, at ON-state the inductor current for DG MOSFET based circuit increases at the rate of:

$$\left(\frac{di}{dt}\right)_{\rm DG}=2\frac{V_{\rm dc}-V_o}{L} \tag{3}$$

The DG MOSFET current still decreases at the same rate as in the case of the conventional MOSFET structure during OFF-state. Therefore, the discharging of inductor experiences no change as an effect of having two gate terminals rather than one, which is beneficial for the designed device.

B. Conduction Efficiency

The conduction losses in the buck regulator topology are mainly as a result of the switching component and the diode. According to [35], [38], [39], during conduction times t_{on} and $t_{off,}$ the current through these components are at the centre of the ramp current, which corresponds to the output current value and flow at a forward voltage of 1 V over a wide range of currents. For the normal buck topology, i.e. using single gate MOSFET, these conduction losses ignoring AC switching losses are given as:

$$P_{\rm dc}=L(Q_1)+L(D_1)=1I_o\frac{t_{\rm on}}{T}+1I_o\frac{t_{\rm off}}{T}=1I_o \tag{4}$$

When making use of the DG MOSFET, the switching transition period T_{on} is halved. This is due to the fact that the DG MOSFET is able to produce double the current hence allowing the maximum current to be reached in half the time period. This results in the conduction losses changing as:

$$\begin{aligned}P_{\text{dc-DG}}&=L(Q_1)+L(D_1)\\&=1I_o\frac{t_{\rm on}}{2T}+1I_o\frac{T-t_{\rm on}}{T}=I_o-\frac{I_o t_{\rm on}}{2T}\end{aligned} \tag{5}$$

This clearly illustrates the use of the DG MOSFET results in smaller losses as compared to that of the single gate MOSFET. The conduction efficiency of a buck regulator can be determined using [35]:

$$\eta_{\rm conduction}=\frac{P_o}{P_o+\text{losses}}=\frac{V_oI_o}{V_oI_o+1I_o}=\frac{V_o}{V_o+1} \tag{6}$$

Therefore, the conduction efficiency for DG MOSFET will be:

$$\eta_{\text{conduction-DG}}=\frac{V_oI_o}{V_oI_o+I_o\left[1-t_{\rm on}/2T\right]}=\frac{V_o}{V_o+1-t_{\rm on}/2T} \tag{7}$$

With the use of the DG MOSFET, conduction losses decrease, the denominator decreases, so conduction efficiency increases, resulting in improved performance of the designed buck regulator.

C. Switching Power

The switching loss of the MOSFET is determined by the overlap of the current and voltage during the switching ON and OFF periods of the MOSFET. The losses or these switching transition periods when using a single-gate MOSFET is given by [3], [34], [39]:

$$\begin{aligned} P_{\text{switching}} &= P(t_{\text{on}}) + P(t_{\text{off}}) \\ &= \frac{I_o V_{\text{dc}} t_{\text{on}}}{6T} + \frac{I_o V_{\text{dc}} t_{\text{off}}}{6T} \\ &= \frac{I_o V_{\text{dc}}}{3}\left(\frac{t_{\text{on}} + t_{\text{off}}}{T}\right) \end{aligned} \tag{8}$$

The switching losses in DG MOSFET is decreases due to the fact that the DG MOSFET produces twice the output or drain current as compared to that of the single-gate MOSFET during the ON-state. Due to the fact that in the buck regulator topology, the inductor current is equal to the output current, authors assume that the MOSFET switching transition period t_{on} is halved rather than the output current increased as the regulator output current is fixed in the design process. This is due to the two gate terminals operating simultaneously and results in switching power as:

$$\begin{aligned} P_{\text{switching-DG}} &= P(t_{\text{on}}) + P(t_{\text{off}}) \\ &= \frac{I_o V_{\text{dc}} t_{\text{on}}}{12T} + \frac{I_o V_{\text{dc}} (1 - t_{\text{on}})}{6T} \\ &= \frac{I_o V_{\text{dc}}}{12}\left(\frac{2T - t_{\text{on}}}{T}\right) \\ &= \frac{I_o V_{\text{dc}}}{12}\left(\frac{2t_{\text{on}} + 2t_{\text{off}} - t_{\text{on}}}{T}\right) \\ &= \frac{I_o V_{\text{dc}}}{12}\left(\frac{t_{\text{on}} + 2t_{\text{off}}}{T}\right) \end{aligned} \tag{9}$$

Therefore, the switching loss for the DG MOSFET is less than that of the single-gate MOSFET. In sub-section E, it contributes to the system efficiency.

D. Total Losses

The total losses are given by the sum of the AC and DC losses of the system [35] i.e.

$$\text{Losses}_{\text{Total}} = \text{Losses}_{\text{AC}} + \text{Losses}_{\text{DC}} \tag{10}$$

In the case of the standard MOSFET based buck regulator topology, this is given by:

$$\text{Losses}_{\text{total}} = I_o + \frac{I_o V_{\text{dc}}}{3}\left(\frac{t_{\text{on}} + t_{\text{off}}}{T}\right) \tag{11}$$

Considering the changes in the AC losses and DC losses when using the DG MOSFET structure as discussed in (5) and (9), the total losses are now given as:

$$\text{Losses}_{\text{Total-DG}} = I_o\left[1 - \frac{t_{\text{on}}}{2T}\right] + \frac{I_o V_{\text{dc}}}{12}\left(\frac{t_{\text{on}} + 2t_{\text{off}}}{T}\right) \tag{12}$$

E. Efficiency

The AC (switching) losses are result of the switching device i.e. MOSFET [35]. For the traditional buck regulator, the efficiency is taken as:

$$\begin{aligned} \text{Efficiency} &= \frac{P_o}{P_o + \text{DC}_{\text{losses}} + \text{AC}_{\text{losses}}} \\ &= \frac{V_o I_o}{V_o I_o + 1 I_o + \frac{I_o V_{\text{dc}}}{3}\left(\frac{t_{\text{on}} + t_{\text{off}}}{T}\right)} \\ &= \frac{V_o}{V_o + 1 + \frac{V_{\text{dc}}(t_{\text{on}} + t_{\text{off}})}{3T}} \end{aligned} \tag{13}$$

Using DG MOSFET, these AC losses becomes half, then the designed buck regulator efficiency increases and using (5), (9), and (12) can be calculated as:

$$\text{Efficiency}_{\text{DG}} = \frac{V_o}{V_o + 1 + \frac{V_{\text{dc}}(t_{\text{on}} + 2t_{\text{off}})}{12T}} \tag{14}$$

It is greater efficiency than the traditional buck regulator.

IV. Simulation and Parametric Analysis of DG MOSFET Based Buck Regulator

Firstly, a basic MOSFET based buck regulator has been revisited, thereafter the DG MOSFET based buck regulator has been designed and fabricated.

A. Buck Regulator with Single-Gate MOSFET

Simulation has been performed on various parts individually and then combined such as power circuit, pulse wave generator to avoid the software runtime errors. For the comparison, simulations have been performed on single-gate MOSFET based buck regulator and DG MOSFET based buck regulator separately as shown in Fig. 8 to Fig. 11, respectively. The system has been tested and then fabricated in the further sections. Simulation results illustrating PWM wave for single-gate MOSFET based buck regulator is shown in Fig. 9.

By the buck regulator with the use of a single-gate MOSFET, the following results have been obtained from the simulation. The efficiency of the system using the equation derived by *Pressman et al.* [35] gives the value using (13) as:

$$\text{Efficiency} = \frac{V_o}{V_o + 1 + \frac{V_{\text{dc}}(t_{\text{on}} + t_{\text{off}})}{3T}} = 74.01\%$$

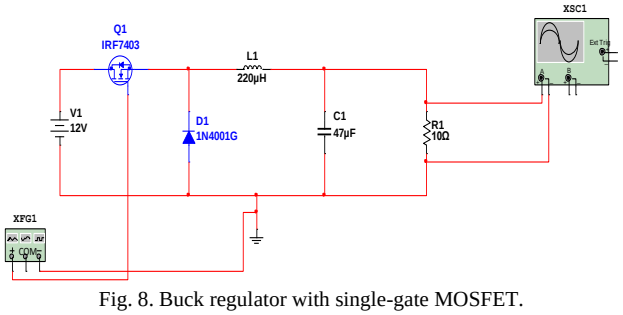


Fig. 8. Buck regulator with single-gate MOSFET.

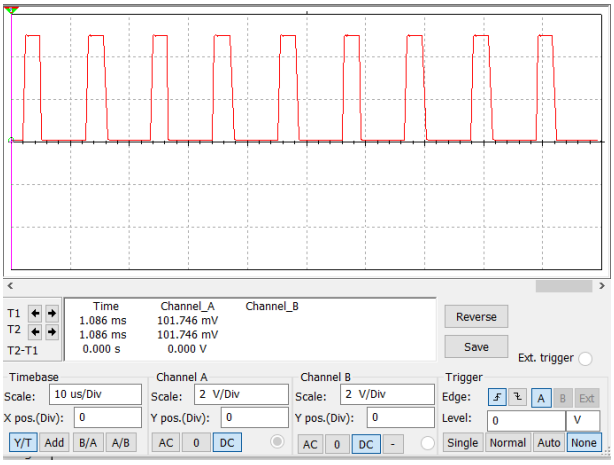


Fig. 9. Simulation results illustrating PWM wave for single-gate MOSFET based buck regulator.

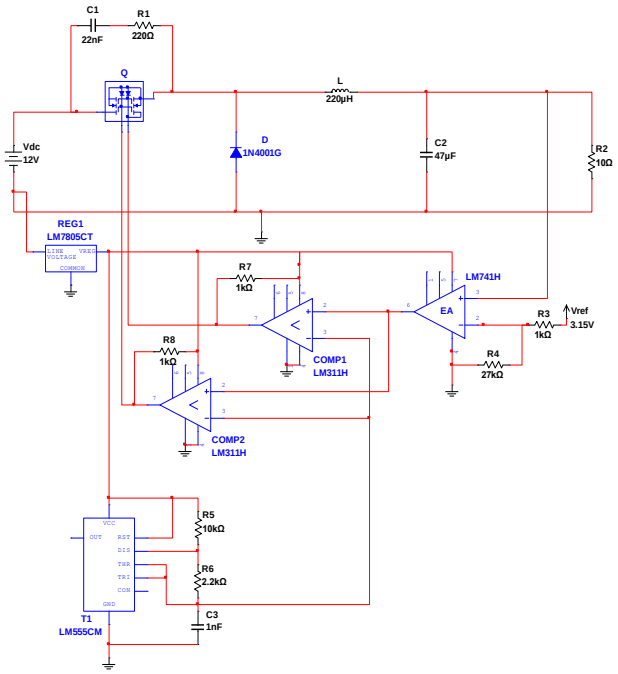


Fig. 10. The full circuit design of DG MOSFET based buck regulator.

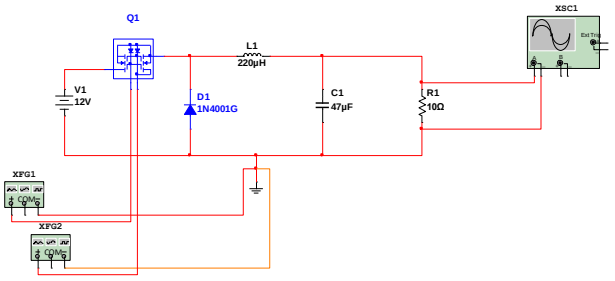


Fig. 11. Buck regulator with DG MOSFET for simulation.

B. Buck Regulator with Double-Gate MOSFET

The complete circuit design (Fig. 10) comprises of the DG MOSFET, inductor, capacitor, and the load resistor. A feedback circuit is used to control the DG MOSFET. This includes a LM741 error amplifier and two comparators used to feed the two gate terminals. The sawtooth wave required for PWM is formed with the use of a NE555 timer. The LM741 operational amplifier has been chosen as an error amplifier with V_{ref} = 3.15 V. The duty cycle for the circuit is $D = V_o/V_{dc}$ = 3.33/12 = 0.275. On the basis of this duty cycle, the inductor can be calculated [35] as:

$$L_{crit} = \frac{(1-D)V_o}{2fI_{OCCM}} = \frac{(1-0.275)\times 3.3}{2\times 100\times 10^3\times 0.1} = 119.625\ \mu H$$

which is near to the standard inductor of 220 µH inductor. The minimum output capacitor can be calculated [35] as:

$$C = \frac{(1-D)}{8Lf^2\times \%V_o} 4.2\ \mu F$$

Since this is the minimum capacitor value, so for the design purpose, 47 µF capacitor has been selected.

The snubber circuit (a combination of C_1, R_1, and Q) is used to protect the diode and DG MOSFET from being damaged by voltage spikes due to the back emf that may be experienced when switching between ON-state and OFF-state [42, 43]. The spike is caused by the instant reversed voltage across the inductor as the inductor polarity reverses during this switch, but current tries to continue flowing in the direction it has been flowing in. The snubber actually slows the voltage spike voltage over a certain time and delivers to the diode, this done with the capacitor. The resistor and capacitor drop the voltage across themselves and reduces the spike.

$$R_{snubber} = \frac{V_{dc}}{I_{out(max)}} = \frac{12}{40} = 82.5\ \Omega$$

$$C_{snubber} = \frac{P}{f(V_{DC})^2} = \frac{0.25}{100\times(12)^2} = 17.36\ nF$$

Therefore, in this design, the selected snubber resistance is 220 Ω and the capacitor is 22 nF. The combination of the sawtooth generator using a NE555 timer and a comparator forms the PWM square wave required for driving the gate terminals of the DG MOSFET. Two comparators will be employed and fed by the NE555 timer as the DG MOSFET will be operating in an independently driven mode i.e. each gate terminal fed by independent voltage sources.

To compare the circuit behaviors gate terminals are independently fed with identical pulse waves of the same duty cycle. The simulation does, however, still assist in the analysis of the behavior of the system compared to its behavior with the use of the single-gate MOSFET structure.

Fig. 12 represents the simulation results for the DG MOSFET based buck regulator and summarized in Table 1 with the comparison of single-gate MOSFET. The conduction losses for the DG MOSFET based buck regulator using (5) is:

$$P_{dc\text{-}DG} = I_o - \frac{I_o t_{on}}{2T}$$

$$= 330\ mA - \frac{330\ mA\times 0.15\ \mu s}{2\times 10\ \mu s}$$

$$= 305.25\ mW$$

The conduction efficiency has been calculated using (7) as:

$$\eta_{\text{conduction-DG}} = \frac{V_o}{V_o + 1 - \frac{t_{\text{on}}}{2T}} = \frac{3.35}{3.35 + 1 - \frac{0.15\ \mu\text{s}}{2 \times 10\ \mu\text{s}}} = 77.14\%$$

The switching power has bene calculated using (9) as:

$$P_{\text{switching-DG}} = \frac{I_o V_{\text{dc}}}{12}\left(\frac{t_{\text{on}} + 2t_{\text{off}}}{T}\right) = 14.85\ \text{mW}$$

Therefore, the total losses using (12) can be calculated as:

$$\text{Losses}_{\text{Total-DG}} = I_o\left[1 - \frac{t_{\text{on}}}{2T}\right] + \frac{I_o V_{\text{dc}}}{12}\left(\frac{t_{\text{on}} + 2t_{\text{off}}}{T}\right) = 313\ \text{mW}$$

However, the efficiency of this designed circuit can be realized using (14):

$$\text{Efficiency}_{\text{DG}} = \frac{V_o}{V_o + 1 + \frac{V_{\text{dc}}(t_{\text{on}} + 2t_{\text{off}})}{12T}} = 76.48\%$$

Fig. 12. Simulation results illustrating sawtooth wave and PWM wave for DG MOSFET based buck regulator.

TABLE I: COMPARISON OF SINGLE-GATE MOSFET AND DOUBLE-GATE MOSFET BASED BUCK REGULATOR

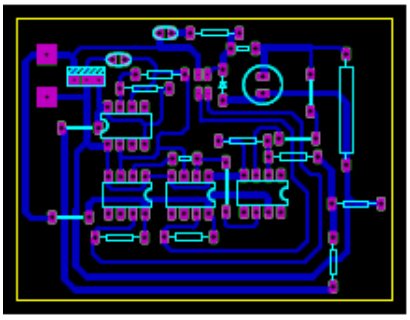
Parameters	Single-Gate MOSFET based buck regulator	Proposed Based buck regulator
Input Voltage	12 V	12 V
Output Voltage	3.19 V	3.35 V
Output Current	319 mA	330 mA
PWM Frequency	100 kHz	100 kHz
PWM Time Period	10 µs	10 µs
Switch ON-Time	0.15 µs	0.15 µs
Switch OFF-Time	0.15 µs	0.15 µs
Switch Transition Period	0.3 µs	0.225 µs
Output Power	1.018 W	1.106 W
Efficiency	74.01 %	76.48 %

This efficiency is for the design circuit with the DG MOSFET, which is better than the efficiency of a single-gate MOSFET based buck regulator. The power delivered to the load is greater in the DG MOSFET case compared to traditional MOSFET structure. The efficiency calculations using the simulated results prove that the DG MOSFET provides greater efficiency. Table I compares the performance of the regulator with the use of the conventional MOSFET against that of the DG MOSFET according to simulation results.

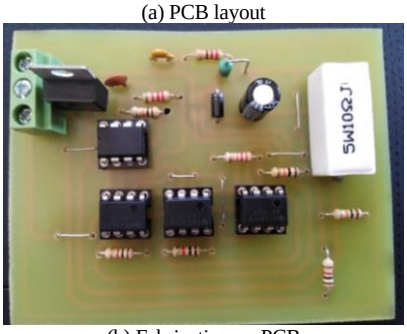
V. FABRICATION OF BUCK REGULATOR WITH DG MOSFET AND ITS TESTING

The Printed Circuit Board (PCB) design, as shown in Fig. 13 is a method of connecting the electronic components. Using a material, which conducts current connections or traces is etched onto a non-conducting surface. This layout results in a more compact and secures design as compared to breadboard or veroboard. Design software including Proteus [44] and Multisim [45] have a PCB layout feature, the designer then has to manoeuvre the components around to achieve a presentable and well thought out layout in terms of the connectivity (i.e. not crossing different connection tracks). The PCB layout produced by the simulation software is shown in Fig. 13.

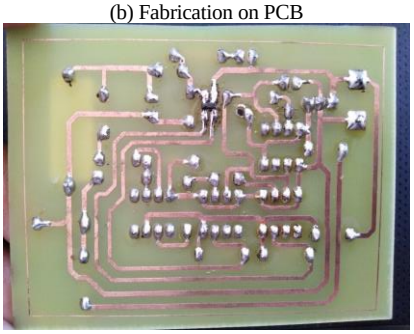
The design is then printed onto the non-conducting substrate as well as the conducting pattern [20], [22], [23]. In this design, the DG MOSFET is soldered on the reverse side of the board as shown in Fig. 13 (c) due to its size. The DG MOSFET used is very sensitive to over current and burns out quickly, it is, therefore, important to use the regulator at the rated parameter values i.e. current of 40 mA. The 12 V input is connected to the terminals on the board with +12 V connected at the top and ground at the bottom. The output voltage is measured across the load resistor.



(a) PCB layout



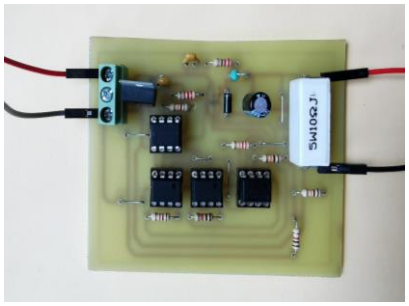
(b) Fabrication on PCB



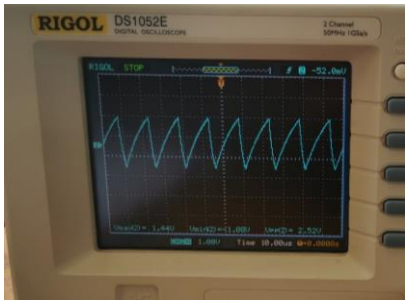
(c) Fabrication on PCB showing surface mount DG MOSFET

Fig. 13. Fabrication process of the DG MOSFET based buck regulator.

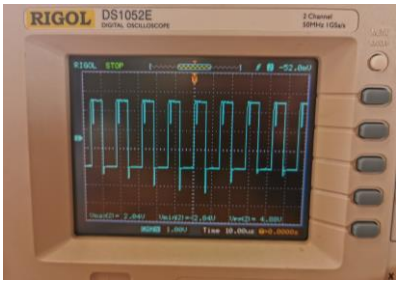
The sawtooth wave can be seen on an oscilloscope by connecting it to pin-7 of the NE555 timer and ground. The PWM waveform is visible at pin-7 of either of the two LM311 comparator chips. The feedback loop that drives the DG MOSFET terminals requires a sawtooth wave compared to the error amplifier voltage to produce the Pulse Width Modulation (PWM) square waveform. This sawtooth waveform is generated with the use of a NE555 timer, as shown in Fig. 14. With the sawtooth wave signal and the error amplifier output voltage as inputs to the LM311 comparator, the PWM waveforms are shown in Fig. 14. This waveform contains valuable information pertaining to the working of the regulator i.e. ON and OFF times of the switch (t_{on} and t_{off}) and duty cycle. Table II shows the values obtained when testing the implemented regulator.



(a) Measurement setup of the fabricated device and other equipment



(b) Generated sawtooth wave



(c) Generated PWM waveform

(d) PWM Frequency and period

Fig. 14. Measurement stages for the various parameters of the fabricated devices.

TABLE II: FABRICATION RESULTS FOR BUCK REGULATOR WITH DG MOSFET

Parameters	Values of fabricated device
Input voltage	12 V
Output voltage	3.1 V
Output current	40 mA
PWM frequency	70.42 kHz
PWM time period	14.2 μs
Switch ON-time	300 ns
Switch OFF-time	400 ns
Duty cycle	21.93 %

Using the equations derived theoretically in the parametric analysis section various parameters have been calculated (based on the values obtained in Table II). The conduction loss using Eq. (5) has been calculated as:

$$P_{\text{dc-DG}} = I_o - \frac{I_o t_{\text{on}}}{2T} = 39.577 \text{ mW}$$

The conduction efficiency as analysed in (7) can be calculated as:

$$\eta_{\text{conduction-DG}} = \frac{V_O}{V_O + 1 - t_{\text{on}}/2T} = 75.81\%$$

For this designed circuit, the switching power using (9):

$$P_{\text{switching-DG}} = \frac{I_O V_{\text{dc}}}{12}\left(\frac{t_{\text{on}} + 2t_{\text{off}}}{T}\right) = 3.099 \text{ mW}$$

Therefore, total losses using (12) for this designed circuit has been analysed as:

$$\text{Losses}_{\text{Total-DG}} = I_O\left[1 - \frac{t_{\text{on}}}{2T}\right] + \frac{I_O V_{\text{dc}}}{12}\left(\frac{t_{\text{on}} + 2t_{\text{off}}}{T}\right) = 42.676 \text{ mW}$$

Finally, the efficiency of this fabricated buck regulator has been achieved using (14) as:

$$\text{Efficiency}_{\text{DG}} = \frac{V_O}{V_O + 1 + \frac{V_{\text{dc}}(t_{\text{on}} + 2t_{\text{off}})}{12T}} = 74.208\%$$

Comparing to the theoretical (simulated) buck regulator with DG MOSFET to the implemented regulator, it has been noticed that the large differences are pertaining to conduction losses, switching power and total losses. The losses in terms of the implemented regulator are much lower, which is an advantage on the system. As a means of comparing the simulated and practical results, Table III compares these results.

TABLE III: SIMULATED AND FABRICATED RESULTS COMPARISON OF DG MOSFET BASED BUCK REGULATOR

Parameters	Simulation Results	Designed Results
Conduction Losses	303.25 mW	39.577 mW
Conduction Efficiency	77.14 %	75.81 %
Switching Power	14.85 mW	3.099 mW
Total Losses	313 mW	42.676 mW
Efficiency	76.84 %	74.208 %

VI. Conclusions and Future Recommendations

In this research work, the focus was on the parametric analysis of the buck regulator with the use of DG MOSFET. Through the use of this DG MOSFET analysis reveals that the DG MOSFET provides faster switching action. The switching time affects various parameters of the buck regulator, most importantly, its efficiency. In this research work, these parameters, based on implemented buck regulator with the use of a DG MOSFET, have been analyzed with its total losses at 42.676 mW and efficiency of 74.208%. This research work designed a DG MOSFET based buck regulator with the specification of input voltage 12 V, output voltage 3.3 V, maximum output current 40 mA, switching frequency 100 kHz, ripple current of 10%, and ripple voltage of 1%.

The conduction efficiency and overall efficiency of the regulator proved to be close to expected theoretical findings with minor differences of ± 2% occurring due to the fabrication of various sections. In conclusion, theoretical analysis and further the implementation of the regulator (fabricated device) with the use of the DG MOSFET enhance and improve the regulator performance in terms of efficiency and losses.

In future, the frequency range can be increased as per the device application. Further improvements could be made on the design to enhance its performance and safety i.e. current protection, diode snubber, input capacitor, etc.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Simone Leeuw (SL) and Viranjay M. Srivastava (VMS) conducted this research; SL designed and fabricated the circuit after that analyzed the data and wrote the paper; VMS has verified the result with the designed circuit; all authors had approved the final version.

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