Realization with Fabrication of Double-Gate MOSFET Based Class-AB Amplifier

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***Abstract*—This research work designs the class-AB amplifier with the application of Double-Gate (DG) MOSFET, which provides insight on how the amplifier can be utilized, in accordance with its future design. Main consideration is the use of DG MOSFET in audio amplifier design, for its low power and low noise application, voltage regulation for high to low power, etc. The challenge of this design is an attempt to use the DG MOSFET as prominent component, to demonstrate it as a usable in common electronic applications. Model of class-AB amplifier using the DG MOSFET (for audio amplifier) has been designed, fabricated, and thereafter analysed with its frequency and power characteristics. This proposed design with 2 W_{rms} audio amplifier drives a nominal 8 Ω load by a 100 mV_{rms} input signal, for the typical audio frequency range of 20 Hz – 20 kHz.**

***Index Terms*—Class-AB amplifier, double-gate MOSEFT, low power device, microelectronics, transistor, VLSI**

I. Introduction

In signal amplification, common types of amplifiers are class-A, class-B, class-C, class-D, class-E, class-F, class-G, class-AB amplifiers etc. These amplifiers can be realized by topologies, efficiency, power consumption, conduction period, etc. [1]. Class AB amplifier is an improvement on both, the class-A and class-B amplifier by introducing a biasing network [2]-[4]. Class-AB amplifier circuit can incorporate the amplifier as an output stage for a simple audio amplifier. The common audio characteristics such as output power, frequency response, and load regulation are requirement for designing [4], [5].

Since the single-gate (SG) MOSFETs have been used extensively in audio amplifier design, and are not application-specific (such as RF transistors), the introduction of the double-gate (DG) MOSFET will improve its advantages and become a potential replacement for SG MOSFETs [6]-[8]. Wang *et al.* [9] have designed a low-noise programmable gain amplifier (PGA) with fully balanced differential difference amplifier and class-AB output stage. This class-AB output stage in proposed programmable gain amplifier (PGA) can achieve a peak current of 8 mA when PGA has a maximum output swing.

Park *et al.* [10] have investigated the stability problems arising from the undesired coupling between input-feed line and distributed active transformer in a linear power amplifier. Lee *et al.* [11] have designed a CMOS power amplifier with high output power and power added efficiency (PAE) to operate in the avalanche region by increasing supply voltage. They achieved the output power at 1-dB compression point of 30.2 dBm with 34.1% PAE for 2.4 GHz. Ciocoveanu *et al.* [12] have designed a single-stage stacked class-AB power amplifier for 5G and achieved the saturated output power of 17.3 dBm with 39.7% maximum PAE at 24 GHz. The output referred 1-dB compression point is 14.3 dBm and the saturated output power varies from 15.9 dBm to 17.3 dBm for frequency range 22 GHz to 28 GHz. It draws 40 mA from 2.9 V supply and the chip size was 0.35 mm x 0.25 mm.

Saso *et al.* [13] have described class-AB one-stage fully differential amplifier for 0.5-μm CMOS test chip. Anisheh *et al.* [14] have proposed a two-stage class-AB operational transconductance amplifier and fabricated using 180-nm CMOS technology under 1.8 V supply voltage. It exhibits 98 dB DC-gain and 21 MHz unity-gain bandwidth with a 100 pF capacitive load, consuming 3 mW. Wang *et al.* [15] have designed a prototype of two-stage amplifier using a 0.5-μm CMOS technology which exhibits an adjacent-channel leakage power of -35 dBc at the designed output power of 24 dBm, with a power-added efficiency of 29% and a gain of 23.9 dB, demonstrating the potential utility of the design approach for 3GPP WCDMA applications.

Safari and Azhari [16] have presented a novel low voltage, low power class-AB current output stage with high linearity and output impedance. The operation of this current output stage has been verified through HSPICE simulations based on TSMC 0.18-μm CMOS technology parameters. For supply voltage ±0.7 V and bias current 5 μA, it delivers output current 14 mA with high output impedance of 320 MΩ and consumes 29 μW. Bansal and Gupta [17] have presented a two stage amplifier using class-AB mode. This performance was verified by using Mentor Graphics Eldo simulation tool with TSMC CMOS 0.18-μm process parameters. The simulation results of amplifier show that GBW is 9 MHz with power consumption 0.5 mW at ±1.5 V supply. Valero *et al.* [18] have designed and fabricated 1.2 V low

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power rail-to-rail class-AB operational amplifier at 0.18-µm CMOS technology which exhibits 86 dB open loop gain and 97 dB CMRR.

Santos *et al.* [19] have designed and measured a fully integrated 130-nm CMOS multimode power amplifier and achieved a gain between 22.4 dB to 31 dB, and power consumption from 171 mW (low gain mode) to 196.2 mW (high gain mode) and maintains the output power >15 dBm at 2.4 GHz. Mehta *et al.* [20] presented a low power class-AB amplifier, which delivers 51.2 mW peak power with consumption of 0.97 mW total static power. It has unity gain bandwidth of 12.3 MHz, SNR 108 dB, exhibits >12 dB better linearity, >14 dB dynamic range with size 0.16 mm^2 in a standard 65-nm CMOS. Giustolisi *et al.* [21] have designed class-AB CMOS output stages in 65-nm CMOS technology and supplied from 1 V and it was capable to source/sink a maximum output current of 1.5 mA from a quiescent value of 20 µA. It has rail-to-rail input/output operation 5 MHz unity gain frequency and 3.15 V/µs slew-rate for a capacitive load of 100 pF, with a power consumption of 99 µW. Tang *et al.* [22] reported a prototype chip using 55-nm CMOS technology and analyzed that the measured static current consumption of the core circuit is 0.35 mA with a 1.8 V supply voltage, 106 dB signal dynamic range and 55 mW output power with load capacitance from 5 pF to 20 nF.

Akter *et al.* [23] have implemented a closed loop class-AB residue amplifier for pipelined analog to digital converters at 40-nm CMOS technology. It dissipates 9 mW, of which 0.83 mW is consumed in the residue amplifiers. It represents 1.8 times improvement in power efficiency compared to class-AB residue amplifiers. Zhao and Reynaert [24] have implemented a 60 GHz dual-mode Power Amplifier (PA) in 40-nm bulk CMOS technology to boost the amplifier performance at millimeter-wave range. This PA achieved the saturated output power of 17.0 dBm (12.1 dBm) and 1-dB compressed power of 13.8 dBm (9.1 dBm) in the high power (low power) mode, respectively. The power added efficiencies at P_{SAT} and P_{1dB} are 30.3% and 21.6%, respectively for the high power mode.

In this present research work, authors have considered the use of DG MOSFET in audio amplifier design, for its low power and low noise application, better voltage regulation for high to low power, etc. This research paper is organized as follows. Section II discusses the basic circuitries, which are used to design this class-AB amplifier. Section III presents the modelling of class-AB amplifier with DG MOSFET and its various parameters and these are simulated in the Section IV. Section V explains the fabrication of proposed amplifier with DG MOSFET and its testing procedure with results. Finally, Section VI concludes the work and recommends the future aspects.

II. Basic Components Used for Design of Power Amplifier

Here some basics of the models (DG MOSFET and lass-AB amplifier) used in this research work have been discussed. Since these two models have wide specifications and applications, so authors restrict the discussion related to the specific design. Fig. 1 represents the process of this design.

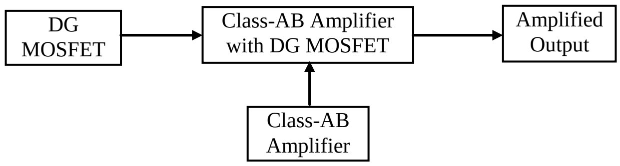


Fig. 1. Process for the design of DG MOSFET based power amplifier.

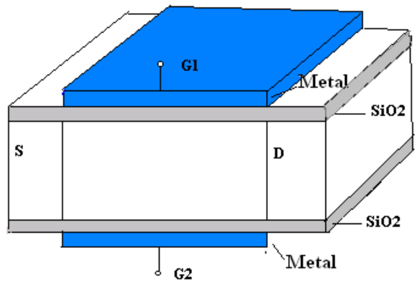


Fig. 2. Schematic of the DG MOSFET [25]. (S: Source, D: Drain, G_1 and G_2: Gate-1 and gate-2, SiO_2: Silicon di-oxide)

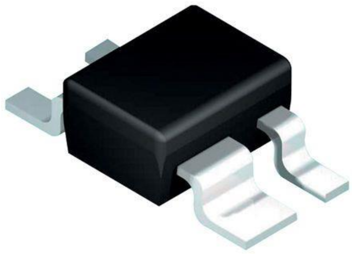


Fig. 3. DG MOSFET structure (BF998) [27].

A. DG MOSFET and Its Differences from SG MOSFET

DG MOSFET has two gate terminals, as opposed to one gate terminal of the SG MOSFET. Fig. 2 shows the ideal planar DG MOSFET. There exist two other types of DG MOSFETs, which are the side-planar (FinFET) and the vertical [25], [26]. Basic DG MOSEFT as BF998 has been used in research work is shown in Fig. 3 [27].

Since there are two gates, which allow the user to control the DG MOSFET from two platforms i.e. each gate. DG MOSFET has advantages over the SG MOSFET such as nearly ideal subthreshold slope, smaller intrinsic gate and junction capacitances, higher ON/OFF current ratio, etc. [28], [29]. Traditional MOSFETs and BJTs have variety of application-specific components such as the IRF540N power MOSFET, which can accommodate a drain to source voltage (from its cut-off region to its saturation region) of 100 V and a drain current of 33 A. To provide a controllable gain for the user, authors have incorporate feedback from the output of the amplifier, with the operational amplifier, utilizing common operational amplifier topologies (such as inverting configuration, non-inverting configuration).

B. Class-AB Amplifiers

The biasing network is used to establish a quiescent current to prevent the transistors from entering into the cut-off mode. This result in each transistor conducting for more than 180° of the input signal, but less than 360°.

This has become a viable option in preventing crossover distortion [4], [30]-[32].

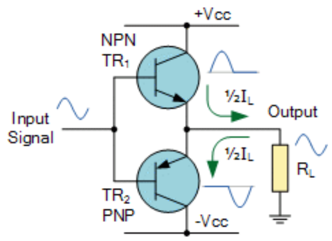


Fig. 4. Basic topology of class-AB amplifier [30].

A three-stage amplifier is usually implemented, consisting of input stage, voltage amplification stage, and output stage (Fig. 4). The output stage resembles the class-AB amplifier topology. The following parameters have been analysed to quantify the DG MOSFET based class-AB amplifier's performance, in terms of its frequency response and its ability to drive a load, in comparison to SG MOSFET.

The operational amplifier allows for a wide use of supply voltages. This will allow flexibility in the design of the circuit [33]. Overall gain control is less complex of the driver stage and can be adapted to the overall gain of the amplifier itself.

Magnitude response and Bandwidth – Ideally, an amplifier amplifies all signals equally. However, in application, most amplifiers need a response of about 20 Hz to 20 kHz, to ensure all audible signals are catered for. Since authors are considering the overall frequency response in this research work, an output filter has not been added to analyse the full bandwidth of the amplifier. The comparison of both (SG and DG MOSFET based) amplifier's performance in the frequency domain allows to analyse the behaviour of amplifiers across the entire frequency spectrum [4]-[8], [34]. The gain for each frequency component may be calculated using $20\log(V_{out}/V_{in})$.

Phase Response – The phase response of an amplifier allows analysing its stability [5]-[8]. In this work authors have a look at the alignment of the poles of the amplifier, in accordance of the –20 dB/decade slopes. The phase delay θ, for each frequency may be calculated as $\Delta t f\times 360°$, where Δt is time delay in seconds, and f is input signal frequency.

Output Impedance – It refers to the ability (or inability) of the amplifier to deliver current to a load [25], [32]-[34]. This enables to identify suitable amplifier, which is designed using the DG MOSFET and the SG MOSFET [4], [35], [36]. The output impedance (R_O) is calculated as:

$$R_o = R_L\left(\frac{V_{open}}{V_L} - 1\right) \tag{1}$$

where V_{open} and V_L are the open-circuit voltage and voltage across load impedance (R_L), respectively.

Supply voltage vs gain vs frequency – These parameters allows to analyse the low power potential of both, the SG MOSFET and DG MOSFET based amplifiers. It will allow users to determine the suitable specifications of further developments of the amplifier itself, and its integration in existing systems such as audio systems and RF systems [4], [34]-[36].

Output Voltage vs Supply Voltage – This parameter allows to determine the output power of both amplifiers under load [4]-[8], [34]-[36]. In this research work design of the class-AB amplifier, using either MOSFET, authors have investigated its ability to drive a speaker for 1 W designed specification.

III. Proposed Design of Class-AB Amplifier with the DG MOSFET

The 2N7000 N-Channel enhancement mode MOSFET has been chosen as a SG MOSFET. The equivalent SG MOSFET based amplifier is shown in Fig. 5. This provides an equivocal testing background to establish a comparison between both MOSFETs [37], [38]. To utilize the DG MOSFET, first it should be considered the way to dive the gates of each MOSFET. The oxide layers of the DG MOSFET can also be considered as identical [39]-[43].

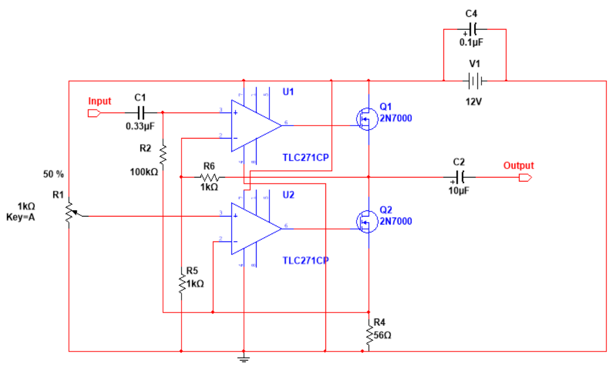


Fig. 5. Circuit design of class-AB amplifier using SG MOSFET.

If one had chosen a DG MOSFET, with differing oxide-layers, this is known as an asymmetrical gate drive. The class-AB amplifier is also an improvement of the push-pull amplifier, by establishing a quiescent current. The push-pull arrangement has NPN transistor (to source the output current for positive half-cycles) and the PNP transistor (to sink the output current for negative half-cycles). Considering input filtering (simple RC high-pass filter) the cut-off frequency can be calculated as $f_c = 1/2\pi RC$ [44].

The full circuit design is shown in Fig. 6. The E12 values of the capacitor and resistor are chosen for this cut-off frequency, R_1 = 100 kΩ, C_1 = 0.33 µF. The supply voltage V_{CC} 12 V, for the circuit construction, and a drain current is 23 mA for transistor M_1. The M_1 is the DG MOSFET that sources the load current. This drain current has been chosen is 30 mA for MOSFET. The datasheet bounds a drain current of 24 mA, given certain drain to source voltages, gate to source voltages and gate voltages. Given these parameters, resistor R_8 is a current limiting resistor, provide a voltage drop towards the drain. Assuming a drain current of 23 mA, the voltage at the drain terminal is $V_{D1} = V_{CC} - I_D R_1$ = 9.7 V. Authors have considered V_{DS} as 7.4 V to accommodate any threshold voltage drop across the drain and source. Typical threshold voltages are 0.6 V to 1 V. Since, V_{D1} is 9.7 V, V_{DS1} is 7.4 V, so $V_{S1} = V_{D1} - V_{DS1} = 2.3$ V.

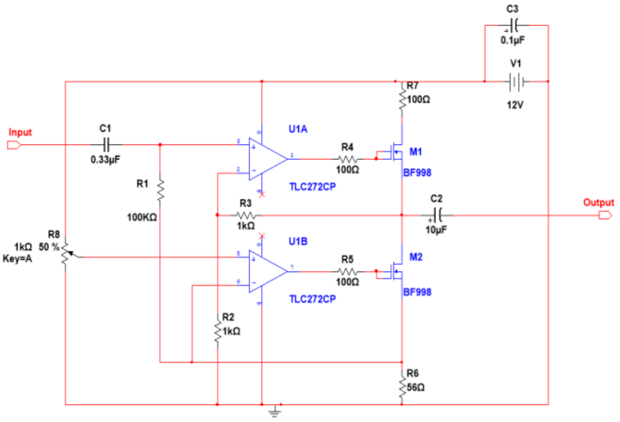


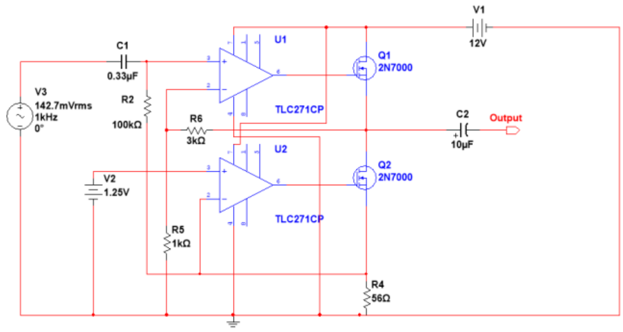
Fig. 6. Complete circuit design of class-AB amplifier using DG MOSFET.

The drain of M_2 is connected to the source of M_1, which also resembles the output node. Thus $V_{D2} = 2.3$ V. Assuming M_2 sinks 90% of the drain current from M_1, $I_{D2} = 21$ mA. From Fig. 6 of the circuit, the source resistance R_2 provides a low source voltage, while maintaining a higher gate to source voltage ($V_{(G1,\,2\text{-}S)}$). A higher $V_{(G1,\,2\text{-}S)}$ allows for the formation of a wider channel between the source and drain. The drain to source voltage (V_{DS}) may be chosen as 1 V to 2 V. Here the selected drain to source voltage is 1.2 V. Thus $V_{S2} = I_{D2}R_S$, so $R_6 = R_S = 57.14\ \Omega$. Therefore, 56 Ω has been selected.

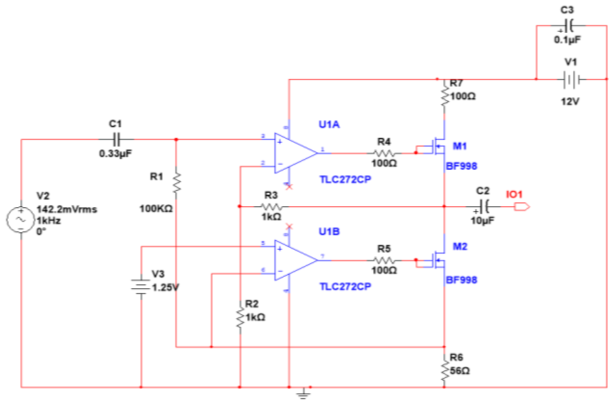
Resistors R_4 and R_5 are taken as 100 Ω, to provide current limiting to the gate of the MOSFETs. The operational amplifier A_1 with open loop gain 2 V/V has been configured as a non-inverting operational amplifier. This will allow the user to set the required open-loop gain of the amplifier. The open-loop gain (A_V) is set by R_2 and R_3, and given as $(1+R_3/R_2)$.

The operational amplifier (U1A) has been configured as an inverting amplifier. This produces a phase-inversion of the input signal, driving DG MOSFET (M_2). The R4, as previously noted, is 100 Ω, and R_6 is the source resistance of 56 Ω. The biasing voltage used on the non-inverting pin of operational amplifier (U1B), can be made adjustable to remove distortion by increasing the current drive from the operational amplifier, it provide a larger output voltage swing. The range of the biasing voltage has been investigated in Multisim, to provide the adequate voltage to the operational amplifier for each input voltage range. The value of 10% V_{CC} (=1.2 V), provides adequate current drive to the DG MOSFET, for an input signal of less than 200 mV. When an input signal of 200 mV is used, distortion can be seen on the lower peak of the output sinusoid.

Including the driver-stage and output stage using the DG MOSFET, the full circuit implementation of the class-AB amplifier uses the TLC272 operational amplifier. It is high-speed, low-power, and operates at single-rail supply. Decoupling capacitors are used across the power supply and at the output terminal of the amplifier. Capacitor C_3 has been chosen as 0.1 µF to reduce high-frequency noise from the power supply. Capacitor C_2 has been chosen to reduce excess charge from the output by providing a reservoir for charge.



(a)



(b)

Fig. 7. (a) SG MOSFET and (b) DG MOSFET based class-AB amplifier with AC input signal.

IV. Analysis and Comparison of SG MOSFET and DG MOSFET based Class-AB Amplifier

The Fig. 7 has been simulated using the AC sweep function to perform a full analysis of the designed amplifier. This allows viewing the entire response of the designed class-AB amplifier with DG MOSFET to a frequency sweep range 1 Hz to 10 MHz. The frequency responses for the SG MOSFET and DG MOSFET based amplifier have been shown in Fig. 8.

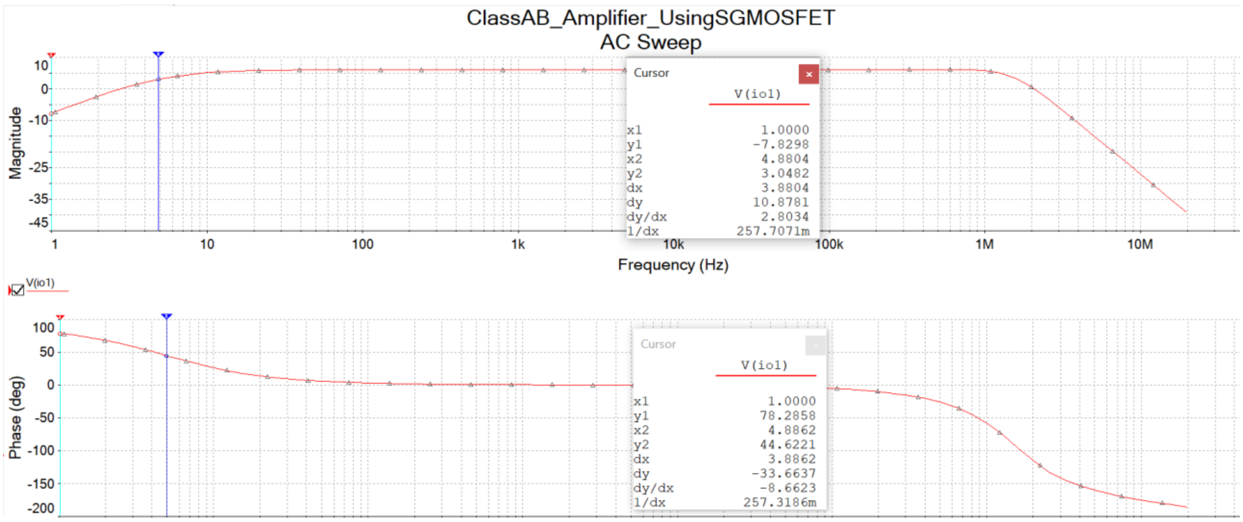
A. Frequency Response

Analysing the SG MOSFET based amplifier, the midband and –3 dB gains is identical to the DG MOSFET based amplifier. However, as it has been observed in Fig. 8, that f_H is approximately 1.609 MHz, showing the bandwidth of DG MOSFET superior in the amplifier application.

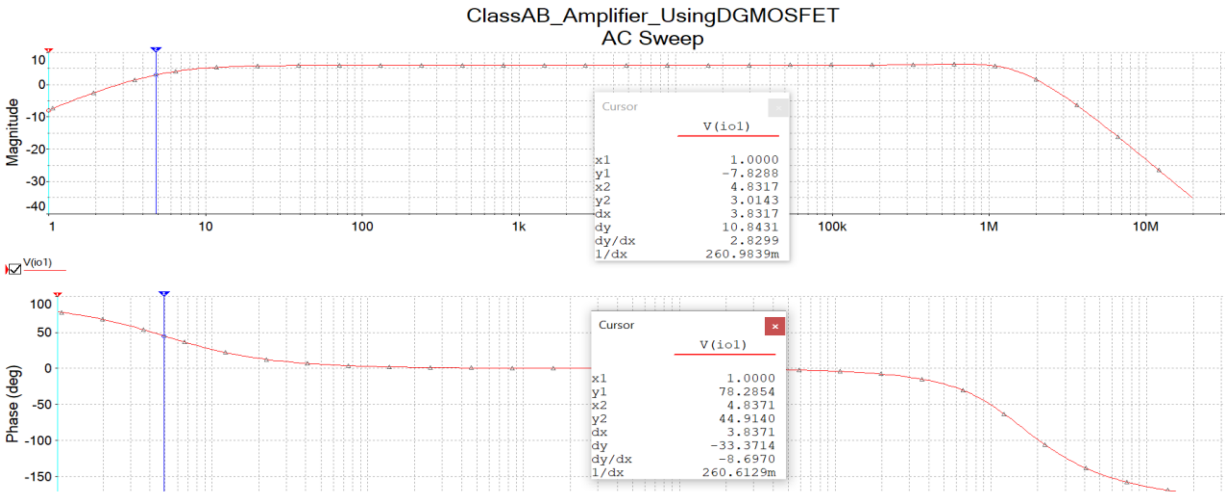
For the DG MOSFET based amplifier the f_L (which is the –3 dB gain at the lower slope of the frequency response) is noted as 3.031 dB (at marker y_2) in Fig. 8 (b) and the lower cut-off frequency (f_L) is 4.8 Hz and the higher cut-off frequency (f_H) is approximately 1.719 MHz (shown by the marker x_2) in Fig. 8 (d). The lower cut-off frequency is determined by the inclusion of input high pass RC filter at the input. Thus, the observed bandwidth is 1.719 MHz.

B. Phase Response

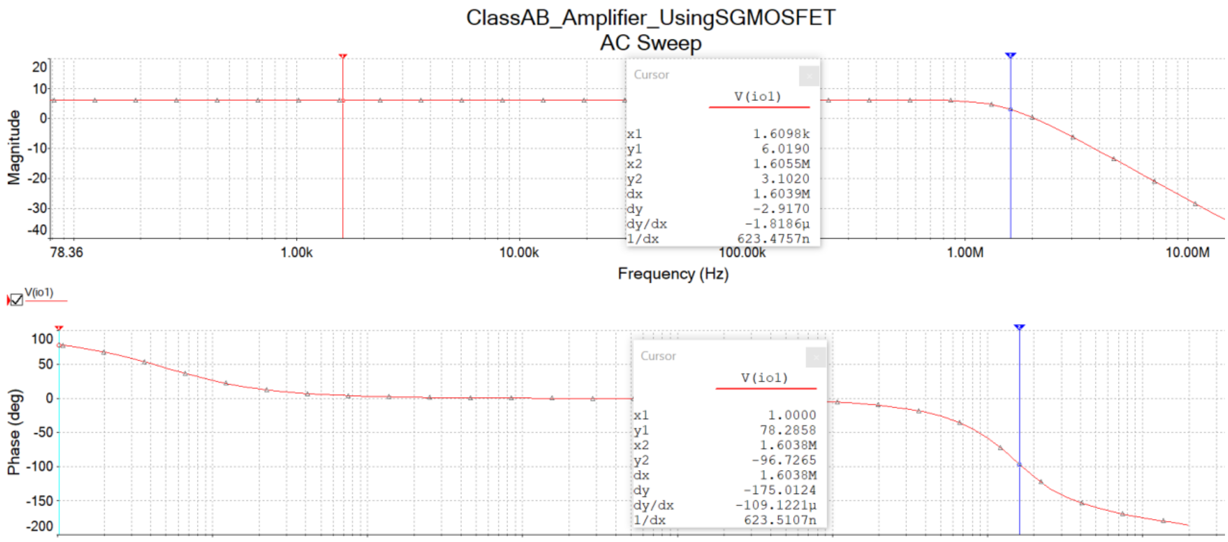
Coupled with the magnitude response, the phase response provides an indication of the stability of the system as shown in Fig. 8. To drive the DG MOSFET using operational amplifiers, analysis of their outputs in terms of the phase response have been considered.



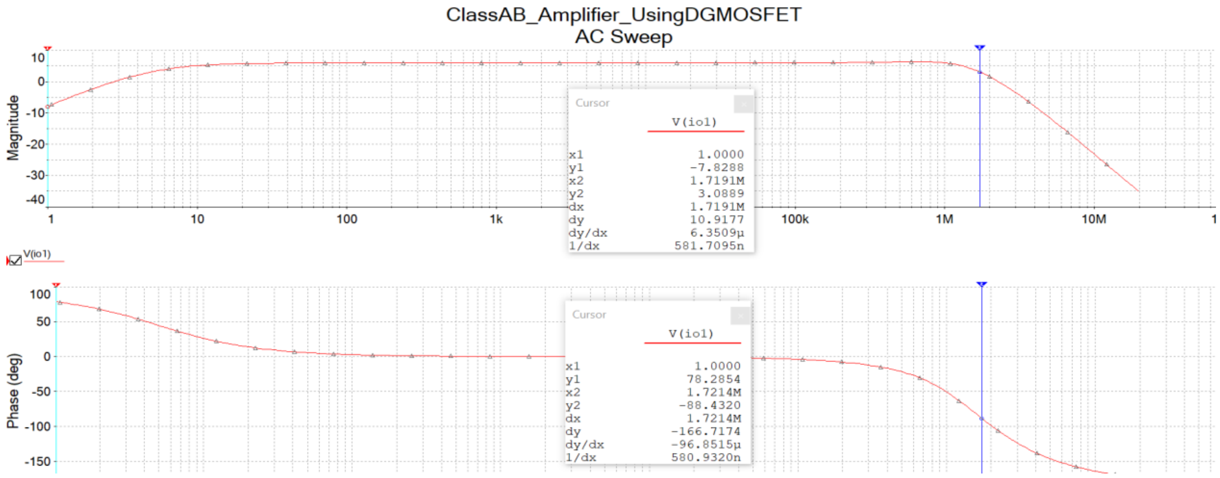
(a) Lower cut-off frequency for SG MOSFET based class-AB amplifier



(b) Lower cut-off frequency for DG MOSFET based class-AB amplifier



(c) Higher cut-off frequency for SG MOSFET based class-AB amplifier



(d) Higher cut-off frequency for DG MOSFET based class-AB amplifier

Fig. 8. Analysis of magnitude and phase response of designed amplifier.

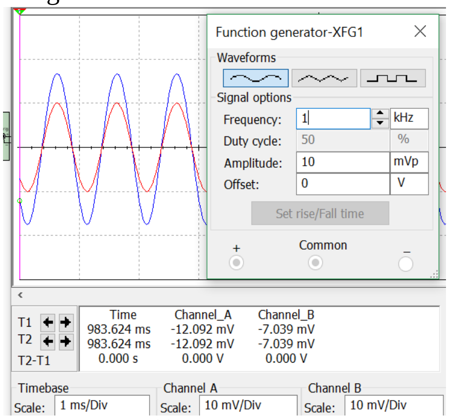
The first pole of both amplifier circuits occurs at approximately 4 Hz, which is between 1 Hz to 1 kHz. For each amplifier, there are two noticeable phase shifts, occurring at 44 ° for the first pole, and –88 ° and –96 ° for the DG MOSFET and SG MOSFET amplifiers, respectively. For both amplifier constructions, at f_{180} (phase shift at –180 °), the mid-band gain is less than unity. However, for the DG MOSFET based amplifier, one may observe a larger phase margin than the SG MOSFET based amplifier, where the phase margin is the phase shift, required to cause instability. This instability incurs a phase shift of -180 °. The phase margin, for the DG MOSFET amplifier is –88 °+180 °=92 °, and SG MOSFET amplifier is –96 °+180 °=84 °. Typical phase delays are denoted to be approximately –45 ° for the first pole, and –135 ° for the second pole, for a two-stage amplifier.

However, since a phase-inverting amplifier has been designed to accommodate the N-channel MOSFET for the lower portion of the input signal, the second pole occurs at phase of ($\theta_{\text{non-inverted}}$+180 °). In conclusion, the DG MOSFET amplifier is inherently more stable than the SG MOSFET amplifier.

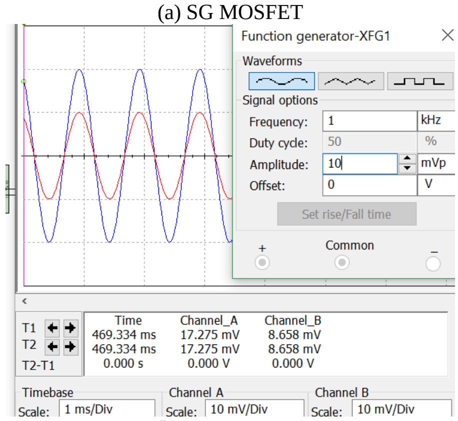
C. Gain Analysis

For the design of Fig. 7, both amplifiers using supply voltage of 6.5 V to analyse the lower limit of the effect. It has been observed that the DG MOSFET amplifier is able to preserve its gain for input signals of 10 mV and 100 mV in Fig. 9 (b) and Fig. 9 (d), respectively. However, for 100 mV_{pk} signal at V_{cc} = 6.5V, distortion can be observed using the SG MOSFET amplifier in Fig. 9 (a) and Fig. 9 (c). Therefore, the amplifier cannot preserve its gain for small signals with a smaller supply voltage.

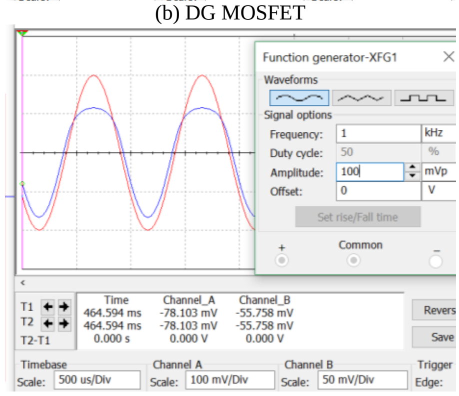
Observing the preservation of the gain (when the supply voltage is varied) allows one to demonstrate the ability of the amplifier to be applied in a range of supply voltages. From the simulation as shown in Fig. 9, the gains for both amplifiers are preserved for supply voltage range of 7 V to 11 V. For the SG MOSFET amplifier, output distortion is present for an input voltage of 100 mV, and a supply voltage of 6.5 V. However, the DG MOSFET amplifier is able to preserve its gain at this supply voltage.



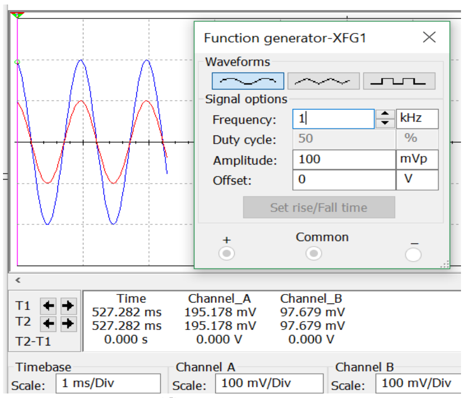
(a) SG MOSFET



(b) DG MOSFET



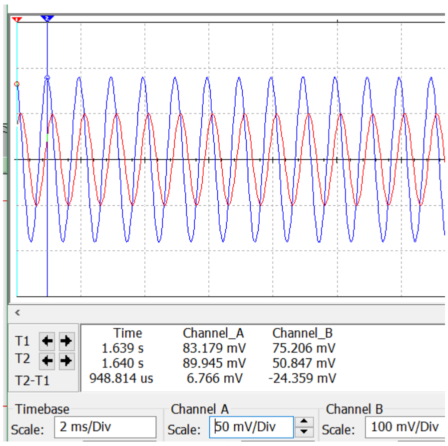
(c) SG MOSFET



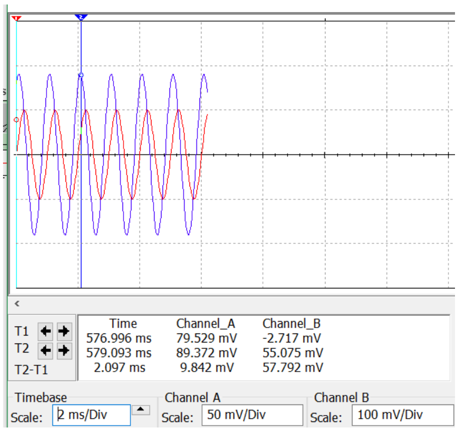
(d) DG MOSFET

Fig. 9. Gain preservation at V_{cc} = 6.5 V for the designed class-AB amplifier circuit at 10 mVpk signal (a) and (b), and at 100 mVpk signal (c) and (d).

D. Output Impedance



(a)



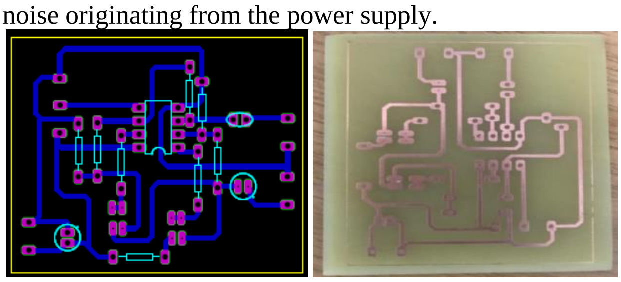
(b)

Fig. 10. Output waveform with the load for (a) SG MOSFET and (b) DG MOSEFT based class-AB amplifier.

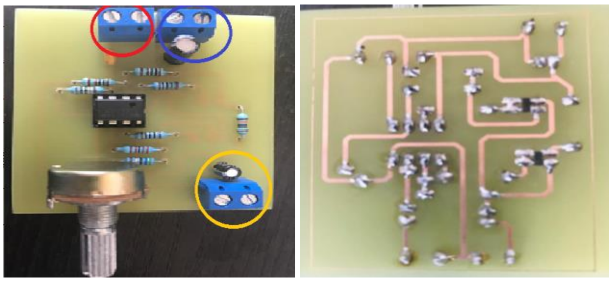
In the simulation of both amplifiers, 8 Ω loads have been used to close the circuit loop. This can be seen as open-loop voltage V_{open}=100 mVpk, closed-loop voltage 89 mVpk. The output resistance for both amplifier models has been calculated using (1) as 0.98 Ω. As previously mentioned, an amplifier that can be designed with smaller output impedance is more desirable amplifier. From the simulation results of both amplifier models for the class-AB amplifier (SG and DG), authors have observed an identical output impedance. The output waveforms with the load for SG MOSFET and DG MOSEFT based class-AB amplifier have been shown in Fig. 10.

V. Fabrication of Class-AB Amplifier with DG MOSFET and It's Parametric Analysis

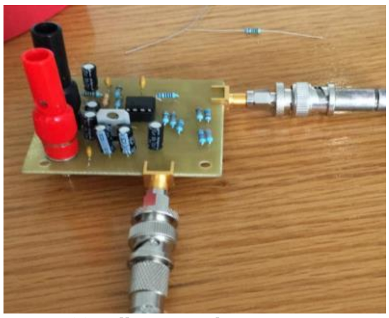
Using Proteus software for the improved Printed Circuit Board (PCB) design functionality, a circuit design has been drawn for the DG MOSFET amplifier [45]-[49]. Implementing a design to obtain PCB layout, this has been observed in Fig. 11. Terminal blocks have been used as power input, signal input, signal output, and strategically placed at the edge of the board to provide ease of access for the user. A dual operational amplifier is used as it contains two operational amplifier chips [50]. This results in additional PCB traces and offers modularity, resulting in one operational amplifier IC being used. A PCB mount potentiometer has been used for the voltage reference of A_2 to the non-inverting pin. A 0.1 µF decoupling capacitor has been used for potential noise originating from the power supply.



(a) PCB layout (b) Etched PCB using Ferric Chloride



(c) Full PCB implementation showing signal input (red), signal output (blue), and input power (yellow). (d) Fabrication on PCB (surface mount DG MOSFET)



(e) Full PCB implementation.

Fig. 11. Fabrication process of the DG MOSFET based class-AB amplifier.

A PCB revision was performed and shown in Fig. 11(e). The changes to the original PCB design include the usage of a ground pour, where the entire copper plane is being used as ground plane, except for signal traces. It has various advantages such as reduced size, convenient ground path for components, shorter return paths for signals, avoids ground loops, etc. Capacitors of 100 nF, 1 µF, and 10 µF (which can be seen as C_6, C_7, C_8 and C_9, C_{10}, C_{11} in Fig. 12 (a)) have been used in parallel to provide adequate decoupling for low to medium frequencies, which could originate from power supply noise. A 100 nF capacitor is used to provide decoupling of the operational amplifier and placed close to the supply voltage pin of the component (C_2). A 12 V regulator was used to provide a stable voltage source for circuit. However, the dropout voltage of the regulator is noted as 2.5 V. This stipulates an input voltage of 14.5 V to supply the regulated 12 V output.

Decoupling capacitors have been used at the input and output of the regulator, in the aforementioned configuration. Shielded connectors have been used (Amphenol SMA connectors J_1 and J_2 in the PCB layout), as input and output signal source and banana connectors (binding posts) were used as power connectors, and strategically placed at the edge of the board. A voltage reference diode has been used to replace the potentiometer in the original circuit design and it is biased at 1.25 V.

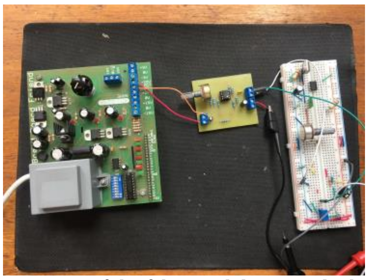
The DG MOSFET is a highly delicate and fragile component, attributed to its SMD nature and use in circuital design. For prototyping ease, SOT-143 adapters have been used. The 2N7000 SG MOSFET used is a more robust transistor.

The SG MOSFET and DG MOSFET based amplifiers have been compared in terms of frequency response and bandwidth. It compares the performance across the frequency band and the limitations of usage and where attenuation of the output signals may begin), power usage and efficiency and the output voltage and current capability in the designed device. Theoretically, the design process carried out was performed to accommodate the constraints of the DG MOSFET [51], [52].

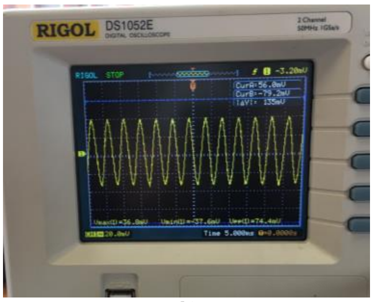
A. *Magnitude Response, Bandwidth, and Phase Response*

Simulation results have shown a larger bandwidth exhibited by the DG MOSFET compared to the SG MOSFET. This has been verified by prototyping results, as the DG MOSFET amplifier exhibits a higher f_L (approximately 70 Hz) also exhibits a higher f_H (in excess of 10 MHz) in Fig. 12 (b). The typical mid-band gain of 6.03 dB (2 V/V), as intended, at the beginning of the circuital design for simplicity is preserved for the DG MOSFET, for both 10 mVpk and 100 mVpk signals. It also exhibits a larger mid-band gain for 10 mVpk input signal. However, the SG MOSFET exhibits a larger flat response for both 10 mVpk and 100 mVpk signals. Therefore, the DG MOSFET amplifier is well suited to high-frequency low-voltage applications.

In Fig. 8, the simulation results show that DG MOSFET amplifier exhibits more stability, and is less capable of oscillating, as the phase margin is larger, than the SG MOSFET amplifier. Observing the prototype results of the both amplifier models, the phase response of both amplifiers does not exhibit a typical phase response of an amplifier. It may conclude, from the phase response, that the amplifier model is highly stable.



(a) Measurement setup of the fabricated device and other equipment.



(b)

(c)

Fig. 12. Measurement stages for the various parameters of the fabricated devices.

B. *Open Loop Gain vs Frequency*

Simulation results (Fig. 9) exhibit the low power ability of the DG MOSFET amplifier, the preservation of the amplifier gain, for both input voltage signals of 10 mVpk and 100 mVpk at supply voltage 6.5 V. Whereas, the SG MOSFET amplifier exhibits distortion for input voltage signal 10 mVpk. However, in prototype testing, the DG MOSFET amplifier exhibits a signal for supply voltage up to 10.48 V (supply voltage used in circuital design) as shown in Fig. 12(c). Therefore, it can be conclude that the SG MOSFET amplifier is less suited to low power application and shows a flexible architecture.

C. *Output Voltage vs Supply Voltage*

In driving to 8 Ω load, the simulated output voltages ranged in nanovolts does not provide a suitable current drive. In addition, of the voltage buffer, the current and voltage drive drastically increased, as the DG MOSFET amplifier boasts an output voltage and current of 43 mV and 5.88 mA, respectively. The SG MOSFET amplifier boasts an output voltage and current of 500 mV and 0.625 A, respectively. The resulting output power from the DG MOSFET amplifier is 0.20 W and from the SG MOSFET amplifier is 0.31 W. By this design, it has been confirmed that the SG MOSFET amplifier has a larger power output, in similar design conditions, as the DG MOSFET amplifier.

VI. CONCLUSIONS AND FUTURE RECOMMENDATIONS

The design of the DG MOSFET based class-AB amplifier has been implemented, using comprehensive circuital design techniques, methods, and components. The DG MOSFET is superior in power applications, as its ability to deliver noticeable output power has been highlighted in extensive testing with frequency analysis over a wide frequency range, than the SG MOSFET. The DG MOSFET poses a favourable frequency response to applications, outside the applied audio frequency band of 20 Hz to 20 kHz.

The designed amplifier circuit provides further design and research into transistor manufacturing, usage, and a next generation implementation model to follow. Several design constraints acknowledged in the designing of the class-AB amplifier can be realized in further amplifier design and may attribute future design work to the analysis and the design of this class-AB amplifier.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Suvashan Pillay (SP) and Viranjay M. Srivastava (VMS) conducted this research; SP designed and fabricated the circuit after that analyzed the data and wrote the paper; VMS has verified the result with the designed circuit; all authors had approved the final version.

REFERENCES

[1] Nathan O. Sokal, "RF power amplifiers, classes A through S - How they operate, and when to use each," in *Professional Program Proceedings, Electronic Industries Forum of New England*, Boston, MA, USA, 6-8 May 1997, pp. 179-252.

[2] G. Giustolisi, G. Palumbo, and S. Pennisi, "Class-AB CMOS output stages suitable for low-voltage amplifiers in nanometer technologies," *Microelectronics Journal*, vol. 92, pp. 1-7, Oct. 2019.

[3] S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees, and J. Benedikt "On the continuity of high efficiency modes in linear RF power amplifiers," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 10, pp. 665-667, Oct. 2009.

[4] B. Cordell, *Designing Audio Power Amplifiers*, 1st Ed., McGraw Hill, 2010.

[5] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*, Norwood: Artech House, 2002.

[6] J. L. Dawson and T. H. Lee, *Feedback Linearization of RF Power Amplifiers*, New York: Springer Publications, 2004.

[7] A. S. Sedra and K. C. Smith, *Microelectronic Circuits: Theory and Applications*, 7th Ed., Oxford University Press, 2014.

[8] V. M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of double-gate MOSFET over single-gate MOSFET for RF switch," *Microelectronics Journal*, vol. 42, no. 3, pp. 527-534, 2011.

[9] J. Wang, Z. Zhu, S. Liu, and R. Ding, "A low-noise programmable gain amplifier with fully balanced differential difference amplifier and class-AB output stage," *Microelectronics Journal*, vol. 64, pp. 86-91, 2017.

[10] J. Park, C. Lee, and C. Park, "Study of stability problems due to undesired coupling of a RF power amplifier using a distributed active transformer," *Microelectronics Journal*, vol. 46, pp. 1046-1052, 2015.

[11] C. I. Lee, W. C. Lin, and Y. T. Lin, "A 2.4 GHz high output power and high efficiency power amplifier operating at inductive breakdown in CMOS technology," *Microelectronics Journal*, vol. 45, pp. 449-453, 2014.

[12] R. Ciocoveanu, R. Weigel, A. Hagelauer, A. Geiselbrechtinger, and V. Issakov, "5G mm-wave stacked class AB power amplifier in 45 nm PD-SOI CMOS," in *Proc. Asia-Pacific Microwave Conference (APMC)*, Kyoto, Japan, 2018, pp. 147-149.

[13] J. M. Saso, A. J. Lopez-Martin, M. P. Garde, and J. Ramirez-Angulo, "Power-efficient class AB fully differential amplifier," *IET Electronics Letters*, vol. 53, no. 19, pp. 1298-1300, 2017.

[14] S. M. Anisheh, H. Abbasizadeh, H. Shamsi, C. Dadkhah, and K. Y. Lee, "98-dB gain class-AB OTA with 100 pF load capacitor in 180-nm digital CMOS process," *IEEE Access*, vol. 7, pp. 17772-17779, 2019.

[15] C. Wang, M. Vaidyanathan, and L. E. Larson, "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 1927-1937, November 2004.

[16] L. Safari and S. J. Azhari, "A novel low voltage very low power CMOS class AB current output stage with ultrahigh output current drive capability," *Microelectronics Journal*, vol. 43, pp. 34-42, 2012.

[17] U. Bansal and M. Gupta, "Two stage class AB-AB amplifier using FGMOS for low voltage operation and SSF for frequency compensation," *Int. J. Electronics Communication (AEÜ)*, vol. 73, pp. 59-67, 2017.

[18] M. R. Valero, N. Medrano, S. Celma, and B. Calvo, "A high-performance 1.2V–99 μW rail-to-rail CMOS class AB amplifier," *Microelectronics Journal*, vol. 46, pp. 96-102, 2015.

[19] E. L. D. Santos, M. A. Rios, L. Schuartz, *et al*., "A fully integrated CMOS power amplifier with discrete gain control for efficiency enhancement," *Microelectronics Journal*, vol. 70, pp. 34-42, 2017.

[20] N. Mehta, J. H. Huijsing, and V. Stojanovic, "A 1-mW class-AB amplifier with −101 dB THD+N for high-fidelity 16 Ω headphones in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 4, pp. 948-958, April 2019.

[21] G. Giustolisi, G. Palumbo, and S. Pennisi, "Class-AB CMOS output stages suitable for low-voltage amplifiers in nanometer technologies," *Microelectronics Journal*, vol. 92, pp. 1-7, 2019.

[22] F. Tang, S. Li, B. Wang, A. Bermak, X. Zhou, and S. Hu, "A low power class-AB audio power amplifier with dynamic transconductance compensation in 55 nm CMOS process," *IEEE Trans. on Circuits and Systems—I: Regular Papers*, vol. 63, no. 9, pp. 1360-1369, Sep. 2016.

[23] M. S. Akter, R. Sehgal, F. van der Goes, K. A. A. Makinwa, and K. Bult, "A 66-dB SNDR pipelined split-ADC in 40-nm CMOS using a class-AB residue amplifier," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 10, pp. 2939-2950, Oct. 2018

[24] D. Zhao and P. Reynaert, "A 60-GHz dual-mode class AB power amplifier in 40-nm CMOS" *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2323-2327, Oct. 2013.

[25] V. M. Srivastava and G. Singh, *MOSFET Technologies for Double-Pole Four-Throw Radio-Frequency Switch*, Switzerland: Springer International Publishing, 2014.

[26] R. T. Cakici and K. Roy, "Analysis of options in double-gate MOS technology: A circuit perspective," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3361-3368, Dec. 2007.

[27] *Discrete Semiconductors*, BF998; BF998R Silicon N-channel dual-gate MOS-FETs, Datasheet, Philips Semiconductor, Aug. 1996.

[28] A. Yesayan, F. Jazaeri, and J. M. Sallese, "Charge-based modeling of double-gate and nanowire junctionless FETs

including interface-trapped charges," *IEEE Trans. on Electron Devices*, vol. 63, no. 3, pp. 1368-1374, March 2016.

[29] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2861-2869, Dec. 2001.

[30] Electronics Tutorials. [Online]. Available: https://www.electronics-tutorials.ws/amplifier/class-ab-amplifier.html

[31] J. R. Angulo, R. G. Carvajal, J. A. Galan, and A. L. Martín, "A free but efficient low-voltage class-AB two-stage operational amplifier," *IEEE Trans. on Circuits and Systems—II: Express Briefs*, vol. 53, no. 7, pp. 568-571, July 2006.

[32] D. Self, *Audio Power Amplifier Design Handbook*, 5th Ed. New York: Focal Press, Taylor and Francis, 2013.

[33] R. Gayakwad, *Op-Amps and Linear Integrated Circuits*, 4th Ed. Pearson, 2000.

[34] Application Report SLOA068, *Guidelines for Measuring Audio Power Amplifier Performance*, Texas Instruments, October 2001, pp. 1-28.

[35] B. Witte, "Voltage transfer: Give me low output impedance," *EDN Network*, Nov. 2018.

[36] G. A. R. Mora and R. Stair, "A low voltage, rail-to-rail, class AB CMOS amplifier with high drive and low output impedance characteristics," *IEEE Trans. on Circuits and Systems—II: Analog and Digital Signal Processing*, vol. 48, no. 8, pp. 753-761, Aug. 2001

[37] P. R. Surkanti and P. M. Furth, "Converting a three-stage pseudoclass-AB amplifier to a true-class-AB amplifier," *IEEE Trans. on Circuits and Systems—I: Express Briefs*, vol. 59, no. 4, pp. 229-233, April 2012.

[38] S. J. C. H. Theeuwen and J. H. Qureshi, "LDMOS technology for RF power amplifiers," *IEEE Trans. on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1755-1763, June 2012.

[39] J. E. Pakaree and V. M. Srivastava, "Realization with fabrication of double-gate MOSFET based differential amplifier," *Microelectronics Journal*, vol. 91, pp. 70-83, Sep. 2019.

[40] S. K. Dargar and V. M. Srivastava, "Design and analysis of IGZO thin film transistor for AMOLED pixel circuit using double-gate tri active layer channel," *Heliyon*, vol. 5, no. 4, pp. 1-15, April 2019.

[41] U. Vishnoi and G. Noll, "Area-and energy-efficient CORDIC accelerators in deep sub-micron CMOS Technologies," *Advances in Radio Science*, vol. 10, pp. 207-213, Sept. 2012.

[42] V. M. Srivastava, "Circuit perspective of terahertz double-gate MOSFET circuits for switch," in *Proc. 12th IEEE India Int. Conference (INDICON)*, Delhi, 2015, pp. 1-4.

[43] Q. Chen, K. A. Bowman, E. M. Harrell, and J. D. Meindl, "Double jeopardy in the nanoscale court [MOSFET modeling]," *IEEE Circuits and Devices Magazine*, vol. 19, no. 1, pp. 28-34, Jan. 2003.

[44] J. M. Fiore, *Operational Amplifiers and Linear Integrated Circuits: Theory and Application*, Jaico Publishing House, 2002.

[45] Proteus software. [Online]. Available: https://www.labcenter.com/pcb/

[46] H. Sood, V. M. Srivastava, and G. Singh, "Small signal modeling of scaled double-gate MOSFET for GHz applications," *J. of Microelectronics, Electronic Components and Materials*, vol. 47, no. 1, pp. 14 - 23, 2017.

[47] S. K. Ghandhi, *VLSI Fabrication Principles: Silicon and Gallium Arsenide*, Wiley, 1994.

[48] D. A. Pucknell, *Basic VLSI Design*, Prentice Hall, 1994.

[49] S. M. Sze, *VLSI Technology*, 2nd Ed. McGraw-Hill Education (India) Pvt Limited, Oct. 2003.

[50] SLOS090D, *TLC271, TLC271A, TLC271B LinCMOS Programmable Low-power Operational Amplifiers*, Texas Instruments, March 2001, pp. 1-69.

[51] J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 3rd Ed. Springer, 2004.

[52] A. Amara and O. Rozeau, *Planar Double-Gate Transistor: From Technology to Circuit*, Springer, 2009.

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