CMOS Operational Floating Current Conveyor Circuit for Instrumentation Amplifier Application

Fahmi Elsayed, Mostafa Rashdan, and Mohammad Salman
College of Engineering and Technology, American University of the Middle East, Kuwait
Email: {fahmi.el-sayed; mostafa.rashdan; mohammad.salman}@aum.edu.kw

***Abstract*—This paper presents a fully integrated CMOS Operational Floating Current Conveyor (OFCC) circuit. The proposed circuit is designed for instrumentation amplifier circuits. The CMOS OFCC circuit is designed and simulated using Cadence in TSMC 90 m technology kit. The circuit aims at two different design goals. The first goal is to design a low power consumption circuit (LBW design) while the second is to design a high bandwidth circuit (HBW design). The total power consumption of the LBW design is 1.26 mW with 30 MHz bandwidth while the power consumption of the HBW design is 3 mW with 104.6 MHz bandwidth.**

***Index Terms*—Analog signal processing, CMOS, low power, low voltage, operational floating current conveyor, VLSI**

I. Introduction

Current conveyors are commonly used in different applications such as instrumentation amplifier circuits [1], Operational Transconductance Amplifiers (OTA), analog filter designs and current multipliers [2], [3].

The Operational Floating Current Conveyor (OFCC) is a five-port general-purpose analog building block. It has transmission properties similar to the Operational Floating Conveyor (OFC) [4], but with an additional high output impedance terminal which allows more maneuvering of the device capabilities than the Current Feedback Amplifier (CFA) and OFC. Similar to both the OFC and CFA circuits, the OFCC has very low input impedance compared to the current conveyor circuits. Better than both OFC and CFA circuits, the OFCC circuit introduces better flexibility as it introduces an extra output terminal.

A current-mode Wheatstone bridge, instrumentation amplifier, universal filter, and readout circuit for biomedical sensors are examples of the OFCC applications [5]-[7]. Fig. 1 shows the basic building block diagram of the OFCC circuit.

The circuit has two input terminals. The first input terminal X is a low impedance current input terminal. The second input voltage terminal Y has high input impedance, as the OFCC has a current feedback amplifier at its input stage. On the other hand, the OFCC has three output terminals W, Z+, and Z-. The W terminal is the output voltage terminal of the current feedback amplifier, and has low output impedance. Both Z+ and Z- are high impedance output current terminals. The Z+ terminal has an output current equal in phase and magnitude to the W terminal. For the Z- terminal, it has an output current which has the same magnitude as the W terminal's current but is 180˚ out of phase.

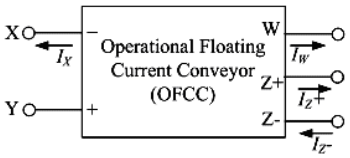

Fig. 1. OFCC block diagram.

The following matrix equation explains the operation of the exact OFCC circuits:

$$\begin{bmatrix} i_y \\ v_x \\ v_w \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ h_v & 0 & 0 & 0 & 0 \\ 0 & -Z_t & 0 & 0 & 0 \\ 0 & 0 & h_{i1} & 0 & 0 \\ 0 & 0 & -h_{i2} & 0 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ i_w \\ v_{z+} \\ v_{z-} \end{bmatrix}. \quad (1)$$

where h_v is the voltage tracking percentage and it is equal to $(1-\epsilon_v)$, where ϵ_v *is* the voltage tracking error. Both h_{i1} and h_{i2} are the current tracking percentages for both the Z+ and Z- terminals respectively. The coefficient h_{i1} is equal to $(1-\epsilon_{i+})$ and h_{i2} is equal to $(1-\epsilon_{i-})$, where ϵ_{i+} and ϵ_{i-} are the current tracking errors of the high output impedance terminals, Z+ and Z- respectively.

The input current at X terminal is multiplied by the open loop transimpedance gain Z_T to produce an output voltage at node W. The output current of the W terminal is conveyed to node Z+, with the same value and phase, and to Z- with the same value but 180˚ out of phase.

Fig. 2 shows a simplified schematic of the BJT realization circuit of the OFCC which was proposed in [4]-[7]. The circuit is based on a commercial integrated CFA circuit (AD846) with many external BJT transistors (CA3096CE). This commercial CFA circuit has a large supply voltage (typical value is 15 V according to the AD846 datasheet). The circuit has high power consumption as well as a high cost and a large area. Furthermore, the connection of current mirror transistors shown in Fig. 2 increases the power consumption dramatically. The bias current drawn by the mirror

Manuscript received November 25, 2019; revised February 25, 2020; accepted April 10, 2020.
Corresponding author: Fahmi Elsayed (email: Fahmi.el-sayed@aum.edu.kw).

doi: 10.18178/ijeetc.9.5.317-323

transistors is a repeated CFA bias current (I_{DC}). The total DC bias current for the OFCC circuit is $5I_{DC}$, while the required action is only to copy the output current from the low output impedance node W to the high output impedance node Z+ and steer it to the other high output impedance node Z-.

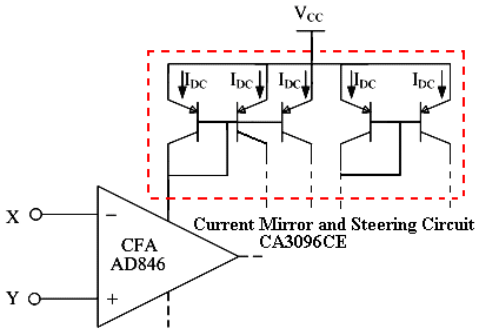

Fig. 2. Realization circuit of OFCC (DC biasing not shown).

A fully integrated CMOS OFCC circuit is proposed in this paper to solve the mentioned challenges. The OFCC circuit in a fully integrated form will improve the performance of the BJT OFCC circuit with respect to current tracking and voltage tracking errors. The integrated OFCC is very suitable for instrumentation amplifiers also, the CMOS-OFCC can be used in low voltage VLSI applications especially in the lab-on-chip (LOC) applications as a read out circuit.

The organization of the paper is as follows: in Section II, the proposed CMOS-OFCC is presented. The analysis for the OFCC circuit is described in Section III. Section IV shows the simulation results and Section V illustrates the proposed OFCC layout while the conclusion is presented in Section VI.

II. Proposed CMOS OFCC Circuit

The first step in designing the proposed OFCC circuit is the design of low power, low voltage CMOS CFA circuit. The congruous CMOS CFA circuit is presented in [8]. This CMOS CFA circuit has a wide bandwidth starting from DC signal. This, in turn, gives the proposed OFCC circuit the ability to be used in LOC applications [7]. The second step in the OFCC design is to design and relocate the current cloning (mirror and steering) circuit to a different position, as compared to the previous AD846 based work, to reduce the overall power consumption of the OFCC circuit. The change in the position must sustain the current tracking functionality between the OFCC output terminals. This is achieved by connecting the current mirror circuit to the high gain stage (last stage) in the buffer circuit of the used CMOS CFA circuit in [8].

Fig. 3 shows the new connection of the current cloning circuit in the proposed OFCC circuit. The repeated supply current in this case is only the current of the final stage in the buffer circuit in the used CFA instead of repeating the whole CFA circuit's current (I_{DC}). The repeated current is ΔI_{DC} where Δ is less than one tenth of the I_{DC}, depending on the design. This method of connection not only reduces the DC current but also reduces the required DC voltage supply as the number of stacking transistors is decreased.

The CMOS schematic of the proposed OFCC circuit is shown in Fig. 4. It could be cleared from the OFCC circuit schematic the new connection of the current cloning circuit (mirror and steering) comparing to the connection used the previous OFCC circuit shown in Fig. 2.

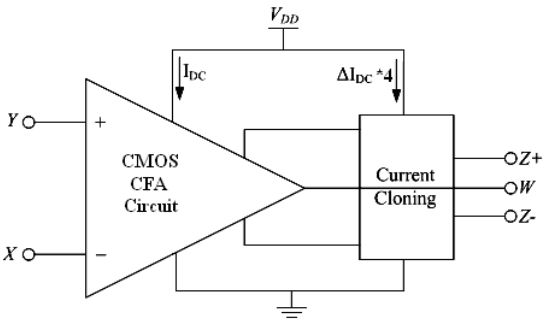

Fig. 3. New OFCC circuit block diagram.

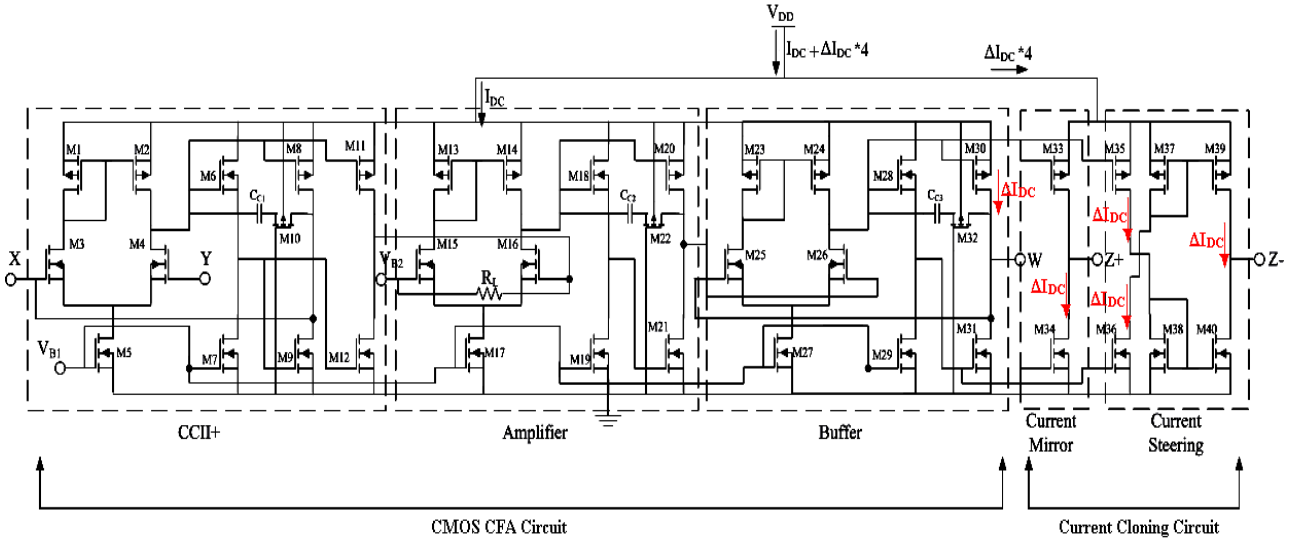

Fig. 4. Proposed OFCC circuit schematic.

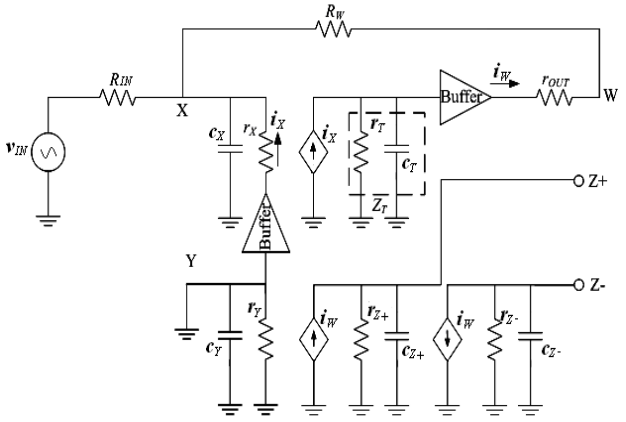

Fig. 5. AC small signal equivalent circuit for the new OFCC circuit in a closed loop inverting configuration.

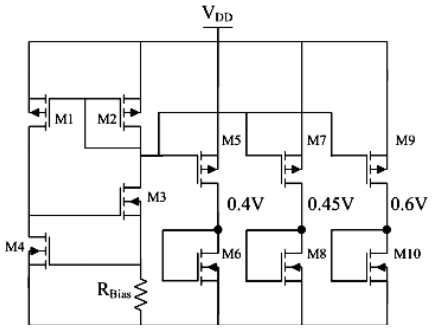

Fig. 6. Self-startup biasing circuit.

III. OFCC Circuit Analysis

Fig. 5 shows the OFCC AC small signal equivalent circuit in a negative feedback configuration.

Like the CFA circuit, the OFCC is designed with negative feedback between the terminals W and X using resistor R_W. This feedback resistor allows the OFCC to operate as a positive or negative current-conveyor while simultaneously reducing the input resistance at the X terminal. The negative feedback improves the DC stability as well as the transfer function accuracy [9].

The transfer function of the OFCC function is given by the following equation:

$$G(s) = \frac{V_{OUT}}{V_{IN}} = \frac{r_X r_{OUT} - R_W Z_T}{R_{IN}(r_X + r_{OUT} + R_W + Z_T)} \quad (2)$$

where

$$Z_T = A_O \times (R_L // \frac{1}{sc_T}). \quad (3)$$

r_{OUT} and r_X are the open loop output impedance and open loop inverting terminal input impedance respectively and A_O is the open loop gain of the high gain stage of the used CMOS OFCC circuit.

From equation 2, neglecting both r_X and r_{OUT} with respect to R_W and Z_T (open loop transimpedance of the OFCC), the overall closed loop gain is given by the following equation:

$$G = \frac{V_{OUT}}{V_{IN}} = -\frac{R_W}{R_{IN}} \times \frac{Z_T}{R_W + Z_T} \cong -\frac{R_W}{R_{IN}}. \quad (4)$$

The closed loop BW (ω_O) of the proposed OFCC circuit is given by

$$\omega_O = A_O \omega_C \frac{R_L}{R_W}. \quad (5)$$

where G is the closed loop gain, and ω_C is the 3 dB bandwidth of the high gain stage of the CFA used in the proposed OFCC circuit.

Fig. 6 presents the self-start up DC biasing circuit, which is needed to provide all the required biasing voltages for the OFCC circuit indicated in Fig. 4. The DC circuit provides 0.6, 0.45 and 0.4 volts bias voltages as indicated in Fig. 6.

IV. OFCC Circuit Simulation Results

The OFCC circuit indicated in Fig. 4 has been designed and simulated using cadence tools in 90 nm CMOS technology. The proposed OFCC aimed at two different design goals. The first goal is to design a low power consumption circuit while the second is to design a high bandwidth circuit.

The voltage supply used in the simulation is 1.2 V which is the standard voltage supply for 90 nm technology. The V_{B1} and V_{B2} in the schematic are DC biasing voltages. The self-start up circuit shown in Fig. 6 has been used to provide the required biasing voltages.

Table I indicates all transistors' geometries (W/L) in (μm/μm) that has been used in the LBW design, while Table II presents all transistors' geometries (W/L) in (μm/μm) that has been used in the HBW design. Table III shows all transistors' geometries (W/L) in (μm/μm) that has been used in the self-start-up DC biasing circuit.

TABLE I: TRANSISTORS' GEOMETRIES (W/L) IN (UM/UM) THAT HAS BEEN USED IN THE LBW DESIGN

Transistor(s)	Aspect ratio (W/L)
M5	22.22/0.8
M6	23.3/0.8
M7	10.5/0.8
M10	10/0.8
M22	6/0.8
M32	6.5/0.8
M33	22.47/0.8
M34	11/0.8
M35	22.85/0.8
M36	11.12/0.8
M37	6.55/0.8
M38	2.58/0.8
M39	6.59/0.8
M40	2.58/0.8
M1,M2	21.9/0.8
M3,M4	15.24/0.8
M8,M11	21.21/0.8
M9,M12	10.4/0.8
M17,M27	20.63/0.8
M18,M28	20.99/0.8
M19,M29	9.6/0.8
M20,M30	22.47/0.8
M21,M31	11/0.8
M13,M14,M23,M24	20.35/0.8
M15,M16,M25,M26	14.16/0.8

TABLE II: TRANSISTORS' GEOMETRIES (W/L) IN (UM/UM) THAT HAS BEEN USED IN THE HBW DESIGN

Transistor(s)	Aspect Ratio (*W*/*L*)
M1,M2,M13,M14,M23,M24	52.4/0.8
M3,M4,M15,M16,M25,M26	26/0.7
M5,M17,M27	27.4/0.8
M6,M18,M28	40.38/0.8
M7,M19,M29	14.1/0.8
M8,M11,M20,M30,M33,M35	25/0.3
M9,M12,M21.M31,M34,M36	10.8/0.3
M10,M22,M32	3/0.3
M37	8.4/0.3
M38	3.36/0.5
M39	8.4/0.5
M40	3.36/0.5

TABLE III: TRANSISTORS' GEOMETRIES (*W*/*L*) IN (UM/UM) THAT HAS BEEN USED IN THE SELF-START-UP DC BIASING CIRCUIT

Transistor(s)	Aspect Ratio (*W*/*L*)
M1	57.64/0.4
M2	53.8/0.4
M3	51.28/0.4
M4	26.89/0.4
M5	53.54/0.4
M6	26.62/0.4
M7	53.93/0.4
M8	16.14/0.4
M9	55.3/0.4
M10	5.53/0.4

From Table I and Table II, the transistors of the differential stages in the amplifier circuits were designed to have long channels, which in turn tend to low values of transistor's small signal output conductance (g_{ds}) values (higher gain). Transistors M8 and M9 in the HBW design have a short channel, with respect to their values in the LBW design, to increase the value of g_{ds} to prove that the increase in g_{ds} reduces the inductive effect.

In the HBW design, the same amplifier circuit is used in all the CFA circuit stages. The amplifier circuit is designed to have a high open loop voltage gain. The high open loop gain is achieved by using long channel transistors (high output resistances) and using high transconductance (gm). The high open loop amplifier gain sustains a high voltage tracking accuracy between the input terminals and at the same time keeps the output voltage of the buffer circuit in a good match with the input signal. Furthermore, the high open loop gain of the amplifier circuit increases the open loop transimpedance of the current feedback amplifier circuit. For the LBW design the same considerations are considered. However, the first amplifier circuit is different from the other two amplifiers. This is to make sure that the circuit works within the nominal design range.

Fig. 7 and Fig. 8 show the high output impedance terminals Z+ and Z- of the proposed OFCC circuit for both LBW design and HBW design respectively.

The tracking action parameters of the proposed OFCC circuit, h_{i1}, h_{i2} and h_v, are 1.02, 0.996 and 0.999 for the LBW respectively. On the other hand, these parameters are 0.82, 0.73 and 1 in the OFCC circuit presented in [4] design while they are 1.06, 0.999 and 0.999 for HBW design.

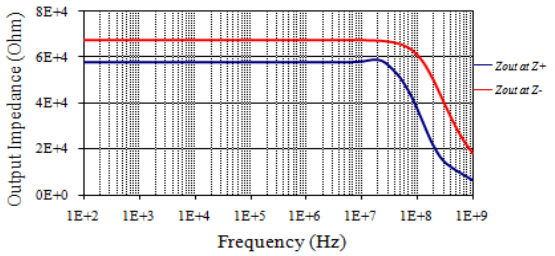

Fig. 7. Output impedance at the Z+ and Z- terminals (LBW design).

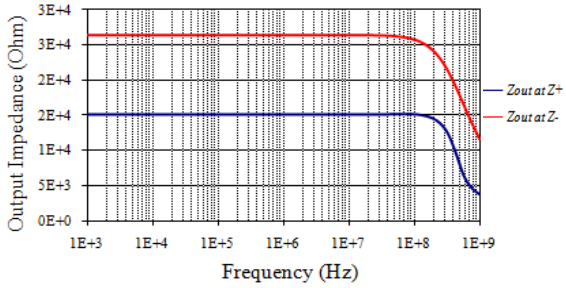

Fig. 8. Output impedance at the Z+ and Z- terminals (HBW design.

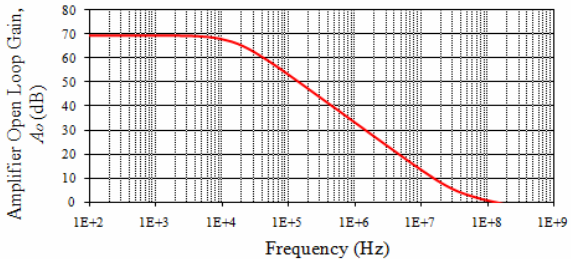

Fig. 9. Open loop gain of the amplifier stage A0 (LBW design).

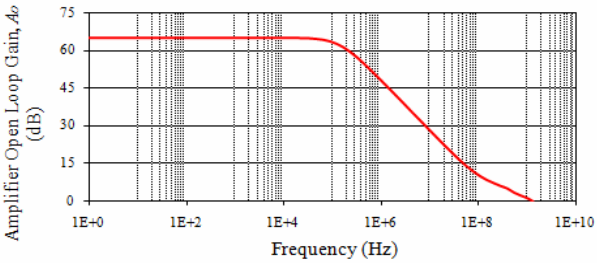

Fig. 10. Open loop gain of the amplifier stage A_0 (HBW design).

Fig. 9 shows the open loop gain of the amplifier versus the frequency. The circuit has an open loop gain equal to 3000 and R_L=800 Ω so, the total calculated trans-impedance is 2.4 MΩ while the simulated value is 2.34MΩ. Fig. 10 shows the open loop gain of the amplifier stage A_0 for the HBW design. The resistor R_L in this design is 400 Ω, the simulated open loop amplifier gain, (A_0) equals to 1780 (65 dB), as shown in Fig. 10.

The LBW CFA circuit has an open loop amplifier gain (A_0) which is equal to 3000 and a 3dB frequency f_c=15 KHz, as shown in Fig. 9. The optimum resistance RF is 1.2 kΩ with R_L=800 Ω. By substituting all these parameters in (5), the bandwidth of the closed loop LBW circuit is 30 MHz.

The simulation result for the LBW CFA circuit in inverting configuration is shown in Fig. 11. The simulation is repeated using different inverting closed loop gains (G). The LBW CFA circuit has a constant

closed-loop BW which is equal to 29.5 MHz (calculated value is 30 MHz).

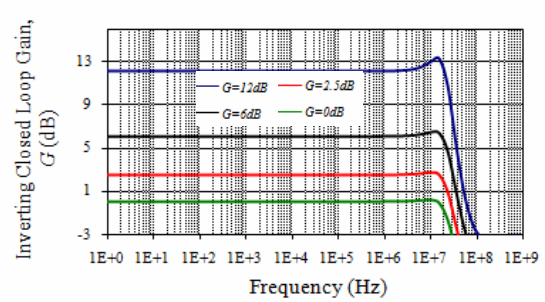

Fig. 11. LBW circuit with different inverting closed-loop gain (BW=29.5 MHz).

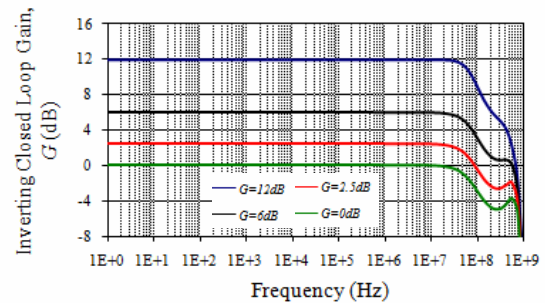

Fig. 12. HBW circuit with different inverting closed-loop gain (BW=104.6 MHz).

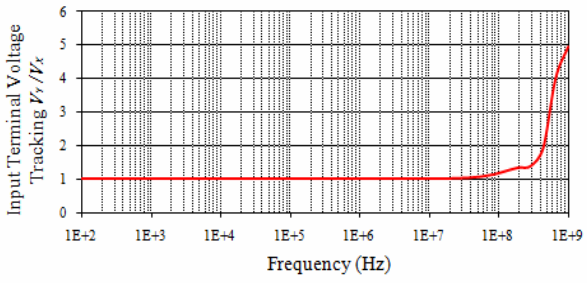

Fig. 13. The input terminals voltage tracking V_y/V_x (LBW).

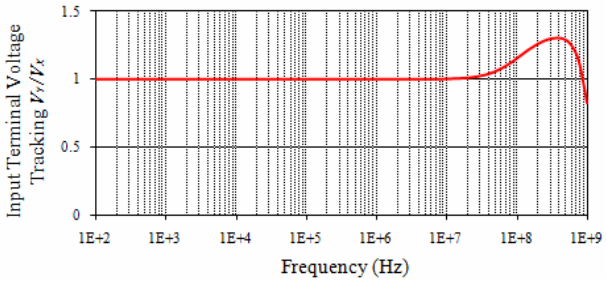

Fig. 14. The input terminals voltage tracking V_y/V_x (HBW).

The HBW CFA circuit has an open loop amplifier gain (A_O) of 1778 and f_c=147 kHz, as shown in Fig. 10. The optimum R_F is 1 kΩ with RL =400 Ω. Substituting all these parameters in (5), the bandwidth of the closed loop LBW CFA circuit is 104.6 MHz.

The frequency response simulation result for the HBW CFA circuit in the inverting closed loop configuration is shown in Fig. 12. The HBW CFA circuit has 104.6 MHz constant BW, which is close to the calculated value (104.6 MHz).

Fig. 13 and Fig. 14 present the input terminals voltage tracking for the LBW and HBW designs, as indicated in the figures, the input terminals (X) and (Y) are perfectly tracking each other for all range of frequencies up to almost 400 MHz.

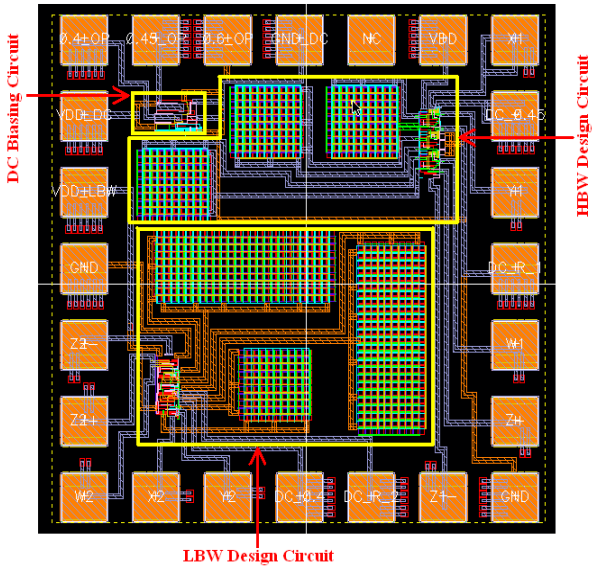

Fig. 15. Layout for the LBW OFCC, HBW OFCC circuits and the start-up DC biasing circuit.

TABLE IV: PERFORMANCE COMPARISON TABLE BETWEEN THE PROPOSED WORK AND OTHER RELATED WORK

Parameters	Units	Ref [13] 2014	Ref [11] 2015	Ref [12] 2017	Ref [10] 2016	Ref [1] 2020	Proposed work
Technology CMOS	µm	0.5	0.13	0.13	0.25	0.18	0.09
Supply voltage	V	3.3	1.2	1.5	±1.25	±0.8	1.2
3dB frequency, diff. gain	MHz	5.6	1200	600	291	559.1	HBW: 104.6 LBW:29.5
DC current range	mA	N/A	N/A	N/A	N/A	±0.35	HBW: 2.5 LBW:1
Open loop gain	dB	76	12	44.5	N/A	N/A	HBW:65 LBW:70
	V/V	6309	3.98	167.8	N/A	N/A	HBW:1778 LBW:3162
Open loop Trans impedance gain	KΩ	N/A	3.94	167	N/A	N/A	HBW:693 LBW:2300
Input impedance	Ω	N/A	8.83	N/A	3	6.36	HBW:8 LBW:20
Output impedance	KΩ	N/A	N/A	N/A	250	6230	HBW:32 LBW:65
Power consumption	µW	280.5	1500	35450	930	472	HBW:3000 LBW:1260
FOM=Gain * BW	KHz	35.34	4.776	100.7	N/A	N/A	HBW:186 LBW:93.2

Table IV presents a performance comparison between the presented work and other related work. The proposed OFCC circuit achieves higher DC current rages compared to the work presented in [1]. It is noted that the author in [11] achieves a higher 3dB frequency that this work but

the open loop gain is very small compared to the proposed work. In order to compare the presented work with other work, a FOM has been calculated for all publications in Table IV. As shown in the last raw, the proposed OFCC achieves the best FOM compared to other related work, which indicates that the proposed OFCC achieves high gain with wide bandwidth when compared to other OFCC circuits. Regarding the input resistance, the proposed OFCC achieves a reasonable input resistance and comparable with others, while presenting the best transimpedance gain. Overall, he proposed OFCC indicated an improved performance when compared to other OFCC designs.

V. Proposed OFCC Layout

The layout of the schematics presented in this paper of the LBW and HBW OFCC circuits is shown in Fig. 15. The LBW OFCC circuit occupies 550 µm by 350 µm while the HBW OFCC occupies 500 µm by 100 µm. The size of the designed pads is 100 µm by 100 µm with 50 µm separation.

The layout passed the Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks for the 90 nm technology kit and was submitted for fabrication.

VI. Conclusion

A fully integrated CMOS OFCC circuit has been presented at two different design parameters. The layout of the designed OFCC circuit has been presented as well. The current cloning circuit in the new OFCC circuit has been relocated in order to reduce the power consumption of the circuit with sustaining the proper OFCC operation. The simulation results have been represented regarding the LBW and the HBW design. The open loop gain, closed loop gain, voltage tracking and the output impedance simulated results have been presented. The consumed DC power for the LBW design is 1.26 mW at 30 MHz bandwidth while it is 3mW at 104.6MHz bandwidth for the HBW design.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Fahmi Elsayed conducted the research, did all the theoretical analysis and design, 60% of simulation part and wrote 70% of the paper; Mostafa Rashdan and Mohammad Salman did 40% of the simulation part analyzed the data, wrote 30% of the paper and did the proof reading; all authors had approved the final version.

Acknowledgment

This work was supported by the Electrical Engineering Dept., the University of Calgary and CMC Microsystems.

References

[1] T. Ettaghzouti, M. Bchir, and N. Hassen, "High CMRR voltage mode instrumentation amplifier using a new CMOS differential difference current conveyor realization," *International Journal of Electrical and Electronic Engineering & Telecommunications*, to be Published.

[2] Prerna and V. Niranjan, "Analog multiplier using DTMOS-CCII suitable for biomedical application," in *Proc. IEEE International Conference on Computing, Communication & Automation*, Noida, India, May 2015, pp. 1353-1357.

[3] H. F. Hamed, A. El-Gaafary, and M. S. A. El-Hakeem, "A new differential current conveyor and its application as a four quadrant multiplier," in *Proc. IEEE Int. Conf. on Electronics, Circuits and Systems*, 2001, pp. 569-572.

[4] A. Khan, M. A. Al-Turaigi, and M. Abou El-Ela, "Operational floating current conveyor: Characteristics, modeling and applications," in *Proc. IEEE Instrumentation and Measurement Technology Conference*, Hamamatsu, Japan, May 1994, pp. 788-791.

[5] D. Nand, N. Pandey, R. Pandey, and S. Jindal, "Operational floating current conveyor based digitally controlled hearing aid," in *Proc. SPIN2018*, Delhi, India, 2018, pp. 647-651.

[6] H. ElGemmazy, A. Helmy, H. Mostafa and Y. Ismail, "A novel CMOS-based fully differential operational floating conveyor", in *Proc. IEEE Computer Society Annual Symposium on VLSI*, Bochum, Germany, 2017, pp. 604-608.

[7] N. Pandey, D. Nand, and R. Pandey, "Generalised operational floating current conveyor based instrumentation amplifier," *IET Circuits, Devices & Systems*, vol. 10, no. 3, pp. 209-219, Nov. 2015.

[8] F. Elsayed, M. F. Ibrahim, Y. H. Ghalab, W. Badawy, and B. Maundy, "A new 90nm current feedback operational amplifier," in *Proc. Canadian Conference on Electrical and Computer Engineering*, 2009, pp. 903-906.

[9] S. J. G. Gift, "An enhanced current-mode instrumentation amplifier," *IEEE Trans. Instrumentation and Measurement*, vol. 50, no. 1, pp. 85–88, Jan. 2001.

[10] M. A. Ibrahim, E. Yuce, and S. Minaei, "A new DVCC-based fully cascadable voltage-mode full-wave rectifier," *Journal of Computational Electronics*, vol. 15, no. 4, pp. 1440–1449, December 2016.

[11] N. M. Edward, Y. H. Ghallab, H. M. Hassan, and Y. I. Ismail, "A CMOS based operational floating current conveyor," in *Proc. IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Cairo, 2015, pp. 157-160.

[12] H. Elgemmazy, A. Helmy, H. Mostafa, and Y. Ismail, "A novel CMOS based fully differential operational floating conveyor," in *Proc. IEEE International Symposium on Very Large Scale Integration (ISVLSI 2017)*, Bochum-Germany, 2017, pp. 604-608.

[13] F. Esparza-Alfaro, A. J. Lopez-Martin, G. Palumbo, and S. Permisi, "CMOS class-AB tunable voltage-feedback current operational amplifier," in *Proc. 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Marseille, 2014.

Fahmi M. Elsayed received his bachelor degree in electronics and communications engineering from Zagazig University, Egypt, 2002. From 2003 to 2007, he was working as Teaching and Research Assistant at the University of Zagazig before joining University of Calgary in 2007. He completed his master degree (M.Sc.) in 2009 and Ph.D. in 2014 at University of Calgary, Alberta, Canada. During his Ph.D. study, from 2011 to 2014, he was working with Ericsson Canada. He was appointed Assistant professor at Zagazig University in 2014. From 2013 to 2015, he was adjunct research assistant at faculty of Kinesiology, University of Calgary. In 2015, he joined American University of the Middle East

(AUM) as Assistant Professor. Currently, he is an assoc. professor with Electrical Engineering Department at the American University of the Middle East in Kuwait.
His research interests are digital signal processing techniques as applied for wireless Communication, RF power amplifier design, RF integrated circuit design and current mode amplifier design. He has two US patents and many research papers.

Mostafa Rashdan received the B.Sc. degree in Electrical Engineering and M.Sc. degree in Electronics and Communications in 1997 and 2001, respectively from Minia University, Egypt. He worked as a Teaching assistant for the High institute of Energy, Aswan, Egypt from 1999 to 2005. In 2011 he received the Ph.D. in Electrical and Computer Engineering from the University of Calgary, Alberta, Canada. He worked as postdoctoral fellow for the RFIC group at University of Calgary from January 2011 till Sept. 2011 and from July 2013 till January 2015. He was working as an assistant professor for the Faculty of Energy Engineering, Aswan University, Aswan, Egypt for the period from Sept. 2011 till June 2013. He is currently working as an assistant professor for the American University of the Middle East in Kuwait. He has won several awards such as the Outstanding Student IC Designer Award from Analog Devices Inc. in Feb. 2013 and Kenneth C. Smith Early Career Award for Microelectronics Research from IEEE 43rd International Symposium on Multiple-Valued Logic (ISMVL 2013). Dr. Rashdan is a member of the IEEE. His current research is focusing on the mixed signal integrated circuit design, time-based serial communication link architectures and high-speed data converters.

Mohammad S. Salman received the B.Sc., M.Sc. and Ph.D. Degrees in Electrical and Electronics Engineering from Eastern Mediterranean University (EMU), in 2006, 2007 and 2011, respectively. From 2006 to 2010, he was a teaching assistant of Electrical and Electronics Engineering department at EMU. In 2010, he has joined the Department of Electrical and Electronic Engineering at European University of Lefke (EUL) as a senior lecturer. For the period 2011-2015, he has worked as an Assist. Prof. in the Department of Electrical and Electronics Engineering, Mevlana (Rumi) University, Turkey. Currently, he is an assoc. professor with Electrical Engineering Department at the American University of the Middle East in Kuwait. He has served as a general chair, program chair and a TPC member for many international conferences. His research interests include signal processing, adaptive filters, image processing, sparse representation of signals, control systems and communications systems.