A Low-Noise Amplifier Utilizing Current-Reuse Technique and Active Shunt Feedback for MedRadio Band Applications

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***Abstract*—In this work, a low-power 0.18-μm CMOS low-noise amplifier (LNA) for MedRadio applications has been designed and verified. Cadence IC5 software with Silterra's C18G CMOS Process Design Kit were used for all design and simulation work. This LNA utilizes complementary common-source current-reuse topology and subthreshold biasing to achieve low-power operation with simultaneous high gain and low noise figure. An active shunt feedback circuit is used as input matching network to provide a suitable input return loss. For test and measurement purpose, an output buffer was designed and integrated with this LNA. Inductorless design approach of this LNA, together with the use of MOSCAPs as capacitors, help to minimize the die size. On post-layout simulations with LNA die area of 0.06 mm^2 and simulated total DC power consumption of 0.5 mW, all targeted specifications are met. The simulated gain, input return loss and noise figure of this LNA are 16.3 dB, 10.1 dB and 4.9 dB respectively throughout the MedRadio frequency range. For linearity, the simulated input-referred P_{1dB} of this LNA is –26.7 dBm while its simulated IIP_3 is –18.6 dBm. Overall, the post-layout simulated performance of this proposed LNA is fairly comparable to some current state-of-the-art LNAs for MedRadio applications. The small die area of this proposed LNA is a significant improvement in comparison to those of the previously reported MedRadio LNAs.**

***Index Terms*—LNA, MedRadio, low-power, current-reuse, active shunt feedback, subthreshold biasing**

I. Introduction

The number of elderly around the world keeps growing as global life-expectancy continues to increase. As a result, cost-effective medical services are becoming more and more important nowadays. This has triggered some widespread research and development activities in wireless communications of biomedical applications, thus resulting in the development of some next generation biomedical devices such as drug delivery implants and neuro-muscular stimulators [1], [2]. The Medical Device Radiocommunications Service (MedRadio) frequency band spans from 401 MHz to 406 MHz. This frequency band was established in 2009 by the Federal Communications Commission (FCC) of the United States and is dedicated for the wireless communications of biomedical devices [3]. Specifically, these refer to devices such as implants and body-worn devices. There are other frequency band options for biomedical devices. Such bands include the ISM band around 2.4 GHz and the European SRD band between 868 MHz to 928 MHz. Both of these however, are less suitable for biomedical applications since they are also being utilized by other applications [4].

Very low power consumption is an important feature for biomedical implants and body-worn medical devices [1], [2], [4]–[7]. This is to maximize battery life hence reducing the frequency of battery replacement. This will eventually result in more stability, reliability and cost-efficiency of the biomedical device. For these devices, the wireless communication part normally has the highest power consumption. Therefore, the key to producing low-power biomedical devices is by having low-power components in the wireless communication part. Another important characteristic of biomedical devices is high sensitivity to be able to detect very low and weak radio-frequency (RF) signals that have undergone significant attenuation by the human body [2]. After all, the RF signals used in biomedical applications should not be overly large as they can be hazardous to the human body. The biomedical devices also must be of reasonably miniature size. This is for handiness as they are either to be body-worn or embedded underneath the skin of the patient [6]. Apart from this, minute size of the integrated circuit will help to further reduce fabrication cost.

The objective of this research work is to design and simulate a low-noise amplifier (LNA) for MedRadio applications. The LNA is one of the most important components in the receiver section of wireless communication systems in general. It is the first active component in the receiver section, and therefore needs to provide adequate gain to amplify the received signal at the antenna. Simultaneously, the amplified signal should only be added with an acceptable amount of noise. This component must also be capable of handling reasonably large received signals without distorting them. For

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maximum power transfer into the input of the LNA, it needs to present an appropriate input impedance, which is typically 50 Ω [8]. In addition, for MedRadio applications, the LNA needs to consume very low power. However, extremely low power consumption of the MedRadio LNA will degrade its gain and noise figure. The main challenge in this work is therefore to achieve a proper trade-off between gain, noise figure and power consumption of the MedRadio LNA. Additionally, this LNA must have a very small size for convenience and cost-reduction purposes.

A low-power 0.18-µm CMOS MedRadio receiver RF front-end that includes a single-ended complementary common-source current-reuse LNA was proposed in 2011 [4]. From the measurements of the standalone LNA, it exhibits gain of 20 dB, noise figure (NF) of 2.8 dB, input return loss (RL) of 15 dB and input third-order intercept point (IIP_3) of –8.1 dBm whilst consuming only 0.15 mW of DC power. The die area of the standalone LNA is 0.35 mm^2. In 2016, [9] reported a cascode inductively-degenerated 0.18-µm CMOS MedRadio differential LNA. This LNA occupies a space of 0.2 mm^2. On measurements, it gives out gain of 31 dB, input RL of greater than 14 dB, NF of 5.8 dB and input-referred 1-dB compression point (IP_{1dB}) of –23 dBm with a power consumption of 0.7 mW. Two years later, [10] reported a 2-stage low-power 0.18-µm CMOS single-to-differential MedRadio LNA. The IC layout of this LNA takes up a space of 0.83 mm^2 and on simulations, it demonstrates gain of 23 dB, NF of 3.1 dB, input RL of 12 dB and IIP_3 of –27.5 dBm. The power consumption of this LNA is just 0.29 mW.

All these 3 reported LNAs for MedRadio applications are having very good balance between gain, noise figure and power consumption. The power consumptions is less than 1 mW for all these three LNAs while the minimum gain amongst them is 20 dB, and the noise figure ranges from 2.8 dB to 5.8 dB. Inductive source-degeneration technique is employed by these LNAs to achieve the excellent gain and noise figure with very low power consumption. However, the use of inductors to implement this technique inevitably results in fairly large overall size of the LNA. Consequently, the biomedical device becomes bulkier thus making it less suitable to be used as implants. It is therefore very advantageous to employ an inductorless topology for the LNA to minimize its size.

Some current state-of-the-art MedRadio LNAs were used as performance benchmark in this work. The targeted general specifications for the MedRadio LNA in this work were therefore derived from these state-of-the-art LNAs. These specifications are summarized in Table I.

TABLE I: TARGETED GENERAL SPECIFICATIONS OF THE MEDRADIO LNA IN THIS WORK

Parameter	Specification
Frequency range	401 MHz to 406 MHz
DC power consumption, P_{DC}	≤ 1.0 mW
Gain, A_v	≥ 15 dB
Noise figure, NF	≤ 6 dB
Input return loss, RL_{in}	≥ 10 dB
Input-referred 1-dB compression point, IP_{1dB}	≥ -30 dBm
Input third-order intercept point, IIP_3	≥ -20 dBm
Die area, A_{die}	≤ 0.1 mm^2

II. SPECIFICATIONS DEFINITION

As a starting point to design a LNA with practically low power consumption, the power consumption specification was set to be a maximum of 1.0 mW since all three MedRadio LNAs reviewed previously are consuming DC power of well below 1 mW. For MedRadio applications, the sensitivity (or the minimum input power at the receiver) is roughly around -90 dBm which is considerably very low [4], [9], [11]. Hence, adequate gain of the LNA is required to amplify weak signals arriving at the receiver of the device prior to the downconversion of these signals by the mixer. Reference [11] suggested a relatively relaxed gain specification of just over 10 dB. Reference [9] on the other hand, proposed a much higher gain specification of greater than 35 dB. Considering that inductorless topology was planned for this LNA, and that the power consumption specification is reasonably very low at less than 1.0 mW, the gain specification was therefore set at 15 dB or greater.

The sensitivity of MedRadio devices can also be used to estimate the noise figure specification of the LNA. Ref. [9] computed a total noise figure value of about 19 dB for the whole receiver portion of a MedRadio device with a sensitivity of around –90 dBm. Since the LNA is the first active block of the receiver chain, [9] went on to propose a noise figure specification of less than 6 dB for the LNA. This noise figure specification was therefore selected for the LNA in this work. The specification for input return loss was set to be at least 10 dB because this is commonly the minimum acceptable level for return loss in most RF and microwave circuits and systems.

Linearity for MedRadio LNAs is usually not much of a concern as MedRadio applications only involve very weak and low RF signals. The maximum received power at the input of MedRadio devices is approximately –30 dBm as estimated by [9]. Thus, the specification for input-referred 1-dB compression point in this work was set to be equal to or greater than –30 dBm. Theoretically, the input third-order intercept point is approximately 10 dB greater than the input-referred 1-dB compression point [12]. The specification for input third-order intercept point was therefore set to be equal to or greater than –20 dBm. The die area specification of the LNA was largely determined by the 0.18-µm CMOS process technology being employed in this work and also by the inductorless topology being planned for this LNA. Due to this inductorless topology, the final size of this LNA was estimated to be significantly smaller than those of the three LNAs reviewed previously. The specification for die area was therefore set to be equal to or less than 0.1 mm^2.

III. CIRCUIT TECHNIQUES

A. Identification of Suitable Circuit Techniques

This LNA should operate within the range of 401 MHz to 406 MHz which is the MedRadio frequency spectrum. Since this frequency range can be considered to be reasonably low in the RF spectrum, it was possible to simply exploit the low-frequency gain of a MOS

transistor to provide the gain in MedRadio frequency band. Inductors were therefore not needed to help resonating the gain at a higher frequency. With this inductorless design approach, the size of the IC would be considerably reduced which would be very suitable for biomedical implants.

The specification for DC power consumption is less than or equal to 1.0 mW which is fairly low. This is essential for biomedical applications to prolong battery life-time. To achieve this very low power consumption, two circuit techniques for low-power design, namely current-reuse and subthreshold biasing, were employed in this LNA design.

For gain, the targeted specification is greater than or equal to 15 dB. This is considerably high for a LNA with power consumption of less than 1.0 mW. The afore-mentioned two low-power design circuit techniques were very much suitable to cater for this requirement; the subthreshold biasing technique provides high ratio of transconductance g_m over drain current I_D whilst the current-reuse technique allows economical use of the current in obtaining a decent gain.

The specification for input return loss is greater than or equal to 10 dB. To achieve this, the active shunt feedback technique was employed. This technique is utilizing a source-follower network (common-drain amplifier). The hugely-popular inductive-degeneration technique is not suitable to be used for input matching in this LNA design as it involves the use of inductor at the source terminal of the main driver transistor.

Another reason for opting with the active shunt feedback technique for input matching was to simultaneously achieve a fairly decent noise figure. The noise figure specification as stated in Table I is less than or equal to 6 dB. This active feedback technique would result in a much better noise figure compared to the resistive feedback technique. In addition, utilizing the current-reuse and subthreshold biasing techniques would produce large transconductance in the main driver that could contribute significantly to a good noise figure for the LNA.

For linearity, the specifications for input-referred 1-dB compression point (IP_{1dB}) and input third-order intercept point (IIP_3) are greater than or equal to –30 dBm and –20 dBm respectively. These specifications were considerably loose and could be achieved quite easily. However, if necessary, the gain of the LNA could be reduced or limited to improve linearity.

Finally, the specification for die area (A_{die}) of the LNA is less than or equal to 0.1 mm^2 which is fairly small in size. This was achieved by employing inductorless circuit topology that saves considerably large amount of space. Further reduction in total die area was attained by utilizing MOS transistors as capacitors (also known as MOSCAPs) instead of using the more common MIM or finger capacitors in the IC layout.

B. Current-Reuse Technique

The current-reuse technique allows the LNA to obtain a much larger transconductance without the need to further increase the current. This can also be viewed as cutting down the amount of current drawn without (or just minimally) affecting the transconductance of the LNA. There are many ways of implementing this current-reuse technique as demonstrated by various authors [4], [11], [13]–[23]. The most common way is by stacking a PMOS transistor on top of a NMOS transistor. With this arrangement, both transistors are in the same DC current path. Either complementary common-source current-reuse or complementary common-gate current-reuse configuration can then be implemented with this arrangement. Using either of these two configurations may almost double the effective transconductance of the amplifier compared to that using only a NMOS transistor with a load in the same DC current path while extracting the same amount of current.

C. Active Shunt Feedback Technique

The active shunt feedback technique is typically applied to a LNA for input impedance matching. This is by presenting a suitable impedance at the input of the LNA, which is normally 50 Ω. This technique is quite common for wideband LNAs and LNAs with inductorless topology for die size reduction [11], [24]–[28]. It is very suitable for implementation on common-source and cascode LNAs where the silicon dioxide insulation between the gate and the drain-source channel of the driving transistor causes the input resistance to be infinitely high. This very high input resistance can then be brought down to a much lower and more appropriate impedance by employing the active shunt feedback technique.

D. Subthreshold Biasing Technique

The subthreshold biasing technique is also known as weak inversion and is a very popular low-power design technique. The use of this technique has been successfully demonstrated by [5], [6], [15], [24]–[27] amongst others to achieve very low power consumption in their respective designs. When the gate-source voltage V_{GS} of the MOS transistor is lower than the threshold voltage V_{TH} of the device, but sufficient enough to form a depletion region at the surface of the silicon substrate adjacent to the drain-source channel, subthreshold biasing can be said to have occurred.

IV. Circuit Design

A. Design Flow

Fig. 1 outlines the overall design flow of the MedRadio LNA in this work. In this flow chart, there are some dotted arrows that show possible paths that could be taken to improve the outcomes of certain results. The design flow began with the design of the LNA's core section, which is the main driver. The next step was the design of a feedback network and the formation of complete LNA by integrating it with the main driver. The last section of the complete circuit to be designed was the output buffer for testing purpose. Schematic-level simulation was then performed on the completed LNA design including the output buffer. Once the schematic-

level simulation results were considered reasonable and acceptable, the physical IC layout was subsequently designed. The next step was to verify the completed layout with Calibre's DRC (design rule check) and LVS (layout-vs-schematic) facilities. The last step in this MedRadio LNA design flow was parasitic extraction which was then followed by post-layout simulation.

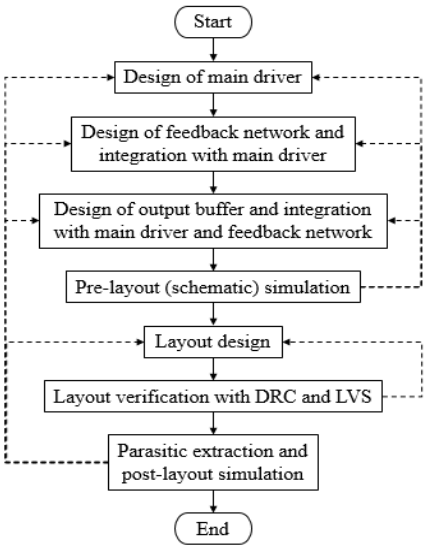

Fig. 1. MedRadio LNA overall design flow.

B. Design of Main Driver

The main driver is the most important part of the LNA. This is the part of the LNA that provides gain for signal amplification. Due to the low power requirement, complementary common-source current-reuse topology had been chosen for the main driver of this LNA. Fig. 2 is the schematic circuit diagram for this main driver.

Fig. 2 contains the complementary common-source current-reuse structure that is comprised of a pair of NMOS and PMOS transistors (M_1 and M_2 respectively) with the PMOS transistor being stacked on top of the NMOS transistor in the same DC current path. With this configuration, current from supply voltage V_{CSCR} that passes through the source-drain channel of M_2 will be reused by M_1. The biasing voltages for M_1 and M_2 are also shown together with the corresponding biasing resistors and DC-blocking capacitors. To be further economical on power consumption, subthreshold biasing technique is to be implemented on NMOS transistor M_1.

For the complementary common-source current-reuse topology, input AC signals are being fed into the gates of both M_1 and M_2, and the amplified output signals appear between the drains of both transistors. R_1 and R_2 biasing resistors prevent AC signals from being shorted to ground whilst C_1, C_2, and C_3 block DC currents. For both M_1 and M_2, the bulk is tied to the source. This eliminates body effect from both transistors. The corresponding simplified small-signal equivalent circuit for the main driver is given in Fig. 3. In obtaining this simplified small-signal equivalent circuit for the main driver, some useful approximations have been made:

- All DC-blocking capacitors (C_1, C_2, and C_3) have very high capacitances thus resulting in very low AC impedance. This is to maximize signal transmission from input to output. These capacitors are therefore shorted for simplicity.
- The shunt biasing resistors R_1 and R_2 are of very high values to minimize AC signal leakage to the biasing voltage points which are AC GND points. These resistors are hence removed (i.e. open-circuited).

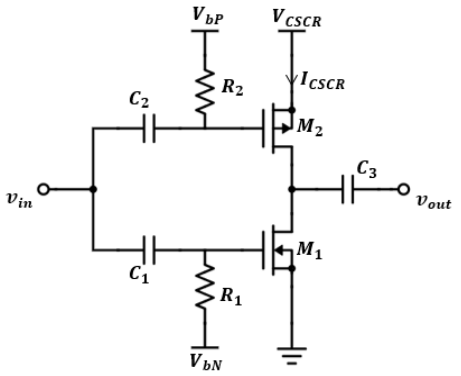

Fig. 2. Schematic circuit diagram for the main driver.

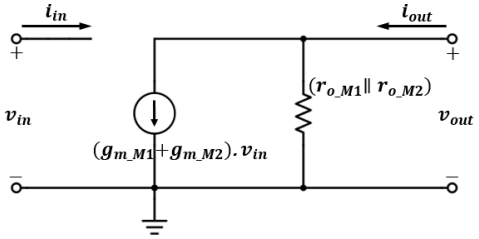

Fig. 3. Simplified small-signal equivalent circuit for the main driver.

In addition, M_1 transconductance $g_{m\_M_1}$ and M_2 transconductance $g_{m\_M_2}$ are added up together, and small-signal output resistances r_{o_M1} and r_{o_M2} are combined in parallel. From Fig. 3, the low-frequency small-signal gain of this main driver can be derived as:

$$A_v = -(g_{m\_M1} + g_{m\_M2})\left(\frac{r_{o\_M1} r_{o\_M2}}{r_{o\_M1} + r_{o\_M2}}\right) \tag{1}$$

This derived gain equation basically implies that the low-frequency small-signal gain can be increased by increasing the transconductances of M_1 and M_2 and the small-signal output resistances of M_1 and M_2. This gain equation may only work quite accurately for very low frequencies. As the frequency increases, the effects of parasitic capacitances associated with MOS transistors are gradually becoming more significant. For noise analysis of this main driver, the noise factor of the main driver F_{MD} can be derived as:

$$F_{\text{MD}} = 1 + \frac{\left(\gamma_{M_1} g_{m\_M_1} + \gamma_{M_2} g_{m\_M_2}\right) \times R_{\text{out}}^2}{A_v^2 \times R_s} \tag{2}$$

where A_v is the small-signal gain, R_S is the source resistance, R_{out} is the output resistance, γ_{M_1} is the thermal noise coefficient for M_1, γ_{M_2} is the thermal noise coefficient for M_2, $g_{m\_M_1}$ is the transconductance of M_1

and $g_{m\_M_2}$ is the transconductance of M_2. This noise factor expression simply indicates that the overall noise figure of the main driver can be reduced by increasing the gain.

Table II summarizes the chosen DC parameters, gate dimensions and transconductances for M_1 and M_2 transistors in the complementary common-source current-reuse structure of the main driver.

TABLE II: DC PARAMETERS, GATE DIMENSIONS AND TRANSCONDUCTANCES FOR M_1 AND M_2 IN THE COMPLEMENTARY COMMON-SOURCE CURRENT-REUSE STRUCTURE OF THE MAIN DRIVER

Parameter	M_1	M_2
Drain current, I_D	0.5 mA	-0.5 mA
Drain-source voltage, V_{DS}	0.4 V	-0.4 V
Gate-source voltage, V_{GS}	0.5 V	-0.6 V
Gate length, L	0.18 μm	0.18 μm
Gate width, W	131.6 μm	144 μm
Transconductance, g_m	9.3 mS	5.7 mS

To estimate the low-frequency small-signal gain of the main driver as given by (1), the transconductance values of M_1 and M_2 are required together with the small-signal output resistances of M_1 and M_2. The small-signal output resistance of a MOS transistor r_o at its operating point can be obtained from the inverse gradient of its I_D vs V_{DS} plot (for a given V_{GS}) at that particular point.

$$r_o = \frac{\delta V_{DS}}{\delta I_D} \tag{3}$$

with small-signal output resistance of M_1 r_{o_M1} =3459 Ω and small-signal output resistance of M_2 r_{o_M2} = 4264 Ω, the low-frequency small-signal gain of the main driver was estimated to be approximately –28.6 or 29.1 dB. This small-signal gain is for very low frequencies close to 0 Hz. The main driver gain at MedRadio frequencies would not therefore exceed this estimated small-signal gain. As frequency increases, this gain will degrade due to parasitic capacitances within the MOS transistors.

C. Design of Feedback Network and Integration with Main Driver

The feedback network links the output of the main driver back to the input. Its function is to provide input impedance matching to attain a reasonable return loss at the input of the LNA. This is important for optimum signal power transfer into the input of the LNA. Active shunt feedback utilizing a source-follower network (common-drain amplifier) had been chosen as the feedback circuit as this technique is well-suited for LNAs with inductorless topology to minimize the size of the IC. For this work, a PMOS transistor was being used instead of a NMOS one. This feedback technique is using a shunt-shunt feedback configuration where the source-follower network shunts the input and output of the amplifier. The output from the amplifier is therefore sampled into the source-follower feedback network, and the output from the source-follower is fed back to the input of the amplifier.

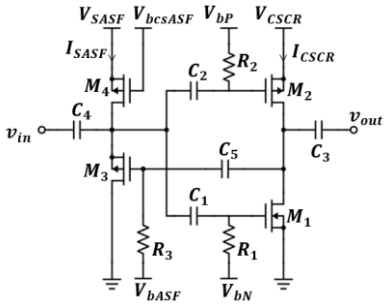

Fig. 4. Schematic circuit diagram for the integration of the active shunt feedback network with the main driver to form the complete LNA.

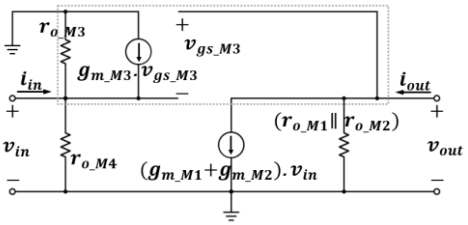

Fig. 5. Simplified small-signal equivalent circuit of the complete LNA. The active shunt feedback loop is marked by grey-dotted rectangle.

Fig. 4 illustrates the integration of this active shunt feedback network with the main driver to form the complete LNA. PMOS transistor M_3 is the driving transistor of this source-follower feedback network, whilst another PMOS transistor M_4 acts as current source. V_{SASF} is the voltage supply from which current I_{SASF} flows through M_4 and M_3 in the source-follower network. The respective biasing voltages for M_3 and M_4 are also shown in Fig. 4. As the driving transistor in the source-follower, M_3 requires biasing resistor R_3 to choke the feedback signal to prevent it from being shorted to ground at M_3s' biasing voltage point. Two additional capacitors, C_4 and C_5 are also included as DC-blocking capacitors. With this integrated active shunt feedback network, the input impedance of the LNA is approximately the impedance looking into the source terminal of M_3. For both M_3 and M_4, the bulk is tied to the source to eliminate body effect so that the circuit will be more predictable and easier to be analyzed. This was the reason why PMOS transistors were chosen for this active shunt feedback network instead of NMOS transistors. With NMOS transistors, the bulk is connected to ground. Thus, connecting the bulk of the driving NMOS transistor to its source terminal will ground the source of the transistor and also the input RF signal of the LNA.

The simplified small-signal equivalent circuit of the main driver in Fig. 3 can be modified to include the active shunt feedback network thus becoming the simplified small-signal equivalent circuit of the complete LNA. This is depicted by Fig. 5 with the active shunt feedback loop linking the output of the main driver back to its input. In this small-signal equivalent circuit, the active shunt feedback network is treated as a common-drain amplifier as described in Chapter 3 of [28].

Just like C_1, C_2, C_3, R_1, and R_2 previously, C_4, C_5, and R_3 have also been omitted in Fig. 5 since their values are considerably very large. From Fig. 5, the low-frequency

small-signal input resistance r_{in} of this LNA can be derived as:

$$r_{\text{in}} = \frac{1}{\frac{1}{r_{o\_M_4}} + \frac{1}{r_{o\_M_3}} + g_{m\_M_3}(1 - A_v)} \quad (4)$$

where $r_{o\_M_3}$ is the small-signal output resistance of M_3, $r_{o\_M_4}$ is the small-signal output resistance of M_4, $g_{m\_M_3}$ is the transconductance of M_3 and A_v is the low-frequency small-signal gain of the LNA. Equation (4) basically implies that the low-frequency small-signal input resistance depends on the low-frequency small-signal gain of the LNA, and the transconductance for M_3 which is the driver transistor of the active shunt feedback network. Since both M_3 and M_4 should be biased in their saturation region, $r_{o\_M_3}$ and $r_{o\_M_4}$ can be estimated to be considerably large (in the range of few kΩ's). Thus, (4) can be approximated and simplified as:

$$r_{\text{in}} = \frac{1}{g_{m\_M_3}(1 - A_v)} \quad (5)$$

Just as for the small-signal gain equation previously, this expression for small-signal input resistance may only be suitable for very low frequencies. This is due to the effects of parasitic capacitances associated with MOS transistors that are gradually becoming more significant as the frequency increases.

From Fig. 4 and Fig. 5, it can also be seen that the small-signal input voltage for the LNA is approximately equal to v_{in} as there is only negligible voltage drop due to considerably large values of $r_{o\_M_3}$ and $r_{o\_M_4}$. Thus, the low-frequency small-signal gain expression for the LNA is approximately the same as that for the main driver. In other words, the low-frequency gain expression for the main driver stays approximately the same even after the integration with the active shunt feedback network, so to speak. This low-frequency gain expression is as given by (1).

For noise analysis of the complete LNA, the noise factor of the complete LNA F_{CL} can be derived as:

$$F_{\text{CL}} = F_{\text{MD}} + \frac{\left(\gamma_{M_3} g_{m\_M_3} + \gamma_{M_4} g_{m\_M_4}\right) R_{\text{in}}^2}{R_s} \quad (6)$$

where F_{MD} is the noise factor of the main driver, R_S is the source resistance, R_{in} is the input resistance, γ_{M_3} is the thermal noise coefficient for M_3, γ_{M_4} is the thermal noise coefficient for M_4, $g_{m\_M_3}$ is the transconductance of M_3 and $g_{m\_M_4}$ is the transconductance of M_4. F_{CL} is closely similar to F_{MD} except with the addition of the "$\frac{\left(\gamma_{M_3} g_{m\_M_3} + \gamma_{M_4} g_{m\_M_4}\right) R_{\text{in}}^2}{R_s}$" term that is caused by the presence of M_3 and M_4 that form the active shunt feedback network at the input of the LNA. However, if $g_{m\_M_3}$, $g_{m\_M_4}$ and R_{in} are relatively small, F_{CL} will be almost equal to F_{MD}.

As given by (4) and (5), the input impedance of the LNA mainly depends on its gain and the transconductance of M_3 which is the driving transistor of the active shunt feedback network. Other parameters such as $r_{o\_M_3}$ and $r_{o\_M_4}$ can be approximated to be very high thus the terms $1/r_{o\_M_3}$ and $1/r_{o\_M_4}$ can be considered negligible. Since MedRadio frequencies are considerably quite low in the RF spectrum, it can be assumed that the input impedance does not change by much going from low frequencies to MedRadio frequencies. Equation (5) therefore was used to estimate the transconductance of M_3 needed to present an input impedance of approximately 50 Ω. From this equation, the approximate value of required $g_{m\_M_3}$ was found to be 1 mS. With the value of $g_{m\_M_3}$ obtained, it was then possible to obtain the size of M_3 and its drain current.

Table III summarizes the chosen DC parameters, gate dimensions and transconductances for M_3 and M_4 transistors in the source-follower active shunt feedback network.

TABLE III: DC PARAMETERS, GATE DIMENSIONS AND TRANSCONDUCTANCES FOR M_3 AND M_4 TRANSISTORS IN THE SOURCE-FOLLOWER ACTIVE SHUNT FEEDBACK NETWORK

Parameter	M_3	M_4
Drain current, I_D	0.1 mA	0.1 mA
Drain-source voltage, V_{DS}	-0.6 V	-0.4 V
Gate-source voltage, V_{GS}	-0.6 V	-0.6 V
Gate voltage, V_G	0 V	0.4 V
Gate length, L	0.18 µm	0.18 µm
Gate width, W	19.68 µm	17.34 µm
Transconductance, g_m	1 mS	N/A

D. Design of Output Buffer and Integration with Main Driver and Feedback Section

For this MedRadio LNA, the input impedance is being taken care of by the active shunt feedback network. For the output, theoretically, another impedance matching circuit is required to match the high output impedance of the MedRadio LNA to 50 Ω. In the real MedRadio band receiver front-end application however, the amplified signal from the output of the LNA is channelled directly into the input of the downconverter mixer in the receiver front-end module. No output matching circuit is needed for the LNA. This downconverter mixer typically has a very high input impedance as the input terminal is normally the gate of a MOS transistor. As a result, the output impedance of the LNA is only slightly affected and hence, the gain at the output of the LNA also changes very slightly. To imitate this condition during testing of a standalone MedRadio LNA, a source-follower circuit can be utilized as an output buffer for the LNA. With this output buffer, the gain measured by the Network Analyzer will be fairly close to that at the output of the LNA.

One of the most common topologies for output buffer is the source-follower, which is essentially a common-drain amplifier. This topology is commonly used as output buffer due to its simple structure that only consists of a driving transistor and a source resistor or a current

source. Fig. 6 illustrates the schematic circuit diagram for the output buffer that was used together with the LNA in this work.

In Fig. 6, the structure of the output buffer consists of NMOS transistor M_5 as the driving transistor and NMOS transistor M_6 as the current source at the source of M_5. The voltage supply for this output buffer is V_{SOB}. Current I_{SOB} flows through M_5 and M_6 from V_{SOB}. The biasing voltages for M_5 and M_6 are also shown as well as biasing resistor R_4 and DC-blocking capacitors C_3 and C_6. R_4 prevents AC signals from being shorted to ground whilst C_3 and C_6 block DC currents from flowing into the transmission path. The incoming AC signals from the output of the LNA are fed into the gate of M_5 and the buffered signals are taken between the source of M_5 and the drain of M_6. Since both M_5 and M_6 are NMOS transistors, their bodies are connected to ground. For M_5, this implies that its source is at a higher potential than its body, thus some body effects such as increased threshold voltage will come into play.

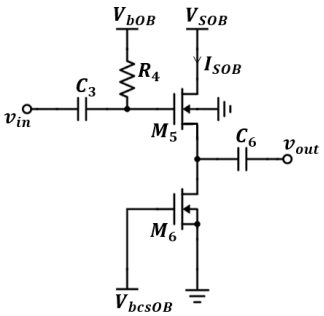

Fig. 6. Schematic circuit diagram for the output buffer used in this work.

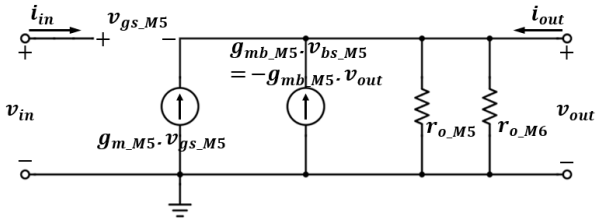

Fig. 7. Small-signal equivalent circuit for the output buffer.

The corresponding small-signal equivalent circuit for the output buffer is depicted in Fig. 7. In Figure 7, C_3, C_6, and R_4 have been omitted for simplicity since their values are considerably very large. The low-frequency small-signal gain of this output buffer can then be derived and approximated as:

$$A_v = \frac{g_{m\_M_5}}{g_{m\_M5} + g_{\mathrm{mb}\_M_5}} \tag{7}$$

where $g_{m\_M_5}$ is the transconductance of M_5 and $g_{\mathrm{mb}\_M_5}$ is the body transconductance of M_5. Equation (7) indicates that the output buffer's low-frequency small-signal gain will never become 1 as ideally-desired, but may approach unity with larger values of $g_{m\_M_5}$.

The main objective in the design of this output buffer was to obtain a reasonable gain to buffer the output signal from the LNA for measurements with a Network Analyzer. As previously mentioned, the gain of this output buffer can never reach the ideal unity. Based on (7), a high value of gain can be achieved by using a large value for M_5s' transconductance $g_{m\_M_5}$. Hence, a relatively large transconductance value of more than 10 mS was targeted for M_5.

Table IV summarizes the chosen DC parameters, gate dimensions and transconductances for M_5 and M_6 transistors in the source-follower output buffer. Fig. 8 illustrates the integration of this output buffer to the MedRadio LNA designed previously.

TABLE IV: DC PARAMETERS, GATE DIMENSIONS AND TRANSCONDUCTANCES FOR M_5 AND M_6 TRANSISTORS IN THE SOURCE-FOLLOWER OUTPUT BUFFER

Parameter	M_5	M_6
Drain current, I_D	6 mA	6 mA
Drain-source voltage, V_{DS}	0.9 V	1.1 V
Gate-source voltage, V_{GS}	0.9 V	0.7 V
Gate voltage, V_G	2 V	0.7 V
Gate length, L	0.18 µm	0.18 µm
Gate width, W	127 µm	134 µm
Transconductance, g_m	41 mS	N/A
Body transconductance, g_{mb}	5 mS	N/A

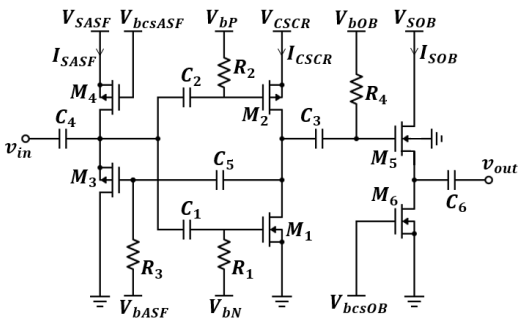

Fig. 8. Schematic circuit diagram of the MedRadio LNA with integrated output buffer.

E. Pre-Layout (Schematic) Simulation

The objective of pre-layout simulations was to provide an initial raw assessment on the performance of the MedRadio LNA. This was important to verify the functioning of the LNA circuit before proceeding with the physical layout design of the LNA.

The schematic circuit of the LNA with integrated output buffer was constructed in Cadence for schematic-level or pre-layout simulation. This is illustrated in Fig. 9.

In Fig. 9, bypass capacitors were added at all DC voltage points in the circuit. Schematically, these bypass capacitors do not affect the simulated performance of the LNA. However, for practical purpose, these bypass capacitors are needed to ground stray RF signals at the DC voltage points. This is to prevent the signals from going into the transmission path of the LNA. For all capacitors in this circuit, MOSCAPs were utilized to help reducing the size of the integrated circuit. All these MOSCAPs, except for the one at the input of the LNA, have a capacitance value of approximately 5 pF for coupling and bypassing purposes. The one at the input was tweaked to a lower value for input impedance matching of the LNA.

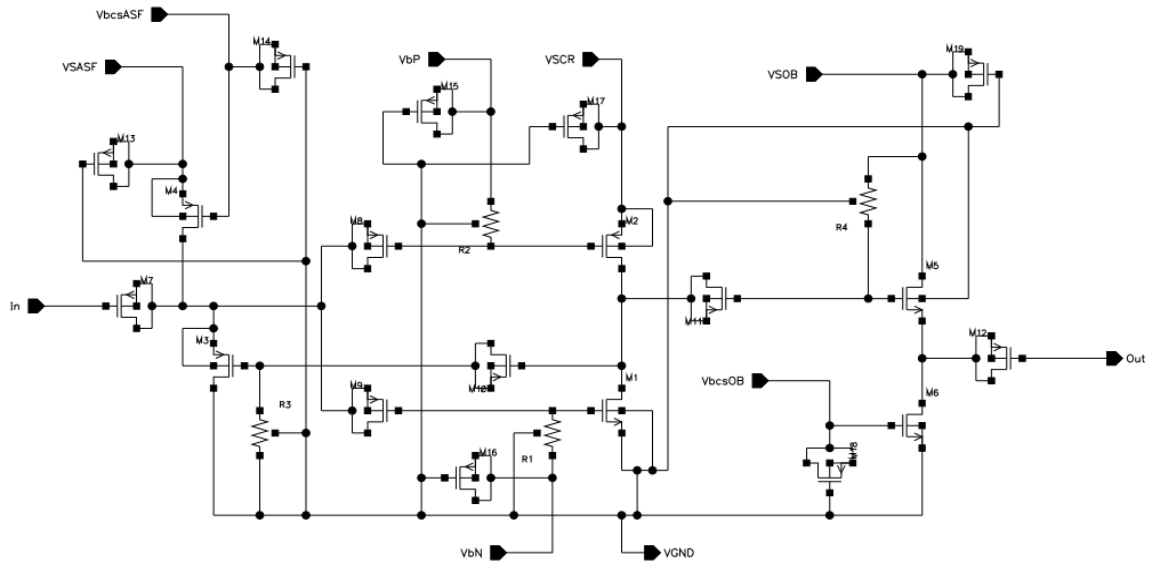

Fig. 9. Cadence circuit schematic for the MedRadio LNA with integrated output buffer.

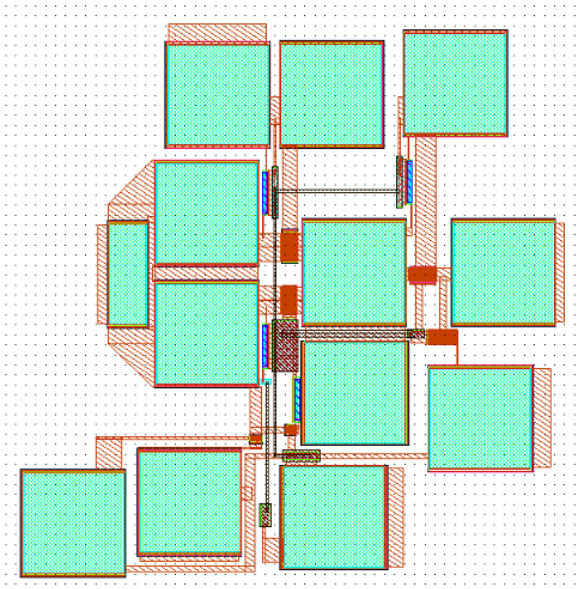

Fig. 10. Physical layout of the proposed MedRadio LNA with integrated output buffer.

F. Layout Design

The physical implementation of this MedRadio LNA circuit was carried out by designing the layout in Cadence Virtuoso. This layout is illustrated in Fig. 10.

Overall, this layout design only occupies about 0.08 mm^2 of space on the die. Without the output buffer, the total area occupied by the actual LNA is just 0.06 mm^2. This small size of the IC is largely due to the use of MOSCAPs as capacitors. MOSCAPs are actually MOS transistors (either NMOS or PMOS) that are used as capacitors. The capacitance value for all the MOSCAPs (except for the one at the input of the LNA) is limited to 5 pF as a trade-off for the small size. This is also the case for all the biasing resistors used in this LNA design, where the resistance value for all these resistors is limited to 150 kΩ. This is to prevent the resistors from being excessively long that they may affect space utilization within the IC layout.

V. Post-Layout Simulation Results

Post-layout simulations were carried out for gain, input return loss, noise figure, input-referred 1-dB compression point and input third-order intercept point with total DC power consumption of 0.5 mW. Fig. 11 illustrates the plots for post-layout simulated S_{21}, S_{11} and noise figure from 0 to 1000 MHz. Fig. 12 shows the plot for post-layout simulated output power versus input power to determine the post-layout simulated input-referred P_{1dB} of this proposed LNA. Fig. 13 by the way, illustrates the post-layout simulated output power versus input power plots of the fundamental tone at 403 MHz and the third-order intermodulation product at 402 MHz of this proposed LNA, with both plots being extrapolated to obtain the IIP_3.

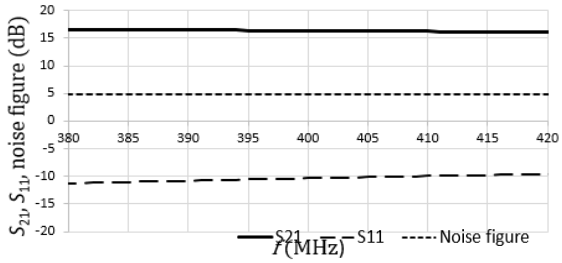

Fig. 11. Post-layout simulated S_{21}, S_{11} and noise figure plots for the proposed MedRadio band LNA.

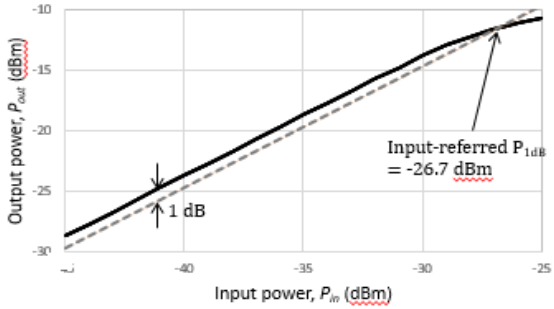

Fig. 12. Post-layout simulated output power versus input power plot to obtain the post-layout simulated input-referred P_{1dB} for the proposed MedRadio band LNA.

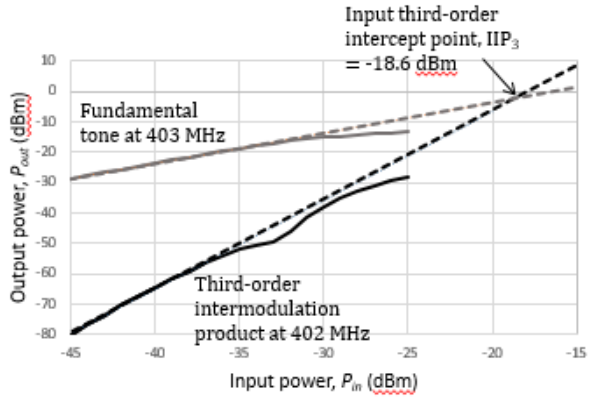

Fig. 13. Post-layout simulated output power versus input power plot to obtain the post-layout simulated input-referred P_{1dB} for the proposed MedRadio band LNA.

TABLE V: POST-LAYOUT SIMULATION RESULTS OF THE PROPOSED MEDRADIO LNA AND COMPARISON WITH TARGETED SPECIFICATIONS

Parameter	Post-layout simulation	Specification
Frequency range	401 MHz to 406 MHz	401 MHz to 406 MHz
DC power consumption, P_{DC}	0.5 mW	≤ 1.0 mW
Gain, A_v	16.3 dB	≥ 15 dB
Noise figure, NF	4.9 dB	≤ 6 dB
Input return loss, RL_{in}	10.1 dB	≥ 10 dB
Input-referred 1-dB compression point, IP_{1dB}	-26.7 dBm	≥ -30 dBm
Input third-order intercept point, IIP_3	-18.6 dBm	≥ -20 dBm
Die area, A_{die}	0.06 mm^2	≤ 0.1 mm^2

All post-layout simulation results of this proposed MedRadio LNA are summarized in Table V. Comparisons are made with the targeted specifications from Table I. Overall, all targeted specifications are met at post-layout level. However, the input return loss has virtually no margin to its targeted specification. It is therefore almost likely that the targeted specification for this parameter will not be met when the fabricated LNA die is tested.

In Table VI, the performance of this proposed MedRadio LNA is compared with that of some current state-of-the-art MedRadio LNAs. FOM or Figure of Merit in Table VI is a numerical expression representing the overall performance of the LNAs. Larger value of FOM indicates better overall performance. In this work, the FOM is defined as:

$$\text{FOM} = \frac{\text{gain (in magnitude)} \times \text{RL}_{\text{in}}\text{(in magnitude)}}{[P_{\text{DC}}\text{(in W)}]^2 \times \text{NF (in magnitude)} \times \left[A_{\text{die}}\text{(in m}^2\text{)}\right]^2} \quad (8)$$

In the FOM defined by (8), the numerator is the product of gain and input return loss, simply because high gain and high input return loss are desired characteristics of LNAs in general. The denominator on the other hand is the product of noise figure, squared power consumption and squared die area. Similar to high gain and high input return loss, low noise figure is also a desired characteristic for all LNAs. However, the power consumption and die area are squared in the denominator since these two are considered the main requirements of LNAs for biomedical applications. Squaring the power consumption and die area gives them more weightage over other parameters namely gain, input return loss and noise figure which are nevertheless still very important for LNAs in general.

TABLE VI: PERFORMANCE COMPARISON OF THE PROPOSED MEDRADIO LNA IN THIS WORK WITH SOME CURRENT STATE-OF-THE-ART LNA FOR MEDRADIO APPLICATIONS

Parameter	This work*	[4]	[9]	[10]
Technology	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS
P_{DC}(mW)	0.5	0.15	0.7	0.29
A_v (dB)	16.3	20	31	23
NF(dB)	4.9	2.8	5.8	3.1
RL_{in}(dB)	10.1	15	14	12
IP_{1dB}(dBm)	-26.7	N/A	-23	N/A
IIP_3(dBm)	-18.6	-8.1	N/A	-27.5
A_{die}(mm^2)	0.06	0.35	0.2	0.83
FOM	7.5×10^{21}	1.1×10^{22}	2.4×10^{21}	4.8×10^{20}

*Post-layout simulation results

In Table VI, the performance of the proposed LNA is fairly comparable with the other state-of-the-art LNAs for MedRadio applications in terms of power consumption, noise figure and die area. In particular, the small die area of only 0.06 mm^2 is quite a significant improvement in comparison to those of the previous designs. The gain and input return loss however are less comparable. These two parameters for the proposed LNA are the worst as compared to that for the other LNAs in Table VI. These two parameters are therefore very much likely to become even worse when the LNA is fabricated and measured. For overall performance, the FOM for the proposed LNA is very much comparable to the other state-of-the-art MedRadio LNAs in the table. It is the second highest amongst all the LNAs, only losing out to the work by [4]. The high FOM of the work by [4] is mostly due to its exceptionally low power consumption of just 0.15 mW.

VI. CONCLUSION

A low-power 0.18-µm CMOS LNA for MedRadio applications has been designed and verified through simulations. All design and simulation work for this proposed LNA were carried out in Cadence IC5 with Silterra's C18G CMOS technology Process Design Kit.

To achieve low-power operation with simultaneous high gain and low noise figure, this LNA utilizes complementary common-source current-reuse topology, with subthreshold biasing applied to the NMOS transistor of this configuration to further reduce the power consumption. This LNA also contains an active shunt feedback circuit as input matching network to provide a suitable input return loss. No output matching network is required for this LNA since its output is to be channelled directly into the downconverter mixer of a MedRadio band receiver front-end module. Therefore, an output buffer was designed and integrated with this LNA for test and measurement purpose. To minimize the die size of this LNA, inductorless circuit topology was employed together with the use of MOSCAPs as capacitors.

From its post-layout simulations with LNA die area of 0.06 mm^2 and simulated total DC power consumption of 0.5 mW, this LNA gives out simulated gain, input return loss and noise figure of 16.3 dB, 10.1 dB and 4.9 dB respectively throughout the MedRadio frequency range. For linearity, the simulated input-referred P_{1dB} of this LNA is –26.7 dBm while its simulated IIP_3 is –18.6 dBm. With these post-layout simulation results, all targeted specifications are met.

Generally, the post-layout simulated performance of this proposed LNA is fairly comparable to some current state-of-the-art LNAs for MedRadio applications. The small die area of only 0.06 mm^2 is a significant improvement in comparison to those of the previously reported MedRadio LNAs. However, the input return loss virtually has no margin to its specification. It is therefore highly likely that this specification will not be met when the proposed LNA is fabricated and tested at IC level.

All these parameters which are quite insignificant in comparison with those of the previous designs must be further improved at post-layout simulation level. With much improved performance at post-layout simulation level, more margins can be created towards the respective target specifications of the parameters. This will therefore increase the chances of achieving the specifications once the proposed LNA is fabricated and tested at IC level.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Both authors conducted the research. The first author wrote the paper and both authors had approved the final version.

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