A New Hybrid Multilevel Inverter with Extended Number of Voltage Steps

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***Abstract*—This paper presents and studies an improved multilevel inverter topology to produce higher voltage levels with reduced switching devices at the inverter output. The suggested topology is based on SCSS multilevel inverter. In this topology, DC sources are divided into two groups, inner group and outer group. The function of the outer dc source group is to create the square waveforms that are close in nature to the required output waveforms. However, the inner group is used to increase the number of the DC voltage levels to produce an output voltage close to the desired wave. This task is accomplished by arithmetic operation (addition or subtraction) of the value of the inner DC source with the blocks created by the outer group, respectively. A hybrid modulation scheme has been utilized to substantially reduce harmonics distortion. The performance of the proposed topology is then compared with other conventional and concurrent structures of multilevel inverter as well as evaluated by simulation results.**

***Index Terms*—Multilevel inverters, hybrid modulation scheme, harmonic distortion, reduce switched count, PLECS**

I. Introduction

Recently, more attention is given to multilevel inverters due to many advantages such as its low harmonic distortion of the output waveforms, low switching device voltage and current stress and reduced switching stress. Furthermore, they have increasingly employed in modern FACTS devices to improve the quality of power systems. Multilevel inverters are also used in electric and hybrid electric vehicles for efficient power conversion from DC to AC conversion [1]–[4]. Generally, the three main types of multilevel inverters are Neutral-Point Clamped or diode-clamped (NPC) [5], [6] Flying Capacitor (FC) [7], [8] and cascaded H-bridge inverters [4], [9]–[12]. In NPC, series capacitors are used at the input side to distribute the input dc link evenly between the power semiconductor devices. This results in lower output voltage distortion and lower potential stress across each device. Various techniques are suggested for controlling multilevel inverters, however, the most commonly used technique is Sinusoidal Pulse Width Modulation (SPWM) [13], [14]. To improve the sinusoidal waveform of the output voltage and decrease its harmonics content, the multilevel inverter output levels should increase. Notwithstanding, the drawbacks of increasing the multilevel inverter output levels are the difficult balancing of the DC-link voltage and the increasing number of clamping diodes required in NPC and FC[15]–[17].

One of the major limitations of these converter has been the use of higher number of switches. To overcome this issue, several topologies have been proposed in the literature. Hybrid inverters are some of the commonly proposed MLIs [18]–[21]. It consists of two parts the first part is a DC-DC converter which generates several levels of output in one polarity, the second part is an H-bridge which works as a polarity changer. Both parts combine to generate a multilevel voltage with dual polarity at the output. In addition, these converters can be configured in symmetrical and asymmetrical modes of dc voltage source selection. With symmetrical configuration, equal magnitude of dc voltage sources is used. With asymmetrical configured dc voltage sources, the magnitudes of dc voltage sources are not same which results in higher number of levels compare to symmetrical configured MLIs. Several hybrid topologies have been proposed considering both configurations. A bidirectional MLI is proposed in [22]. This topology includes the H-bridge for polarity change and requires three DC sources to generate 7 levels. In the proposed MLI involves a five-level DC/DC converter and H-bridge. It uses 4 capacitors to obtain 9 levels of output voltage. A switched-capacitor (SC) MLI is presented in [23] however, it also requires the use of H-bridge with two DC sources and one capacitor to generate 7 levels at the output. An MLI based on a modified H-bridge basic unit is presented in [24]. By cascading the H-bridge units,

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more number of levels can be generated but not all the available levels from the DC links available [24]–[26].

Another important aspect of the MLI topologies has been its practical applications. With the asymmetrical configuration, the variation of the magnitude of dc voltage sources makes them impractical due to unavailability of such dc voltage sources. The aim of this paper is to introduce an improved multilevel inverter topology that produces more levels at the inverter output with a minimum number of switching devices. The proposed topology is based on SCSS multilevel inverter in which the DC sources are divided into two groups, inner group, and outer group. The function of the outer dc source group is to generate the waveforms of square in nature which are close in the shape to the required output waveforms. However, the inner group of the proposed topology is used to enhance the quality of the output voltage by adding the voltage levels to the square block to produce smother sinusoidal wave. This task can be accomplished by connecting the voltage sources of inner and outer groups in additive or subtractive polarity. A hybrid modulation scheme has been utilized to substantially reduce harmonics distortion. The performance of the proposed topology is then compared with other conventional and concurrent topologies as well as evaluated by PLECS simulation. Modern topologies considered in this paper for comparison with the proposed one are Switched Series/Parallel Sources (SSPS)-based MLI [27], [28], Series-Connected Switched Sources (SCSS)-based MLI [29], [30], Cascaded Bipolar Switched cells (CBSC)-based MLI [31] and Packed-U Cell (PUC) topology [32]–[34]. Finally, the simulation results of the proposed topology are validated using experimental measurements.

The paper is organized as follows. Circuit and switching states are discussed in section II. Section III introduces the Hybrid modulation scheme. The power loss analysis has been provided in Section IV. The proposed topology with other conventional topologies, are compared in section V. Section VI illustrates the simulation results. Finally, the summary and conclusion are discussed in section VII.

II. Proposed Topology

Fig. 1 shows the proposed 11-level multilevel inverter topology that consists of four dc voltage sources and eleven unidirectional power switches. The power switches turn on and off states for the proposed topology are illustrated in Table I.

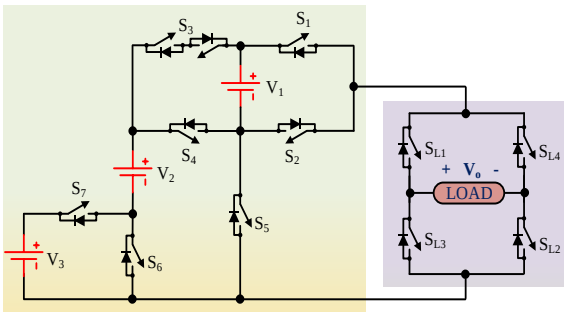


Fig. 1. 11-level multilevel inverter, n=2.

TABLE I: Switching Table

State	$V_o/V_{o,max}$, pu	V_o	Switches
1	0	0	2, 5
2	V_{dc}	V_1	1, 5
3	V_{dc}	V_2-V_1	2,3, 6
4	2 V_{dc}	V_2	1, 3, 6
5	2 V_{dc}	V_2	2, 4, 6
6	3 V_{dc}	V_2+V_1	1, 4, 6
7	3 V_{dc}	V_3+V_2-V_1	2, 3, 7
8	4 V_{dc}	V_3+V_2	2, 4, 7
9	4 V_{dc}	V_3+V_2	1, 3, 7
10	5 V_{dc}	V_3+V_2+V_1	1, 4, 7

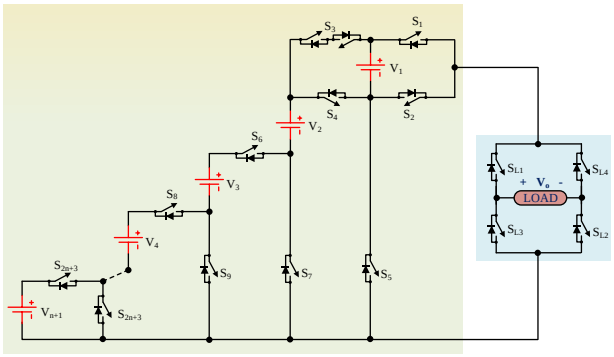


Fig. 2. Generalized structure of the proposed topology.

In order to generate higher voltage steps without addition of number of switches and dc voltage sources to the proposed topology, the values of the dc voltage sources are set to be configured in asymmetrical mode, i.e., the ratio of the dc sources is $V_1 = V_{dc}$, $V_2 = V_3 = V_4 = \cdots = V_{n+1} = 2V_{dc}$, where n is the number of cells.

Fig. 2 shows n-level multilevel inverter topology. The different formulation of proposed n-level topology are given as:

$$N_{steps} = 4n + 3 \tag{1}$$

$$N_{switch} = 2n + 7 \tag{2}$$

$$N_{source} = n + 1 \tag{3}$$

$$V_{o,max} = \sum_{k=1}^{n-1} V_k = (2n+1)V_{dc} \tag{4}$$

It is also very important to evaluate the variety of the values of dc voltage sources ($N_{variety}$) and the value of the blocking voltage of the switches (V_{block}) as these parameters are vital to determine the total cost of any multilevel inverter. To decrease the inverter's total cost, $N_{variety}$ and V_{block} must be reduced. The variety of dc voltage sources and the value of the blocking voltage of the switches are low, decrease [13]. $N_{variety}$ is given by

$$N_{variety} = 2 \tag{5}$$

with E_n denotes the blocked voltage by switch S_n, $V_{block,n}$ can be calculated using the following steps:

When n=2

$$E_1 = E_2 = V_{dc} \tag{6}$$

$$E_3 = 2V_{dc} \tag{7}$$

$$E_4 = E_7 = 2V_{dc} \tag{8}$$

$$E_5 = (2\times 2)V_{\text{dc}} \tag{9}$$

$$E_6 = (2\times 1)V_{\text{dc}} \tag{10}$$

$$E_{L1} = E_{L2} = E_{L3} = E_{L4} = 5V_{\text{dc}} \tag{11}$$

$$V_{\text{block},2} = E_1 + E_2 + E_3 + E_4 + E_5 + E_6 + E_7 + E_{L1} + E_{L2} + E_{L3} + E_{L4} = 34V_{\text{dc}} \tag{12}$$

When n=3

$$E_1 = E_2 = V_{\text{dc}} \tag{13}$$

$$E_3 = 2V_{\text{dc}} \tag{14}$$

$$E_4 = E_7 = E_9 = 2V_{\text{dc}} \tag{15}$$

$$E_5 = (2\times 3)V_{\text{dc}} \tag{16}$$

$$E_6 = (2\times 2)V_{\text{dc}} \tag{17}$$

$$E_8 = (2\times 1)V_{\text{dc}} \tag{18}$$

$$E_{L1} = E_{L2} = E_{L3} = E_{L4} = 7V_{\text{dc}} \tag{19}$$

$$V_{\text{block},3} = E_1 + E_2 + E_3 + E_4 + E_5 + E_6 + E_7 + E_8 + E_9 + E_{L1} + E_{L2} + E_{L3} + E_{L4} = 50V_{\text{dc}} \tag{20}$$

Therefore, in general, $V_{\text{block},n}$ has the following expression:

$$V_{\text{block},n} = 2\left(n^2 + 6n + 4 - \sum_{k=1}^{n} k\right)V_{\text{dc}} \tag{21}$$

III. Hybrid Modulation Scheme

In the hybrid modulation scheme, the switches operate at different frequencies. Inner switches modulation can be obtained by creating the wave shape of the area with a red color grid design as shown in Fig. 3 [13].

$$v_{\text{ref}} = V_1 \sin(2\pi ft) - 0.4\left[u(t-t_1) - u(t-t_8) - u(t-t_9) + u(t-t_{16})\right] - 0.4\left[u(t-t_3) - u(t-t_6) - u(t-t_{11}) + u(t-t_{14})\right] \tag{22}$$

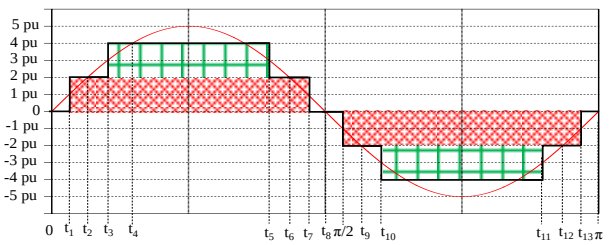


Fig. 3. Hybrid modulation PWM technique with two blocks in each half-cycle.

To obtain the general expression of v_{ref}, it is required to find the number of blocks per half-cycle as follows.

$$N_{\text{core}} = N_{\text{cells}} - 1 \tag{23}$$

In order to obtain the intervals of each block, it is necessary to calculate the peak of the blocks (V_{core}) and the number of starts and ends of the blocks per half-cycle (T_{core}), for example, t_1 and t_3. V_{core} and T_{core} can be calculated using the following equations:

$$V_{\text{core}} = \frac{1}{N_{\text{core}} + 0.5} \tag{24}$$

$$T_{\text{core}} = 4N_{\text{core}} \tag{25}$$

Therefore, the general expression of v_{ref} is

$$v_{\text{ref}} = V_1 \sin(2\pi ft) - V_{\text{core}}\left[\sum_{i=1,3,5,\ldots}^{\frac{T_{\text{core}}}{2}-1} u(t-t_i) - u(t-t_{i+T_{\text{core}}}) + \sum_{j=2,4,6,\ldots}^{\frac{T_{\text{core}}}{2}-2} u(t-t_{T_{\text{core}}-j}) - u(t-t_{2T_{\text{core}}-j})\right] \tag{26}$$

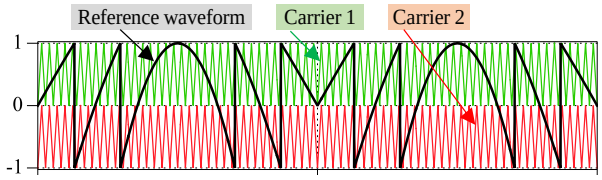


Fig. 4. Modified reference wave and the two carriers.

The reference wave v_{ref} is modulated using two triangular carriers, carrier 1 and carrier 2 as shown in Fig. 4.

Therefore, the modulation index m is defined as:

$$m = \frac{v_{\text{ref}}}{cr_{1,2(\text{peak})}} \tag{27}$$

where $0 \le m \le 1$.

One of the major key performance factors in evaluating the performance of the output waveform is the Total Harmonic Distortion index (THD) and can be calculated as follows.

$$\text{THD} = \frac{\sqrt{\sum_{n=3,5,7,\ldots}^{\infty} b_n}}{b_1} \tag{28}$$

where b_n is obtained using the following equation.

$$b_n = \frac{4V_{\text{dc}}}{n\pi}\left[1 + \sum_{i=1}^{N_{\text{levels}}-2} \cos(n\alpha_i)\right] \text{ for } n \text{ odd} \tag{29}$$

IV. Losses Calculation

In general, there are two kinds of losses are associated with the power semiconductor devices known as conduction losses and switching losses. The conduction losses of the IGBT ($P_{c,\text{IGBT}}(t)$) and diode ($P_{c,D}(t)$) are calculated as follows:

$$P_{c,\mathrm{IGBT}}(t)=\left[V_{\mathrm{sw}}+R_{\mathrm{sw}}(t)i^{\beta}(t)\right]i(t) \quad (30)$$

$$P_{c,D}(t)=\left[V_D+R_D i(t)\right]i(t) \quad (31)$$

where V_{sw} is the voltage drop in conduction mode of the switch, V_D is the voltage drop in conduction mode of the diode, R_{sw} is the equivalent resistance of the switch, R_D is the equivalent resistance of the diode, and β is a constant based om the manufacturer's specification of the switch.

If there are N_{sw} number of number of switches and N_D number of diodes in the considered path at instant t, the average conduction power loss (P_c) of the multilevel inverter is given as:

$$P_c=\frac{1}{2\pi}\int_0^{2\pi}\left[N_{\mathrm{IGBT}}(t)P_{c,\mathrm{IGBT}}(t)+N_D(t)P_{c,D}(t)\right]dt \quad (32)$$

Switching losses are associated with the transition of the state of the switches. By considering the linear variations of the voltage and current of the switches during the switching period, the turn-on ($E_{on,k}$) and turn-off ($E_{off,k}$) energy losses of switch k are given by [28], [29]:

$$E_{\mathrm{on},k}=\int_0^{t_{\mathrm{on}}}v(t)i(t)dt=\frac{1}{6}V_{\mathrm{SW},k}I't_{\mathrm{on}} \quad (33)$$

$$E_{\mathrm{off},k}=\int_0^{t_{\mathrm{off}}}v(t)i(t)dt=\frac{1}{6}V_{\mathrm{SW},k}It_{\mathrm{off}} \quad (34)$$

where I' is the current flowing through the switch after turning on, I is the current flowing through the switch before turning off, and $V_{sw,k}$ is the off-state voltage drop on the switch.

Therefore, the overall switching loss (P_{sw}) is given as:

$$P_{\mathrm{sw}}=f\sum_{k=1}^{N_{\mathrm{switch}}}\left(\sum_{i=1}^{N_{\mathrm{on},k}}E_{\mathrm{on},k,i}+\sum_{i=1}^{N_{\mathrm{off},k}}E_{\mathrm{off},k,i}\right) \quad (35)$$

where f is the fundamental frequency, $N_{on,k}$ and $N_{off,k}$ are the numbers of turn-on and turn-off during a fundamental cycle for k^{th} switch, $E_{on,k,i}$ is the average energy loss during the i^{th} turn-on of k^{th} switch, and $E_{off,k,i}$ is the average energy loss during the i^{th} turn-off of k^{th} switch.

Hence, the overall power loss of the multilevel inverter (P_{Loss}) is calculated as:

$$P_{\mathrm{Loss}}=P_c+P_{\mathrm{sw}} \quad (36)$$

The inverter efficiency (η) is

$$\eta=\frac{P_{\mathrm{out}}}{P_{\mathrm{in}}}=\frac{P_{\mathrm{out}}}{P_{\mathrm{out}}+P_{\mathrm{Loss}}} \quad (37)$$

where P_{out} is the output power and P_{in} is the input power.

For the estimation of the efficiency of the proposed topology, PLECS software has been used using (30)-(37). In PLECS, the power semiconductor devices are used with their thermal modeling for the accurate measurement of the power losses. Fig. 5 shows the curve relating the efficiency with the output power. The maximum efficiency of the proposed topology is 98.1% at the output power of 400W. Furthermore, the power loss distribution of different switches have also been provided in Table II with different loading conditions.

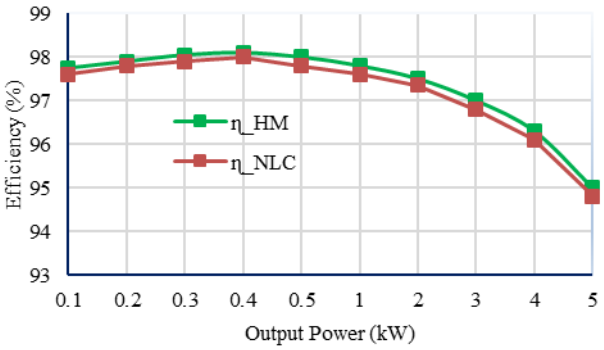


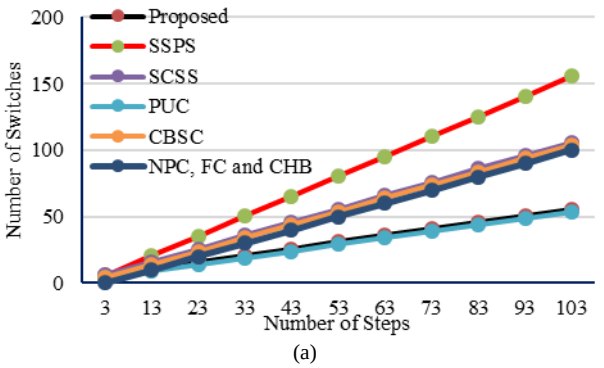
Fig. 5. Efficiency vs output power curve.

TABLE II: POWER LOSS DISTRIBUTION OF THE PROPOSED TOPOLOGY

Power Loss of	Output load	
	Z = 100Ω	Z = 100Ω + 100mH
Switch S_1	2.01	1.81
Switch S_2	2.01	1.81
Switch S_3	0.4497	0.439
Switch S_4	2.404	2.05
Switch S_5	0.121	0.210
Switch S_6	0.6289	0.5947
Switch S_7	2.0585	1.7793
Switch S_{L1}	1.3326	1.23
Switch S_{L2}	1.3326	1.23
Switch S_{L3}	1.3326	1.23
Switch S_{L4}	1.3326	1.23

V. COMPARISON PROCESS

In this section, a comparison has been carried out between the proposed topology and other modern topologies including SSPS, SCSS, PUC, and CBSC along with conventional NPC, FC and CHB. The relationships between N_{switch}/N_{source} and N_{steps}, are given in Table III. Fig. 6 depicts the variation of number of switches and number of sources against number of steps. From Fig. 6, it is clear that the proposed topology requires a lower number of switches and dc voltage sources compare to all other classical topologies used for the comparison.



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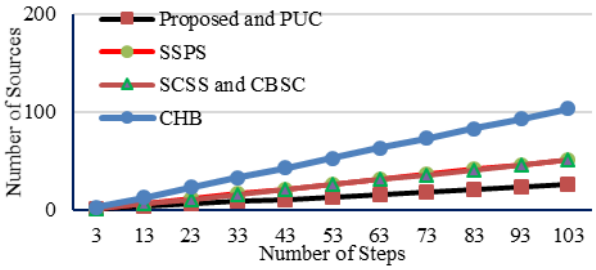


(b)

Fig. 6. Comparison of (a) number of switches and (b) number of sources with respect to number of steps.

TABLE III: COMPARISON TABLE

Topology	N_{source}	N_{switch}	$N_{variety}$
NPC, and FC	1	N_{steps}–3	1
CHB	N_{steps}	N_{steps}–3	1
SSPS	$\frac{N_{steps}}{2}$	$\frac{3N_{steps}-6}{2}+4$	1
SCSS	$\frac{N_{steps}-1}{2}$	N_{steps}–3	1
PUC	$\frac{N_{steps}+1}{4}$	$\frac{N_{steps}+5}{2}$	$\frac{N_{steps}+1}{4}$
CBSC	$\frac{N_{steps}-1}{2}$	$(N_{steps}+1)^*$	1
Proposed	$\frac{N_{steps}+1}{4}$	$\frac{N_{steps}+9}{2}$	2

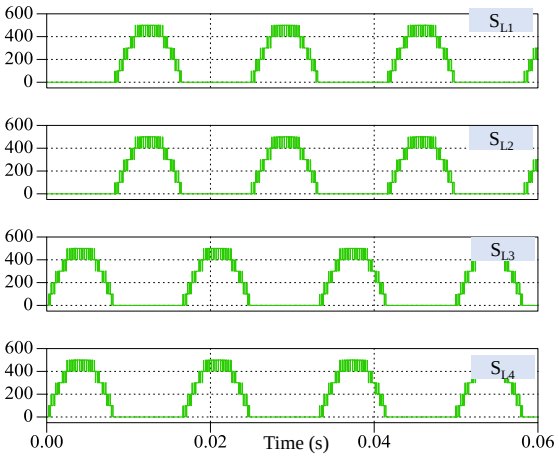
*Bidirectional switches

VI. SIMULATION RESULTS

The proposed model is simulated using PLECS for the 11 level output voltage. The modulation index m = 1 while the modulation frequency f_m is set to be 3600 Hz. The different parameters used for the simulation has been given in Table IV.

TABLE IV: SIMULATION PARAMETERS

Parameter	Value
DC voltage source	100 V, 200 V
Output frequency	60 Hz
Carrier frequency	3600
Resistive load	100Ω
Inductive load	100mH



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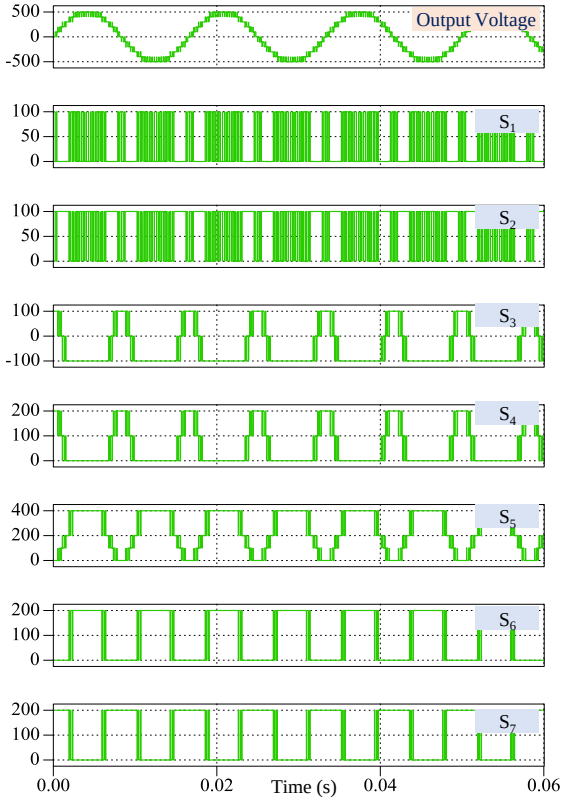
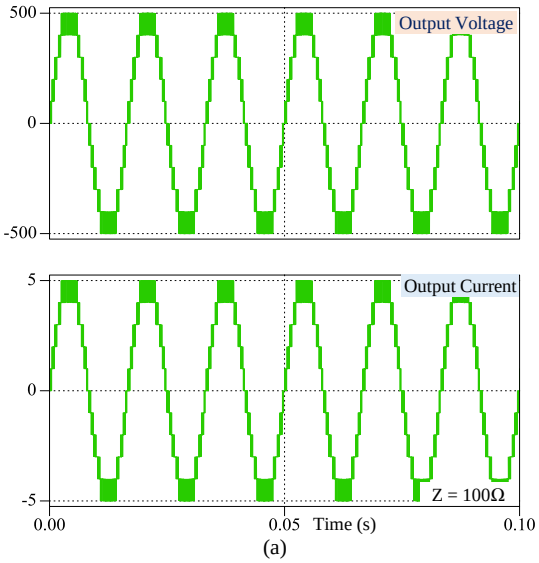


(b)

Fig. 7. Simulation results of (a) voltage stress of switches of H-bridge and (b) output voltage and voltage stress of switches S_1 - S_7.

With the voltage source magnitude of V_1 = 100 V, V_2 = V_3 = 200 V, the peak of the 11 level output voltage is 500 V with a voltage step of 100 V. Fig. 7 (a) depicts the voltage stress of four switches configured in H-bridge used for the polarity change. All these four switches have to withstand the maximum voltage of 500 V. Fig. 7 (b) illustrates the output voltage with the voltage stress of switches S_1 to S_7. The voltage stress across the switches S_1-S_3 has a value of V_1, i.e. 100 V. Similarly, the voltage stress of switches S_4 to S_7 has a value equal to $2V_{dc}$, i.e., 200 V.



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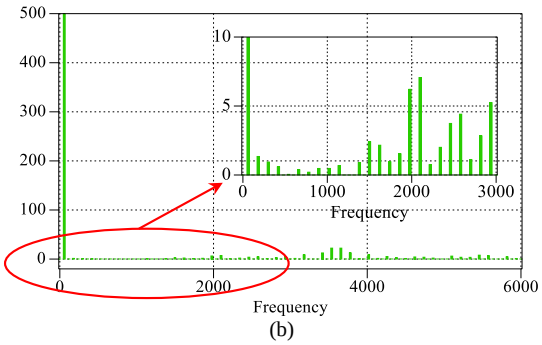
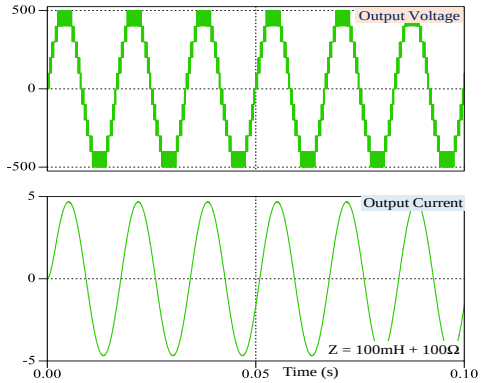


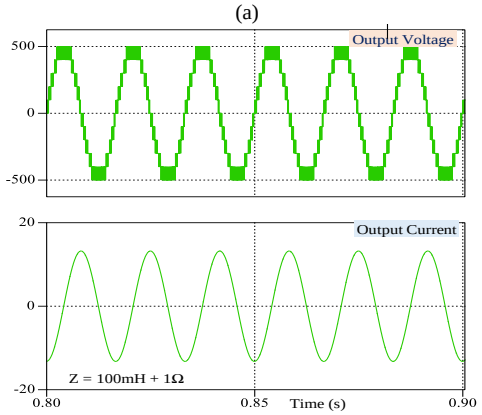
(b)

Fig. 8. Simulation results of (a) output voltage and current with unity pf and (b) FFT of the output voltage.

The proposed topology has been tested with different loading conditions. Fig. 8 (a) shows the output voltage and current with unity power factor (pf). A resistive load of 100 Ω is connected across the load terminals. This gives the peak value of the load current as 5 A. Furthermore, the THD spectrum of the output voltage has been depicted in Fig 8 (b). With 11 level output voltage, the voltage THD comes out to be 9.46%.



(a)

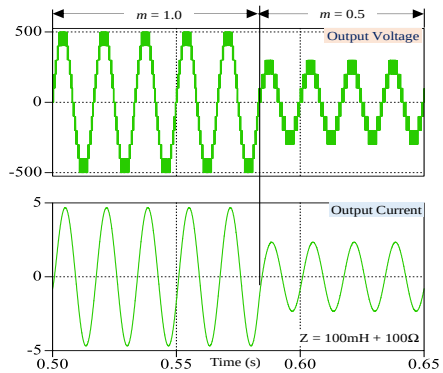


(b)

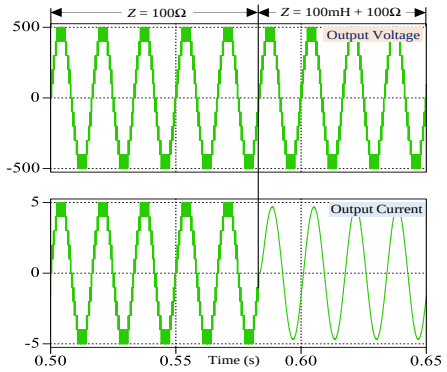
Fig. 9. Output voltage and current with pf of (a) 0.95 and (b) 0.03.

In addition to the unity pf load, the proposed topology has been validated using loads of different values of power factor. The voltage and current waveforms with a power factor of 0.95 and 0.03 have been illustrated in Fig. 9 (a) and (b) respectively.

Furthermore, the proposed topology has been validated using the dynamic conditions. Fig. 10 (a) shows the waveforms of output voltage and current with the change of modulation index. The modulation index is changed from 1.0 to 0.5 with the series connected resistive-inductive load of Z=100 mH+100 Ω. A change of load type has also been considered. Fig. 10 (b) shows the output quantity with the change of load from a purely resistive load of 100 Ω to the resistive-inductive load of Z=100 mH+100 Ω. In all these dynamic conditions, a satisfactory performance of the proposed topology has been obtained.



(a)



(b)

Fig. 10. Output voltage and current with (a) change of modulation index from 1.0 to 0.5 and (b) change of load.

VII. Conclusion

An improved multilevel inverter with more levels and less number of switching devices at the inverter output was introduced in this paper. The DC sources of the proposed topology are divided into two groups, inner group, which is used to produce the higher number of the DC voltage levels to produce smother wave, and outer group employed for building up square waveforms or blocks that are close in form to the required output waveforms. Adding/subtracting the dc voltage sources of the inner block to/from the blocks created by the outer group was used to accomplish the required task. The performance of the proposed topology was also compared with conventional and concurrent topologies. PLECS simulation program was employed to evaluate the performance of the proposed topology.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Hussain Bassi and Muhyaddin Rawa conducted the conceptualization and methodology; Hussain Bassi

developed and validated the software; Muhyaddin Rawa conducted the formal analysis and investigation; Hussain Bassi and Muhyaddin Rawa wrote the manuscript; Hussain Bassi reviewed and edited the final paper; Muhyaddin Rawa conducted the visualization of the final paper. All authors have read and agreed to the published version of the manuscript.

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