Realization with Fabrication of Double-Gate MOSFET Based Third Order High Pass Filter

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Abstract—**This research work designs a third order high pass filter with the replacement of traditional MOSFET and amplifiers with double-gate (DG) MOSFET. A theoretical background for the fundamental concepts involved in this work has been analyzed. Thereafter, mathematical analysis of circuit design based on the fundamental concepts has been conducted, simulated, and finally fabricated. The objective of this research work is to improve the filter specifications via application of DG MOSFETs. The system has been designed for corner frequency (f_c) = 10 kHz, the gain ≥ unity. The components in the stopband ($f < 0.01f_c$) have at least −20 dB attenuation with the bandwidth greater than 1.5 MHz.**

Index Terms—**Double-gate MOSFET, filter design, gate engineering, high pass filter, microelectronics, transistor, VLSI**

I. INTRODUCTION

Filters are generally classified by their function as low pass, high pass, band pass, and band stop etc. [1]-[3]. High pass filters (HPFs) can be designed using different methodologies including cascade, multiple-loop feedback, or the ladder simulation method [4], [5]. The high pass filters are widely used in audio electronics to reduce low-level noise, amplification of high frequency signals, elimination of rumble distortions, etc. These filters are designed using amplifiers. The filter performance is determined by its various parameters [6]-[8]. Adjusting the components and utilizing the application of double-gate (DG) MOSFET technology, the parameters such that the overall performance is improved [9], [10].

Denisenko *et al.* [11] have designed a third order low pass RC filter for practical use as a spectrum limiter at the input of various analogy-to-digital converters. The third order high pass harmonic filter has been widely used in industry. Ding *et al.* [12] have the complete design method along with simple design formulas. It's objective is to address the design gap by presenting a complete design method for the third order high pass filter. Jie *et al.* [13] have designed a third order high pass filter using the second generation current transmission device, which has low power consumption, strong anti-interference, and easy integration. Jiang *et al.* [14] have proposed an improved third order generalized integral flux observer, theoretical analysis shows that it can effectively eliminate the dc and high order components in the estimated rotor flux without any negative effect on the amplitude and phase angle of the fundamental waveform. Jerabek *et al.* [15] have designed the fractional order low pass filter and fractional order highpass filter based on follow the leader feedback topology to control the key parameters electronically. Aleema *et al.* [16] have derived the third order damped filter with equal and unequal capacitors and realized the relations among their circuit parameters. Then the optimal design problem of the two third order high pass filters was formulated regarding these expressions to minimize the filter cost.

Lulec *et al.* [17] have designed a third order filter which has cutoff frequency of 540 kHz, an integrated input referred noise of 17 μV and out-of-band IIP$_3$ of 55 dBm, while consuming 150 μW in the phase clock generator. Naidoo *and* Srivastava [18] have designed a third order active high pass filter with the cylindrical surrounding double-gate (CSDG) MOSFET for the cutoff frequency 0.3 THz, gain −41.848 dB. Comparing this gain with the gain of −43.12 dB that was achieved with the traditional transistor based circuit, the performance was improved. Kardoulaki *et al.* [19] have presented the results from CMOS hyperbolic-sine (sinh) filters fabricated in a commercially available 0.35-mm CMOS technology. Sawigun *et al.* [20] have design and fabricated a compact nano-power fourth order band pass filter operating at 0.5 V supply with adjustable centre frequency range from 125 Hz to 16 kHz in 180-nm CMOS IC technology. This filter was cascaded second order circuit cells and achieved 1 kHz center frequency, dynamic range of 55 dB, and 2 nW power consumption. Silva *et al.* [21] have discussed the applicability of a compact CMOS current-mode companding integrator in the design of analog continuous-time filters with high linearity in 130-nm CMOS technology with 90 μm^2 total active area. It performs a useful frequency bandwidth of up to 4 MHz and a third order intermodulation distortion smaller than −47 dB for input amplitudes ranging from 0.1 μA to 1 μA. Pinto *et al.* [22] have designd a model of fifth order Butterworth low pass filter, implemented in a 130-nm CMOS technology which operate in weak inversion supplied with 0.25 V and consumes 603 nW.
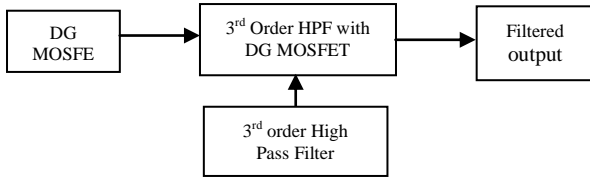
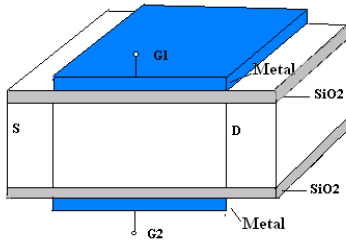Fig. 1. Process for the design of DG MOSFET based 3rd order filter.

Fig. 2. Schematic of the Double-Gate MOSFET [25]. (S: Source, D: Drain, G_1 and G_2: Gate-1 and gate-2, SiO_2: Silicon di-oxide).

Naidoo and Srivastava [23] have analyzed the steps involved in the design and simulation of third order active high pass filter for 100 GHz (0.1 THz). This filter used the operational amplifier for the first stage and transistor for the further stage. To further extend this work, Naidoo and Srivastava [24] have used the CSDG MOSFET. However, these existing works have not used DG MOSFET. To extend these works, in the present research work authors have designed the third order high pass filter with the help of DG MOSFET. Therefore, Butterworth filter of third order has been designed as it satisfies various requirements such as passband operation and improved transition band characteristics. The design process highlights the specifications such that additional filters may be designed for varying specifications. The system is designed for corner frequency (f_c) = 10 kHz. The gain of designed system is $\geq$ unity, the stopband ($f < 0.01f_c$) has at least -20 dB attenuation and the bandwidth is greater than 1.5 MHz.

This research paper is organized as follows. Section II discusses the basic theory of the DG MOSFETs and HPFs. Section III represents the modeling of the system, which is applied to design the third order HPF and proposed circuit. Section IV details the parameters calculations and simulations. Fabricated circuit design is discussed in the Section V and its implementation and testing are analyzed in Section VI. Finally, Section VII concludes the work and recommends the future aspects.

II. BASICS OF DOUBLE-GATE MOSFET AND HIGH PASS FILTERS

Some basics of the model (DG MOSFET and filter) used in this research work are discussed in this section. Since two models used have wide specifications and applications, authors restrict the discussion related to the specific proposed design. Fig. 1 represents the process flow of this design.

A. Double-Gate (DG) MOSFET and It's Small Signal Model

The basic structure of a MOSFET has three terminals: the gate (G), drain (D), and source (S). The DG MOSFET

has four terminals with two of them functioning as gate terminals as shown in Fig. 2 [25], [26]. The performance and packaging density of a MOSFET are inversely proportional to its physical parameters such as channel length and the gate metal oxide thickness. However, limiting factors known as Short Channel Effects (SCEs) play an influential role in negatively affecting the performance of the MOSFET [27]-[29]. These include the threshold voltage, ON and OFF currents, and the sub-threshold slope. Also, the carrier mobility decreases and threshold voltage roll-off occurs as the length of the channel decreases. The DG MOSFETs are more capable in an electrostatic sense to their single-gate counterpart. In the global semiconductor industry, the downscaling of transistors can be observed to be an ongoing trend, thus technologies such as the DG MOSFETs, which allow for improvement upon characteristics at small scales, are very suitable.

The two gates allow the better control of the channel in comparison to one gate. At low dimensions, the threshold voltages will be lower, and the MOSFET can handle a low voltage range. This voltage range may not be effective in switching the MOSFET ON or OFF, the DG MOSFET allows the better control of this. The short channel effects in the DG MOSFET are decreased allowing for downscaling up to 10 nm for the length of the Gate.

The transistor can be used to model the operational amplifier which performs as an active component of filter. The active filters allow the easier tuning and adjustability as well as generating a gain, which allows for better performance concerning certain parameters [30], [31]. The active filter decreases the loading effects and allows for the decrease in size of the circuit. The use of a transistor element instead of an operational amplifier allows the decrease in size and complexity of the circuit
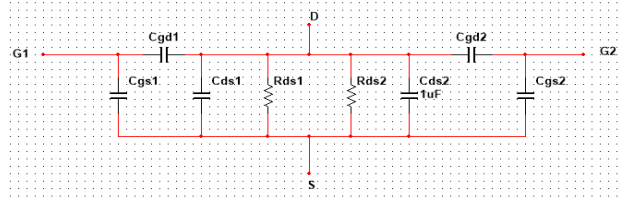
(a) DG MOSFET high frequency model.
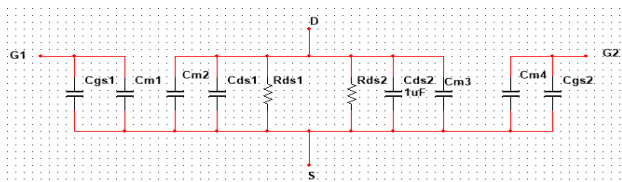
(b) DG MOSFET high frequency model using Millers theorem
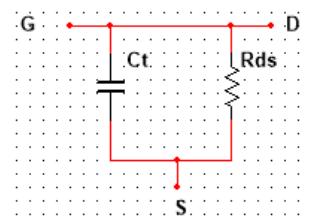
(c) DG MOSFET simplified high frequency model

Fig. 3. Small signal model of the DG MOSFET.

as well greater design capabilities. The MOSFET also uses low power and has high input impedance. The DG MOSFET offers greater electrostatic capabilities at downscaled sizes. The power efficiency is greater than the traditional MOSFET, as well it's switching capabilities. At low voltage operation, the DG MOSFETs generate less noise/error compared to the basic MOSFETs. A high frequency model can be formulated utilizing the capacitances found using the terminal charges [32], [33]. The various capacitances and resistances are labeled between the terminals, hence a model can be established as shown in Fig. 3. The gain is given by $A_v = -g_m R_{ds}$.

Capacitances in parallel can be easily combined, but for capacitances in series (both terminals not connected to ground), Miller's theorem can be used to split the capacitance in question allowing for mathematical analysis [27], [34], [35] as $C_1 = C(1-A_v)$ and $C_2 = C(1-1/A_v)$ and $g_m R_{ds} >> 1$. Therefore:

$$\begin{cases} C_{m1} = C_{gd1}(1-A_v) = C_{gd1}(1+g_m R_{ds}) \\ C_{m2} = C_{gd1}(1-\dfrac{1}{A_v}) = C_{gd1}(1+\dfrac{1}{g_m R_{ds}}) \approx C_{gd1} \\ C_{m3} = C_{gd2}(1-A_v) = C_{gd2}(1+g_m R_{ds}) \\ C_{m4} = C_{gd2}(1-\dfrac{1}{A_v}) = C_{gd2}(1+\dfrac{1}{g_m R_{ds}}) \approx C_{gd2} \end{cases} \quad (1)$$

where A_v and g_m are the voltage gain and trans-conductance, respectively. R_{ds} and C_{gd} are the resistance between drain and source terminal and capacitance between gate to drain, respectively. Here m denotes the Miller equivalent as shown in Fig. 3 (b). To calculate the equivalent capacitance (C_t) of this circuit, the intermediary capacitances have been formulated in (2) and then finalized as:

$$\begin{cases} C_1 = C_{gs1} + C_{m1} \\ C_2 = C_{m2} + C_{ds1} + C_{ds2} + C_{m3} \\ C_3 = C_{m4} + C_{gs2} \\ C_t = C_1 + C_2 + C_3 \end{cases} \quad (2)$$

Therefore −3 dB cutoff (the upper threshold) frequency will be

$$f_{cutoff} = \frac{1}{2\pi\tau} = \frac{1}{2\pi C_t R_{ds}} \quad (3)$$

B. Fundamental Concepts of High Pass Filters

Filter is designed to remove unwanted signal components from an input signal [6]-[8], [36], [37]. The term passband refers to the frequency range of which the filter allows the signal through and likewise stopband relates to the frequency range that the filter blocks off. For a non-ideal filter, a transition band exists. This is the frequency band between the stopband and the passband, i.e. signal components here are not fully blocked or passed through. Stopband attenuation (A_{min}) relates to the extent to which a filter blocks (attenuates) signal components in the stopband. Maximum ripple in the

passband (A_{max}) is the range of magnitudes possible in the passband [38]-[40].

A HPF is usually modeled as a linear time-invariant system, hence the stopband frequency range is that from zero to the stopband edge frequency and the pass band frequency range is from the passband edge frequency to the upper limits that can be processed. The degree of attenuation in the stopband and the cutoff frequency is determined when designing the filter [41]-[43]. HPFs are used in audio systems to separate and direct higher frequency signals to specific speakers as well as in mixing consoles for controlling attenuation to high frequencies and also AC coupling for protection of power amplifiers. The HPFs are also widely used in image processing for noise reduction, image adjustments, and communication systems involving signal communication across varying frequency bands.

III. MODELING OF THIRD ORDER HIGH PASS FILTER WITH DG MOSFET AND ITS PARAMETERS
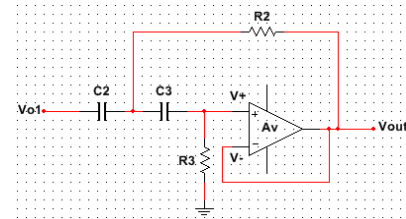
A. Basic Active Filter

An active filter can be realized by the use of active components such as transistors or amplifiers [21], [27], [29], [42]-[44]. This allows for improvement towards physical characteristics such as cost and performance. A first order non-inverting active filter with some gain has been implemented as shown in Fig. 4 (a), which is a basic cell for this research work. The DC voltage gain is given by $k = 1 + R_5 / R_4$. Hence the transfer function and cutoff frequency relation is

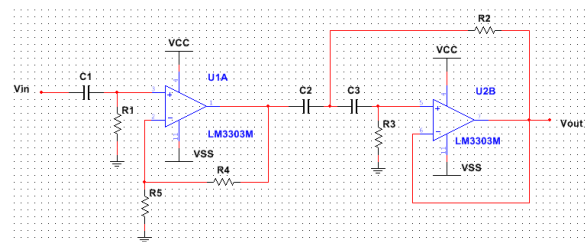$$\frac{V_1}{V_i} = k \frac{s}{s+(1/C_1 R_1)} = \left(1+\frac{R_5}{R_4}\right)\frac{s}{s+2\pi f_{c1}} \quad (4)$$
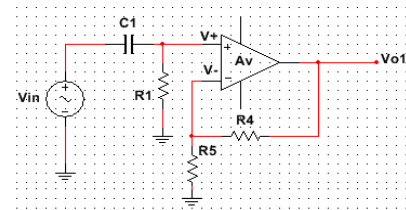
(a) 1st order active HPF

(b) 2nd order active HPF

(c) Third order active HPF

Fig. 4. Basic circuits of the high pass filters.

For the 2nd order high pass active filter, assume unity gain is implemented, i.e. no R_4 or R_5 used (Fig. 4 (b)). Using Kirchoff's current law $i_2 = i_3 + i_4$ and Ohm's law for each current [27], [44]:

$$i_2 = (V_i - V_2)sC_2, \quad i_3 = \frac{V_2 - V_o}{R_2}, \quad i_4 = (V_2 - V_o)sC_3 \quad (5)$$

To remove the V_2 element, we need to take the voltage at the positive input of the operational amplifier. As the DC voltage gain is unity, this voltage is simply V_o, due to feedback. Using Ohm's law and combining the nodal analysis, the transfer function is generated as follows:

$$T(s) = \frac{V_o}{V_i} = \frac{s^2 C_2 C_3 R_2 R_3}{s^2 C_2 C_3 R_2 R_3 + s R_2 (C_2 + C_3) + 1}$$

$$= \frac{s^2}{s^2 + s \frac{1}{R_3} \left(\frac{1}{C_3} + \frac{1}{C_2} \right) + \frac{1}{C_2 C_3 R_2 R_3}} \quad (6)$$
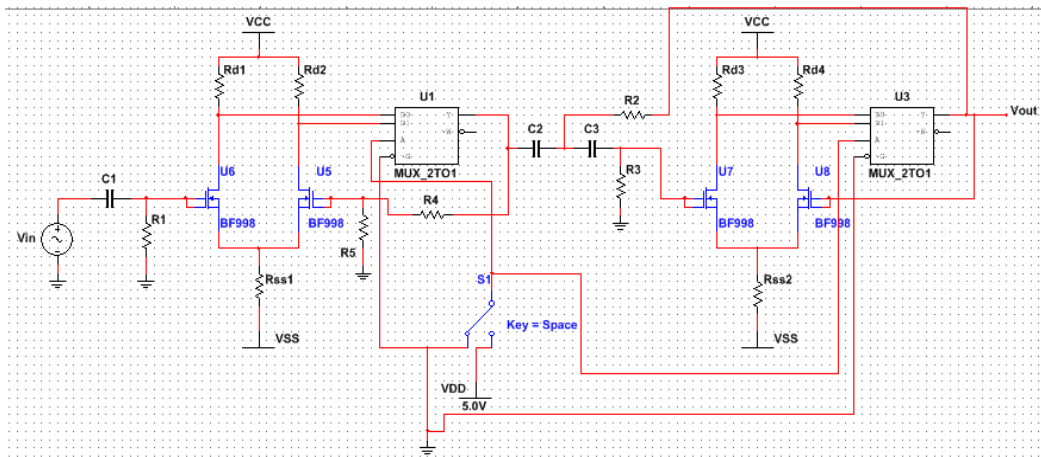
In (6) for simplification, the term $1/C_2 C_3 R_2 R_3$ can be replaced by f_{c2} using:

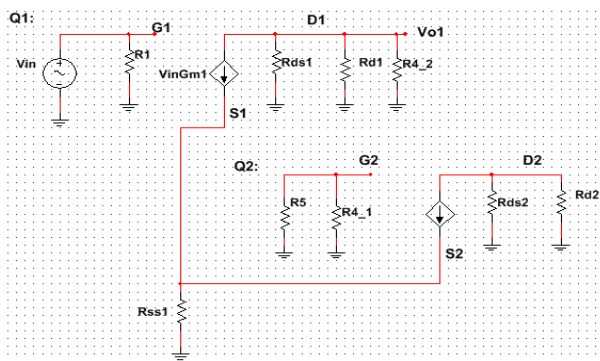$$f_{c2} = \frac{1}{2\pi} \sqrt{\frac{1}{C_2 C_3 R_2 R_3}}$$

The 3rd order active high pass filter comprises of an active 1st order HPF cascaded with an active 2nd order HPF, as shown in Fig. 4(c). For component calculations, the preset coefficients for either Bessel or Butterworth filters can be used [31], [37]-[40], [44], [45]. The circuit is formed by cascading the active 1st order HPF circuit with the active 2nd order HPF circuit. The overall transfer function is expressed in (7).

B. Proposed 3rd Order HPF Using DG MOSFET

The DG MOSFET based novel differential amplifier circuits with multiplexers has been implemented in place of operational amplifiers. The output of the differential amplifier is taken after the multiplexers as shown in Fig. 5(a).

$$T(s) = T_{1st}(s) T_{2nd}(s) = k_1 \frac{s}{s + \frac{1}{C_1 R_1}} \cdot \frac{s^2}{s^2 + s \left(\frac{1}{C_3 R_3} + \frac{1}{C_2 R_3} \right) + \frac{1}{C_2 C_3 R_2 R_3}}$$

$$= \frac{k_1 s^3}{s^3 + s^2 \left(\frac{1}{C_1 R_1} + \frac{1}{C_3 R_3} + \frac{1}{C_2 R_3} \right) + s \left(\frac{1}{C_1 C_3 R_1 R_3} + \frac{1}{C_1 C_2 R_1 R_3} + \frac{1}{C_2 C_3 R_2 R_3} \right) + \frac{1}{C_1 C_2 C_3 R_1 R_2 R_3}} \quad (7)$$

(a) DG MOSFET based 3rd order high pass filter

(b) Small signal model (1st order)
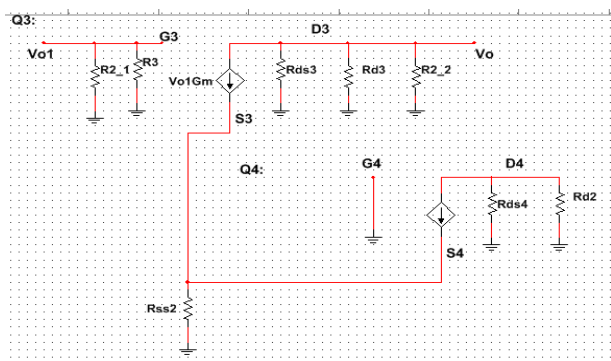
(c) Small signal analysis (2nd order)

Fig. 5. Proposed 3rd order high pass filter based on DG MOSFET.

The small signal model of proposed device with the DG MOSFET has been used for the analysis [46]-[48]. In this research work for small signal modeling, capacitors are short circuited. The input for transistor Q_2 is grounded, with a feedback component. Hence, a short circuit (zero voltage) can be presumed to exist between the source and gate terminals. The gain can be obtained by using Kirchoff's voltage law and analyzing the connections of resistors as:

$$\frac{V_{o1}}{V_{in}} = -\frac{1}{2}\frac{V_{in}G_{m1}(R_{ds1} \| R_{d1} \| R_{4\_2} \| R_{ss1} \| R_{ds2} \| R_{d2})}{V_{in}} \quad (8)$$

To simplify (8), following values have been replaced:

$$G_{m1} = G_m, \ R_{d1} = R_{d2} = R_d, \ R_{ds1} = R_{ds2} = R_{ds}$$

Also, for the parallel combinations of resistances of equal value, it can be simplified to $R_x \| R_x = R_x/2$. Therefore, the gain of (8) is simplifies to:

$$\frac{V_{o1}}{V_{in}} = -\frac{1}{2}G_{m1}\left(\frac{R_{ds}}{2} \| \frac{R_d}{2} \| R_{4\_2} \| R_{ss1}\right) \quad (9)$$

Resistance (R_{ds}) is very high relative to the other resistances, hence (9) can be further simplified to:

$$\frac{V_{o1}}{V_{in}} = -\frac{1}{2}G_{m1}\left(\frac{R_d}{2} \| R_{4\_2} \| R_{ss1}\right) \quad (10)$$

The gain analysis has been conducted with similar symmetry concerning resistors, hence:

$$\frac{V_{out}}{V_{o1}} = -\frac{1}{2}\frac{V_{o1}G_m(R_{ds3} \| R_{d3} \| R_{2\_2} \| R_{ss2} \| R_{ds4} \| R_{d4})}{V_{o1}} \quad (11)$$

The resistances allow for simplification are $R_{ds3} = R_{ds4} = R_{ds}$ and $R_{d3} = R_{d4} = R_d$; resulting in a simplified gain:

$$\frac{V_{out}}{V_{o1}} = -\frac{1}{2}G_m\left(\frac{R_{ds}}{2} \| \frac{R_d}{2} \| R_{2\_2} \| R_{ss2}\right)$$

$$\frac{R_{ds}}{2} \gg \frac{R_d}{2} \| R_{4_2} \| \frac{R_{ss}}{2} \quad (12)$$

$$A_{V2} = \frac{V_{out}}{V_{o1}} = -\frac{1}{2}G_m\left(\| \frac{R_d}{2} \| R_{2\_2} \| R_{ss2}\right)$$

Therefore, the transfer function is given by

$$T(s) = \frac{A_V s^2}{s^2 + s\left(\dfrac{1}{R_2C_2} + \dfrac{1}{R_3C_3} + \dfrac{(1-A_V)}{R_2C_2}\right) + \dfrac{1}{R_2R_3C_2C_3}} \quad (13)$$

and the magnitude response is

$$|T(j\omega)| =$$

$$\frac{|A_V|\omega^2}{\sqrt{\left(\dfrac{1}{R_2R_3C_2C_3} - \omega^2\right)^2 + \left(\omega\left(\dfrac{1}{R_2C_2} + \dfrac{1}{R_3C_3} + \dfrac{1-|A_V|}{R_2C_2}\right)\right)^2}} \quad (14)$$

When cascading the stages together as shown in Fig. 5 (a), the loading effect at the connection between the stages exists. This is because the input of the second stage affects the output of the first stage and vice versa. The gain A_{v2} is also adjusted accordingly:

$$A_{V2}^* = \frac{V_{out}}{V_{o1}} = -\frac{1}{2}G_m\left(\| \frac{R_d}{2} \| R_{2\_2} \| R_{ss2}\right)\left(\frac{R_2^*}{R_2^* + R_3}\right) \quad (15)$$

Considering the more concise transfer function analysis, the magnitude response for the overall system can be described by the combination of the responses for the first and second stages in (16).

$$|T(j\omega)| = \frac{|A_{V1}|}{1+|A_{V1}|\dfrac{R_5}{R_4 + R_5}} \cdot \frac{\omega}{\sqrt{\omega^2 + (\dfrac{1}{R_1C_1})^2}} \cdot |T_{LE}(j\omega)| \cdot \frac{|A_{V2}^*|\omega^2}{\sqrt{\left(\dfrac{1}{R_2R_3C_2C_3} - \omega^2\right)^2 + \left(\omega\left(\dfrac{1}{R_2C_2} + \dfrac{1}{R_3C_3} + \dfrac{(1-|A_{V2}^*|)}{R_2C_2}\right)\right)^2}} \quad (16)$$
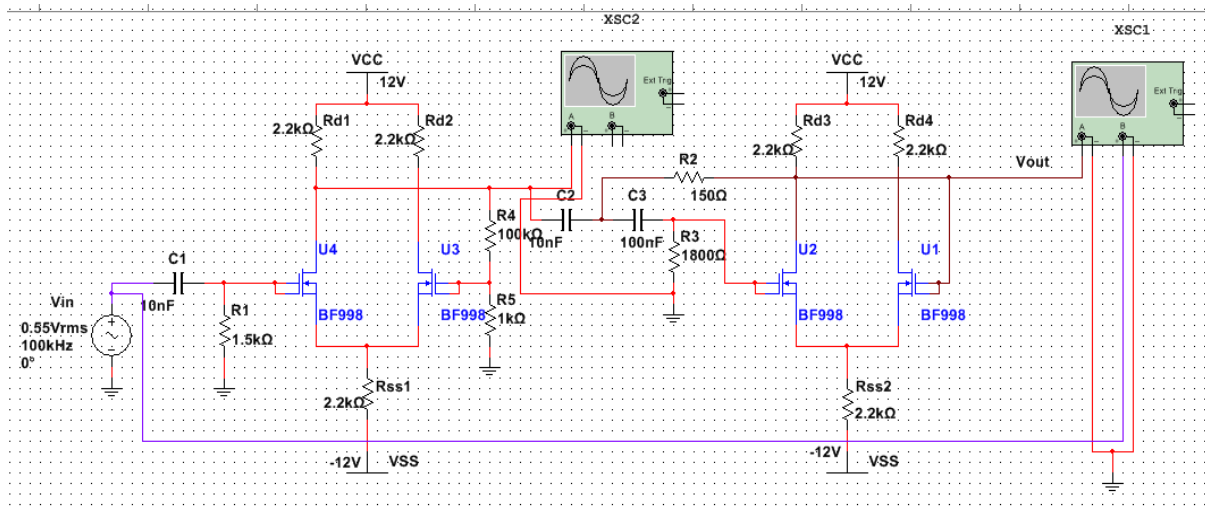

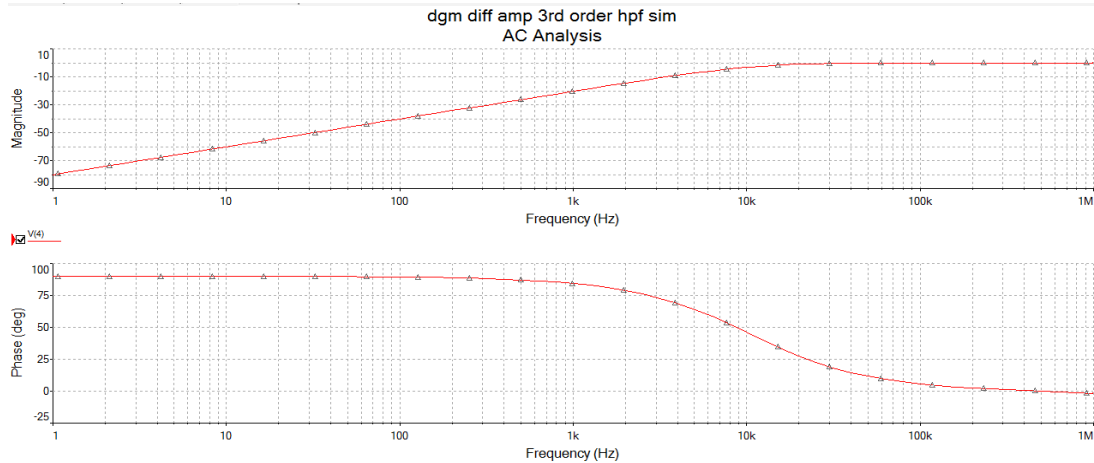Fig. 6. Simulation procedure of designed 3rd order high pass filter based on DG MOSFET.

Fig. 7. Frequency response of 3rd order HPF based on DG MOSFET.

IV. PARAMETRIC ANALYSIS OF DG MOSFET BASED 3RD ORDER HIGH PASS FILTER

For the parametric analysis of DG MOSFET based 3rd order high pass filter the designed circuit has been simulated as shown in Fig. 6. The DG MOSFET high frequency pole is approximately 34 MHz, hence it is suitable for RF switch operation and the corner frequency selected is 10 kHz. The following equations yield the resistance values for some assumed capacitor values, filter type and cutoff frequency:

$$R_1 = \frac{1}{2\pi f_c a_1 C_1}$$

$$R_2 = \frac{1}{\left(2\pi f_c\right)^2 b_2 C_2 C_3 R_3} \qquad (17)$$

$$R_3 = \frac{1}{2\pi f_c a_2}\left(\frac{1}{C_2} + \frac{1}{C_3}\right)$$

The filter model is designed to be a Butterworth filter, hence coefficient values are $a_1 = 1$, $b_1 = 0$, $a_2 = 1$, $b_2 = 1$ [49]. Setting the cutoff frequency and capacitor values to $f_c = 10$ kHZ, $C_2 = 10$ nF, and $C_3 = 100$ nF. Capacitor C_3 is set as higher than C_2 to allow for smoother output waveform and larger gain. Hence, the analysed resistances are $R_1 = 1.59$ kΩ, $R_2 = 144.69$ Ω, $R_3 = 1.75$ kΩ. The closest suitable and available values for $R_1 = 1.5$ kΩ, $R_2 = 150$ Ω, $R_3 = 1.8$ kΩ have been used in this research work. Simulations and analysis for the individual stages (1st order filter and 2nd order filter) have been conducted. The circuit for the full 3rd order HPF, constituting of cascading the 1st order HPF (1st stage) with the 2nd order HPF (2nd stage). The same input voltage of 0.3 V$_{rms}$ has been applied each time. Images detailed simulations have been presented in Fig. 7 and the results are summarized and displayed in Table I.

The frequency response (Fig. 7) of the circuit (Fig. 6) shows significant improvement as the low frequency attenuation (voltage drop in the stopband) has increased as well the rate of transition between the stopband and passband has sharpened which has been observed in the gains between 1 kHz and 10 kHz.

TABLE I: SIMULATION RESULTS FOR THIRD ORDER HIGH PASS FILTER BASED ON DG MOSFET

| Frequency (kHz)	Input voltage (V$_{pk-pk}$)	Output Voltage (V$_{pk-pk}$)	Voltage gain (V/V)	Voltage Gain calculated (V/V)
0.1	558 m	-259 μ	0.464 m	5.5941 μ
1	566 m	17.5 m	30.919 m	4.64 m
10	563 m	559 m	0.9929	420.52 m
30	562	874 m	1.5552	1.1530
100	556 m	0.956 m	1.7194	1.8966

The filter shows a large degree of attenuation in the stopband, inversely proportional to the frequency. The filter also shows almost ideal Butterworth characteristics, being entirely flat in the passband. The overall gain of the filter in the passband is just above unity. The corner frequency of approximately 10 kHz is achieved. The characteristics of the filter improved due to increased complexity concerning the higher order. The application of DG MOSFETs in the form of differential amplifiers is comparatively more suitable as compared to other active devices, therefore, provides the successful application for the filter design.

V. FABRICATION OF 3RD ORDER HIGH PASS FILTER WITH DG MOSFET

The implementation for the full system has been conducted on Printed Circuit Boards (PCB) as shown in Fig. 8 (a) which is further design and its front side with components naming is shown in Fig 8 (b) and its backside connections is in Fig. 8 (c). A differential amplifier PCB has been generated to allow for isolated testing of the differential amplifier and the individual stages of the system. The PCB has been designed in compliance with highlighted requirements with regards to drill sizes, track sizes, and the overall circuit size [50]-[56]. The track sizes implemented is 0.635 mm for the connections to both the SMD components and the IC sockets with it being 1.016 mm elsewhere. The pad and drill sizes used were 2.032 mm × 1.016 mm except for the SMD components, which have predetermined sizes. The single sided PCB has been selected, as the overall complexity is capable of being implemented as single sided PCB.
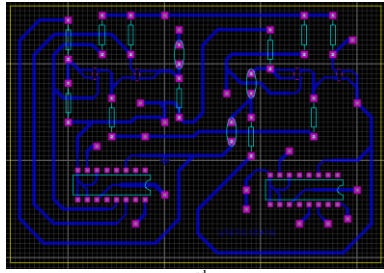
(a) PCB Design of 3rd order DGMOSFET HPF
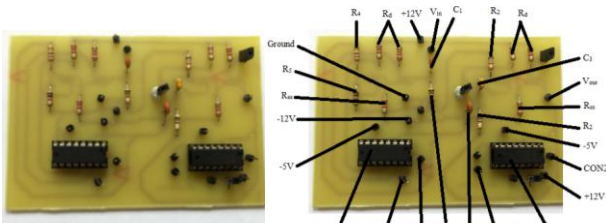
(b) Implementation of PCB for DG MOSFET based 3rd order HPF (front side)
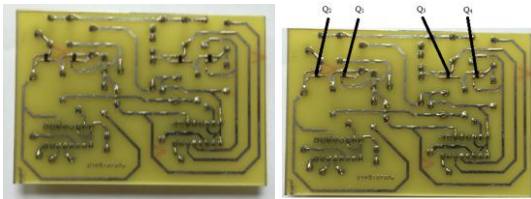
(c) Implementation of PCB for DG MOSFET based 3rd order HPF (back side)

Fig. 8. Fabrication procedure of the proposed 3rd order high pass filter based on DG MOSFET.

The Dual-In-line Package (DIP) type components, i.e. the capacitors, resistors and headers are soldered using normal methods. The multiplexer IC required an IC socket holder as the high temperatures from the soldering iron would burn the DIP chip. This is not the case for the SMD components, as they are designed to handle fairly high temperatures. There are various methods for soldering SMD components, with a popular method achieved via the use of the SMT reflow oven. The DC voltage rails are connected via headers on the PCB. An electronic trainer circuit board is used to provide the supply voltages, as the circuit needs both ±12 V (DG MOSFET DC rails), ±5 V (multiplexer DC rail and switch input) and ground, which the trainer provides all at

once.

The advanced soldering iron has been used as it has the capability of adjusting its temperature, allowing a range from 200 °C to 420 °C [57]. It also allows for changing the tip and a 0.3 mm tip is used. The thin tip is required for soldering SMD components. The multiplexer selected was chosen as it has a high DC voltage rails, low noise and relatively high bandwidth [58]. The PCB was connected to the power supplies and tested for various frequencies. This was performed for both the positive and negative sides (via the multiplexer).

VI. TESTING OF FABRICATED 3RD ORDER HIGH PASS FILTER WITH DG MOSFET

After the fabrication of the proposed device, the setup for the measurement and various parametric analyses has been shown in Fig. 9 (a). It has been used for the testing procedure. The results are recorded and are summarized in the Table II, alongside the calculated and simulated values. The gain for the negative side resembles an almost normalized value, being fairly lower than that on the positive side. This is due to the fact that the resistance and capacitor connections are made to the positive input side and hence the loading effects are not as relevant to the negative side gain. The results for the negative side are tabled in Table III.

TABLE II: RESULTS FOR IMPLEMENTATION OF 3RD ORDER DG MOSFET HPF FOR POSITIVE CONTROL SIGNAL

Frequency (Hz)	Input Voltage (mV$_{pp}$)	Output Voltage (V$_{pp}$)	Measured Gain (V/V)	Simulated Gain (V/V)	Calculated Gain (V/V)
102.306	566	9.2 m	16.254 m	0.464 m	1.2602 m
1.007k	560	18.4 m	32.857 m	30.919 m	59.9 m
10.0747k	560	472 m	842.86 m	0.9929	933.45 m
29.9565k	560	840	1.5000	1.5552	1.47383
100.821k	560	940	1.6786	1.7194	1.6542

TABLE III: RESULTS FOR IMPLEMENTATION OF 3RD ORDER DG MOSFET HPF FOR NEGATIVE CONTROL SIGNAL

Frequency(Hz)	Input Voltage (mV$_{pp}$)	Output Voltage (mV$_{pp}$)	Measured Gain (V/V)
100.208	568	14	24.468 m
1.0065k	560	23.6	42.143 m
9.9876k	560	356	635.71 m
30.1458k	568	648	1.2408
99.994k	568	736	1.2958

(a) Full setup for testing of proposed device

(b) Input voltage maximum

(c) passband gain

(d) Cut-off frequency

(e) bandwidth

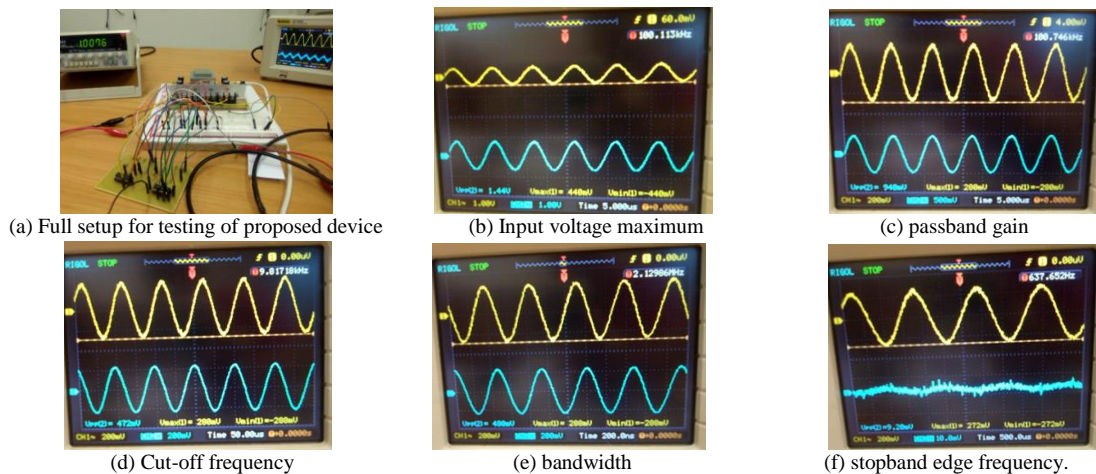(f) stopband edge frequency.

Fig. 9. Measurement setup and its analysis for the fabricated device.

A. Input Voltage Range

The DC voltage rails for the amplifier are finite and set values, which determine the maximum and minimum values for the output voltage. For single sided outputs this is further decreased and shifted. The input voltage for the third order high pass filter is varying at 100 kHz frequency and checking where the gain is attenuated. The results are shown in Fig. 9 (b). The minimum input voltage generated by the function generator is $V_{in(pp)} = 120$ mV$_{p-p}$. The upper limit for the input voltage is obtained to be $V_{in(p-p)} = 880$ mV$_{pp}$ (gain of 1.6364). The input voltage range is a necessary characteristic as it denotes the limitations on the input signal when maximum gain is expected.

B. Passband Gain Analysis

The passband gain measured at 100 kHz is shown in Fig. 9 (c). The passband gain is obtained to be $A_{v(max)} = 2.2495$ dB. The passband gain is an important characteristic as it directly correlates to the performance of the filter that is the degree to which the filter allows certain signal components to pass through. It is also required in modeling of the stopband and transition band characteristics.

C. Cut-off Frequency Measurment

The cut-off frequency (-3 dB frequency) is the amplitude for a normalized frequency response. The cut-off frequency is the fundamental characteristics for all filters, as it corresponds to the threshold point at which the filter functionality occurs. The cutoff frequency for the circuit is found at -3dB $+ A_{v(max)} = -750.5$ mdB. This is shown in Fig. 9 (d). The gain at this frequency is -788.74 mdB. The cut-off frequency found is approximately 9.8 kHz, compared to the designed value of 10 kHz. The minor difference is due to the tolerance in capacitances and resistances values.

D. Bandwidth Analysis

The bandwidth of the system is obtained by keeping the input voltage constant and varying the frequency. It is expected for the bandwidth to be less than predicted due to the use of multiplexers. The testing results are displayed in Fig. 9 (e). The point where the magnitude is approximately 3 dB below the passband gain (-0.067 dB gain in this instance) is at 2.02 MHz, which is the bandwidth for this designed device. The bandwidth is very closely linked to the possible applications of the HPF, as different technologies offer different bandwidths. Hence by analyzing the bandwidth required and possibly other characteristics, a suitable technology can be determined. The bandwidth of 0 to 2 MHz is suitable for aviation and AM radio applications.

E. Transition Band

The minimum stopband attenuation is approximately -20 dB. This corresponds to one hundredth of the passband gain (approximately 16.786 mV/V). The attenuation in the transition band is exponentially decreasing. This is visible in the decibel range, but

elsewhere it appears flat as they approach zero (all gain values are very small hence the difference between values is also small). The transition band is obtained by lowering the frequency until a sufficient value is found. The stopband is resulted to end at 657.652 Hz, hence transition bandwidth is approximately 9.42 kHz. The transition bandwidth is an important characteristic as it allows for modelling of possible errors in application of the system. Lower the transition band corresponds to greater performance of the system.

Table IV depicts a comparison of the results obtained via the implementation and those obtained via simulation as well as implementation of other technologies for the design of a 3rd order high pass filter with various technologies.

TABLE IV: COMPARISON OF VARIOUS TECHNOLOGIES FOR THE FILTERS

Term	[49]	[18]	This work (simulated)	This work (achieved)
Technology used	CMOS	CSDG MOSFET	DGMOSFET	DGMOSFET
Type	Bessel	Butterworth	Butterworth	Butterworth
Order	3	3	3	3
Cut-off Frequency	1 kHz	0.3 THz	~9.69 kHz	~9.8172 kHz
Bandwidth	1 THz	~50MHz	13 MHz	2.01986 MHz
Passband Voltage Gain	0 dB	-33.499 dB	2.35 dB	2.2495 dB
Circuit Area Size	52 x 47 mm²		65 x 97 mm²	65 x 97 mm²
Power Supplies	+- 5V		+-12V (+-5V for switch) (+12V and -5V for MUX	+-12V (+-5V for switch) (+12V and -5V for MUX
Additional functionality		Very high frequency operation	Multiplexers applied allowing generation of two filters	Multiplexers applied allowing generation of two filters

VII. CONCLUSIONS AND FUTURE RECOMMENDATIONS

The systemic design steps were followed resolutely, from theoretical analysis, circuit design, mathematical analysis, circuit simulations, finally to fabrication and testing. The results of the simulations are completely matching the theoretically achieved results, provide basis for a successful implementation of the design. This implementation satisfies the necessary requirements while correlating with results obtained via the simulations and calculations. The final analysis of the system concluded that the bandwidth is approximately 2 MHz (theoretically predicted that the bandwidth of DG MOSFETs is 38 MHz). Therefore, the filter design using DG MOSFET technology is viable providing the bandwidth required correlates to the expected one.

Possible applying analogue switches and corresponding logic circuit instead of the multiplexer IC may improve the bandwidth generated, but could also increase the complexity and size of the designed circuit. The gain generated is higher than comparative circuits, and can be improved further via increased the resistance R_4 in the design. In future this work can be extended using the CSDG MOSFET.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Sashin Ramdhani (SR) and Viranjay M. Srivastava (VMS) conducted this research; SR designed and fabricated the circuit after that analyzed the data and wrote the paper; VMS has verified the result with the designed circuit; all authors had approved the final version.

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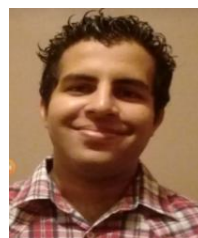
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