High CMRR Voltage Mode Instrumentation Amplifier Using a New CMOS Differential Difference Current Conveyor Realization

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***Abstract*—This paper describes a new CMOS realization of differential difference current conveyor circuit (DDCC). The proposed design offers enhanced characteristics compared to DDCC circuits previously exhibited in the literature. It is characterized by a wide dynamic range with good accuracy through the use of adaptive biasing circuit instead of a constant bias current source as well as a wide bandwidth (560 MHz) and a low parasitic resistance at terminal X about 6.86 Ω. A voltage mode instrumentation amplifier circuit (VMIA) composed of a DDCC circuit and two active grounded resistances is shown as application. The proposed VMIA circuit is intended for high frequency applications. This configuration offers significant improvement in accuracy as compared to the state of the art. It is characterized by a controllable gain, a large dynamic range with Total Harmonic Distortion (THD) less than 0.27 %, a low noise density (22 nV/Hz$^{1/2}$) with a power consumption about 0.492 mW and a wide bandwidth nearly 83 MHz. All proposed circuits are simulated by TSPICE using CMOS 0.18 µm TSMC technology with ± 0.8 V supply voltage to verify the theoretical results.**

***Index Terms*—Differential Difference Current Conveyor (DDCC), Adaptive biasing circuit, Instrumentation Amplifier (IA), Voltage mode, Common-Mode Rejection Ratio (CMRR).**

I. Introduction

An instrumentation amplifier is an important electronic device widely applied to amplify the small differential signals in the presence of large common-mode interference. This integrated circuit presents a kind of differential amplifier family which can be found in medical instrumentation [1]-[5], readout circuits of biosensor [6], [7], data acquisition and signal processing [8].

The first proposed instrumentation amplifier circuit is built of three operational amplifier integrated circuits and seven resistances. This circuit is characterized by major cons which are the limitations of the bandwidth and the common-mode rejection ratio (CMRR). To solve these problems, novel instrumentation amplifier topologies were introduced in the literature. In 2010, Erkan Yuce has proposed four instrumentation amplifier (IA) topologies, one of which is current-mode (CM) while the others are voltage-mode (VM), using current feedback operational amplifiers (CFOAs) [9]. In 2013, a new design of a chopper current mode instrumentation amplifier composed by two second generation current conveyor circuits was presented. This circuit aims to be the reading circuit of a high precision temperature sensor [10]. In 2016, a new design of a current mode instrumentation amplifier (CMIA) based on the flipped voltage follower (FVF) was proposed [11].

In this paper, a high performance differential difference current conveyor circuit (DDCC) operated at ± 0.8 V is presented. Through the use of a modified flipped voltage follower cell as an adaptive biasing circuit and compensation impedances in form of a resistance in series with a capacitor, this circuit is characterized by a voltage dynamic range about ± 0.62 V with THD less than 0.25 %, a low parasitic impedance at terminal X (6.86 Ω) and wide bandwidth about 558 MHz. Also, the current mode responses of DDCC circuit show a ± 0.35 mA dynamic range and a bandwidth about 560 MHz. The power consumption is about 0.472 mW.

As an application, a controlled voltage mode instrumentation amplifier circuit using a DDCC circuit and two grounded active resistances is proposed. This circuit is intended for high frequency applications. It is characterized by controlled gain, wide bandwidth about 83 MHz, a high CMRR (146 dB) and power consumption about 0.492 mW.

II. Adaptive Biasing

The adaptive biasing circuit presents a typical solution very used in the modern applications to solve the problem of the large bias current [12], [13]. This circuit is characterized by a high input impedance, a low output resistance, high precision currents and the possibility to operate with a lower voltage supply.

The schematic diagram of differential pair polarized by adaptive biasing circuit [14], [15] is presented in Fig. 1. This technique allows to couple the differential pair by two DC voltage level shifters.

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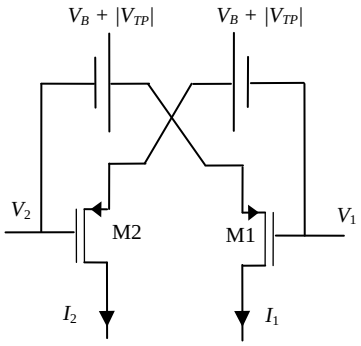

Fig. 1. Schematic diagram of differential pair biased by adaptive biasing circuit.

The current drain expression of differential pair operating in saturation mode is given by :

$$I = \frac{\beta}{2}\left(V_{SG} - |V_{TP}|\right)^2 \quad (1)$$

where $\beta = \mu_p C_{ox}(W/L)$, V_{SG} is the source gate voltage of transistor, V_{TP} is threshold voltage, W is gate width, L is gate length, C_{ox} is the gate oxide capacitance per unit area, μ_n is charge carrier effective mobility.

Assuming that the transistors M1 and M2 are identical, the differential output current (I_d) is defined as :

$$I_d = I_1 - I_2 = \frac{\beta}{2}\left(V_{SG1} + V_{SG2} - 2|V_{TP}|\right)\left(V_{SG1} - V_{SG2}\right) \quad (2)$$

In order to obtain a linear differential current (I_d), the term $V_{SG1}+V_{SG2}-2|V_{TP}|$ must have a constant value. As solution, two floating DC voltage sources with values $V_B-|V_{TP}|$ have been integrated, as shown in Fig. 1.

The sum and difference relationships between V_{SG1} and V_{SG2} are given by :

$$V_{SG1} + V_{SG2} = 2\left(V_B + |V_{TP}|\right) \quad (3)$$

$$V_{SG1} - V_{SG2} = 2\left(V_1 - V_2\right) \quad (4)$$

The differential output current expression has become

$$I_d = 2\beta V_B\left(V_1 - V_2\right) = g_m\left(V_1 - V_2\right) \quad (5)$$

where g_m is the trans-conductance.

The linear input signal range and the linear output signal range are delimited respectively by

$$\left|V_1 - V_2\right| < V_B \quad (6)$$

$$I_d < 2\beta V_B^2 \quad (7)$$

Fig. 2 shows different CMOS source follower topologies. The common drain amplifier is presented in Fig. 2 (a). It presents the simplest design of a high linearity unity buffer [16]. This circuit can be operated with a minimum supply voltage:

$$V_{DD,\min} - V_{ss,\min} = V_{SD1,sat} + V_{SD2,sat} \quad (8)$$

Also, this circuit can be used as a voltage follower where the output voltage follows the input voltage with a DC level shift (V_{SG1}):

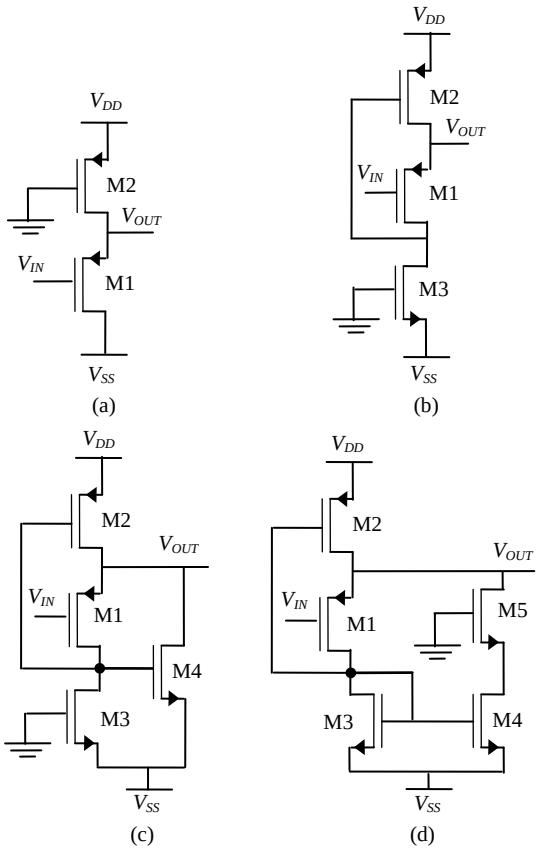

Fig. 2. Voltage buffer: (a) common-drain, (b) flipped voltage follower (c) folded flipped voltage follower, and (d) modified folded flipped voltage follower.

$$V_{OUT} = V_{IN} + V_{SG1} \quad (9)$$

Regarding behavior of large-signal, this circuit is capable to sink a large current from the load, but its sourcing capability is limited by the current drain of transistor M2. The major disadvantage of this circuit is that the current through the transistor M1 depends on the output current. Consequently, the voltage gain is less than unity.

The voltage gain and the output resistance expressions are given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{r_{o1} r_{o2} g_m}{r_{o1} + r_{o2} + r_{o1} r_{o2} g_m} \quad (10)$$

$$R_{OUT} = \frac{r_{o1} r_{o2}}{r_{o1} + r_{o2}} \quad (11)$$

The circuit shown in Fig. 2 (b) presents a modified voltage follower circuit named flipped voltage follower (FVF) [17], [18]. The drain current transistor M1 is kept constant, regardless of the output current, through to the use of transistor M3 as a source of bias current. Considering that the short-channel effect $V_{SG,M1}$ held constant, the voltage gain is unity. Contrary to the classic voltage follower, this circuit is able to source a large amount of current. But, its damping capability is limited by the current through the transistor M1. The large sourcing capability is due to the low impedance at the output node.

The voltage gain and the output resistance expressions are given by :

$$\frac{V_{OUT}}{V_{IN}} = \frac{r_{o1}r_{o2}r_{o3}g_{m1}g_{m2}}{r_{o2}+r_{o2}r_{o3}g_{m2}+r_{o1}r_{o2}g_{m1}+r_{o1}r_{o2}r_{o3}g_{m1}g_{m2}} \quad (12)$$

$$R_{OUT} = \frac{r_{o1}r_{o2}+r_{o2}r_{o3}}{r_{o1}+r_{o2}+r_{o3}+r_{o1}r_{o2}r_{o3}g_{m1}g_{m2}} \quad (13)$$

The minimum supply voltage used to power FVF circuit is expressed by :

$$V_{DD,\min} - V_{SS,\min} = V_{SD_{M3},sat} + V_{SD_{M2},sat} + |V_{TP2}| \quad (14)$$

The linear operation region of FVF circuit is still valid for transistors M1 and/or M2 operated in saturation region. The valid region of limited common mode input voltage range is expressed by :

$$V_{SS} + V_{DS_{M3},sat} - |V_{TP1}| < V_{CM} < V_{DD} - V_{SD_{M2},sat} - V_{SD_{M1},sat} - |V_{TP1}| \quad (15)$$

The folded flipped voltage follower (FFVF) presented in Fig. 2 (c) is introduced as a solution for the limited current delivering capability of FVF [19]. The transistor M4 provides additional current whenever it is required by load. Therefore, this circuit is capable to sink and provide large current. The voltage gain and the output resistance expressions are given by :

$$\frac{V_{OUT}}{V_{IN}} = \frac{r_{\Pi}g_{m1}(g_{m2}+g_{m4})}{(r_{o1}+r_{o3})(r_{o4}+r_{o2})+r_{\Pi}g_{m1}(g_{m2}+g_{m4})} \quad (16)$$

$$R_{OUT} = \frac{r_{o2}r_{o4}(r_{o1}+r_{o3})}{(r_{o1}+r_{o3})(r_{o4}+r_{o2})+r_{\Pi}g_{m1}(g_{m2}+g_{m4})} \quad (17)$$

where $r_{\Pi}=r_{o1}r_{o2}r_{o3}r_{o4}$.

The minimum supply voltage used to power FFVF circuit is expressed by:

$$V_{DD,\min} - V_{SS,\min} = V_{SD_{M2},\text{sat}} + V_{DS_{M4},\text{sat}} + |V_{TP2}| + |V_{TP4}| \quad (18)$$

The valid region of limited common mode input voltage range is expressed by

$$V_{SS} + V_{DS_{M4},sat} + |V_{TP4}| - |V_{TP1}| < V_{CM} < V_{DD} - V_{SD_{M2},sat} - V_{SD_{M1},sat} - |V_{TP1}| \quad (19)$$

The modified folded flipped voltage follower (FFVF) is presented in Fig. 2 (d). The transistor M5 has been integrated in order to minimize the output impedance.

The voltage gain and the output resistance expressions are given by (20) and (21).

The characteristics for all voltage follower circuits have been estimated by TSPICE using 0.18 µm CMOS TSMC with ±0.8 V supply voltage. The output voltage variations according to the input voltage variations show the same linear behavior over an input voltage range from –0.8 V to 0.45 V, as presented in Fig. 3.

From Fig. 4, it can be noticed that, the output impedance of modified folded flipped voltage follower at low frequency is less than those of flipped FVF, conventional FVF and common drain amplifier. The output impedances present resistive behaviors equal respectively to 170 Ω, 461.2 Ω, 873.9 Ω and 4.52 kΩ up to 0.6 GHz.

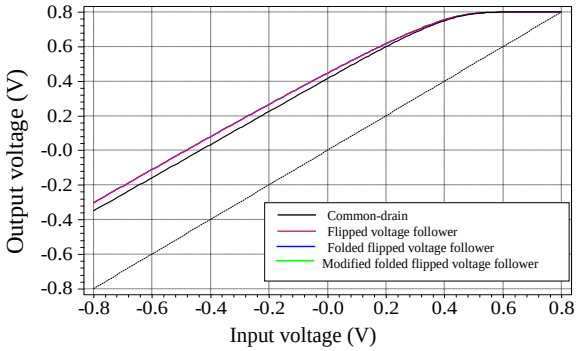

Fig. 3. DC voltage transfer characteristics.

$$\frac{V_{OUT}}{V_{IN}} = \frac{r_{o2}r_{o4}r_{o5}g_{m1}g_{m3}g_{m4}g_{m5}+r_{02}r_{o4}r_{o5}g_{m1}g_{m3}g_{m5}(g_{m3}+g_{m2})}{r_{o2}g_{m3}(g_{m3}+r_{o4}r_{o5}g_{m1}g_{m4}g_{m5})+r_{o5}r_{o4}g_{m3}g_{m5}(g_{m3}+g_{m1}r_{02}(g_{m3}+g_{m2}))} \quad (20)$$

$$R_{OUT} = \frac{r_{o1}r_{o4}r_{o5}g_{m5}g_{m3}^2}{r_{o4}r_{o5}g_{m5}(r_{o1}g_{m1}g_{m3}+g_{m2})(g_{m3}+g_{m4})+r_{o1}g_{m3}(g_{m3}+r_{o4}r_{o5}g_{m2}g_{m4}g_{m5})} \quad (21)$$

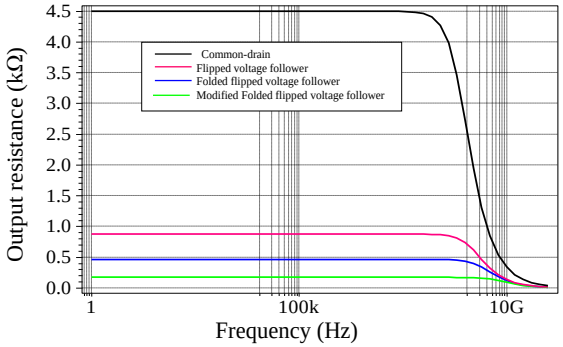

Fig. 4. Variation of output impedances according to frequency.

III. Differential Difference Current Conveyor Circuit DDCC

A. Circuit Description

The differential difference current conveyor circuit was introduced as new active building block in 1996 by W. Chiu *et al.* [20]. This circuit has three voltage input terminals (Y1, Y2, Y3) with high impedances, a current input terminal (X) with a low impedance and a current output terminal (Z) with a high impedance. The relationships between voltage and current terminals can be expressed in the real case by (22).

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 \\ 0 & 0 & 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \end{bmatrix} \quad (22)$$

where β_j=1−ε_{vj} for (j=1, 2, 3) and α=1−ε_i, whereas ε_{vj} and ε_i ($|\varepsilon_{vj}|$<<1 and $|\varepsilon_i|$<<1) represent voltage and current tracking errors of circuit, respectively. There are two types of DDCC depending on the sign of α, namely positive-type (DDCC+) or negative-type (DDCC−).

The overall CMOS circuit of the proposed DDCC is shown in Fig. 5. The input stage is composed by two PMOS differential pairs (M1, M2) and (M3, M4) biased by two adaptive biasing circuits, composed by CMOS source follower shown in Fig. 3 (d), and three current mirrors (M5, M6), (M7, M8) as well as (M9, M10) such as the drains of M6 and M8 are connected respectively to M9 and M10.

The offset voltage expression among the input voltages (V_{Y1}, V_{Y2}, V_{Y3}) and the output voltage (V_X) is given by

$$\Delta V = V_X - (V_{Y1} - V_{Y2} + V_{Y3}) \approx \sqrt{2}\lambda_p \left[V_{D1}\left(\sqrt{\frac{I_{D1}}{\beta_1}} - \sqrt{\frac{I_{D3}}{\beta_3}} \right) - V_{D2}\left(\sqrt{\frac{I_{D2}}{\beta_2}} - \sqrt{\frac{I_{D4}}{\beta_4}} \right) \right] \quad (23)$$

where λp is the channel length modulation parameter. (V_{D1}, V_{D2}, V_{D3}, V_{D4}) and (I_{D1}, I_{D2}, I_{D3}, I_{D4}) are the drain voltages and the drain currents of transistors M1, M2, M3 and M4.

It is clear that the offset voltage is null because the two pair differentials M1-M2 and M3-M4 have the same characteristics and the sum of drain currents I_1+I_3 and I_2+I_4 are equal since the drain terminals of transistors M6 and M8 are connected respectively to the drain terminals of transistors M9 and M10.

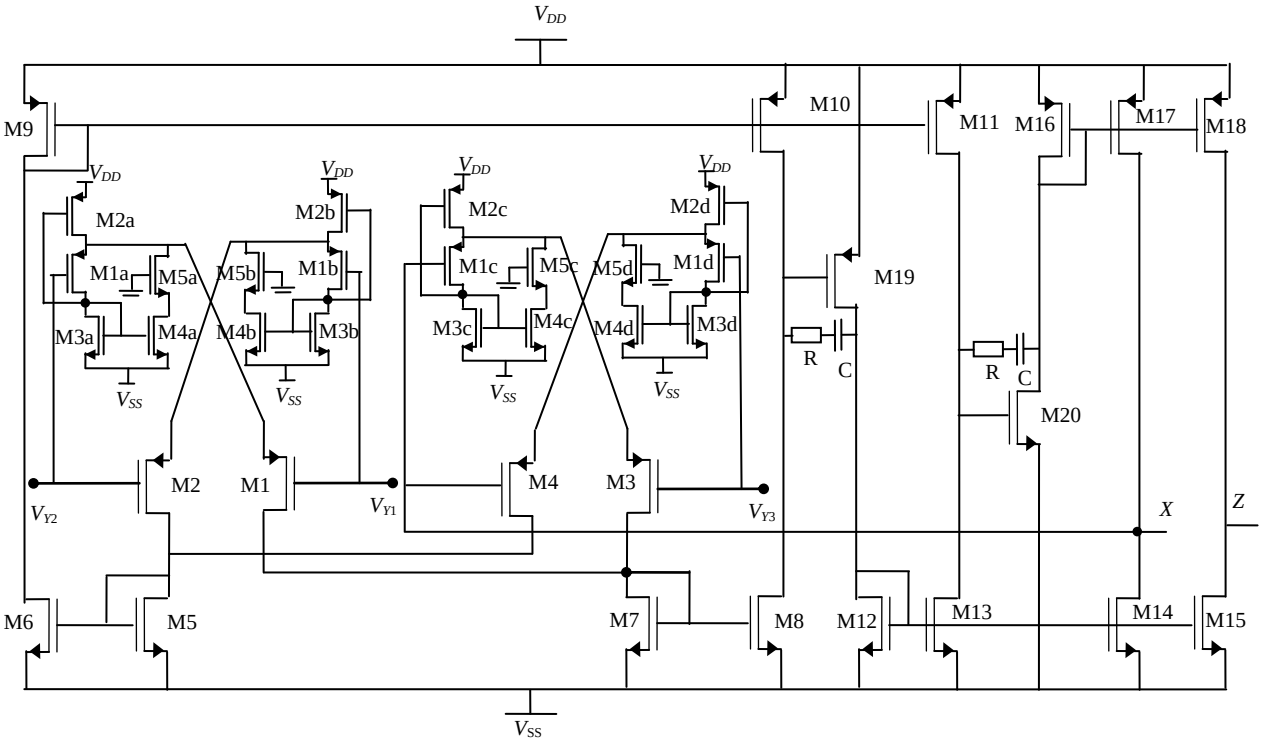

Fig. 5. Proposed differential difference current conveyor circuit (DDCC).

The output stage composed of transistors M11 to M20 is constituted by two current mirrors and two offset adjustments. The current mirror M12-M15 has the same current drain than the two current mirrors M5-M6 and M7-M8 since the drain terminal of transistor M11 is connected to the drain terminal of transistor M13. Moreover, the connection of two drain terminals of transistors M14 and M15 respectively to the drain terminals of transistors M17 and M18 check the second property of the DDCC circuit.

$$I_X = I_Z \quad (24)$$

According to the small-signal equivalent circuit analysis, the expressions of β_j are given as following, while taking into account that the transistors of NMOS and PMOS current mirrors are characterized by same trans-conductance (g_{mN}, g_{mP}) and same resistor seen at the drain of transistor (r_N, r_P):

$$\beta_1 = \frac{V_X}{V_{Y1}} = \frac{r_N^3 r_P^3 g_{mP} g_{mN} (g_{m2} + g_{m1})}{(r_P + r_N)^3 + r_N^3 r_P^3 g_{mP} g_{mN} (g_{m2} + g_{m1})} \approx 1 \quad (25)$$

$$\beta_2 = \frac{V_X}{V_{Y2}} = -\frac{r_N^3 r_P^3 g_{mP} g_{mN} (g_{m4} + g_{m3})}{(r_P + r_N)^3 + r_N^3 r_P^3 g_{mP} g_{mN} (g_{m4} + g_{m3})} \approx -1 \quad (26)$$

$$\beta_3 = \frac{V_X}{V_{Y3}} = \frac{r_N^3 r_P^3 g_{mP} g_{mN} \left(g_{m4} + g_{m3}\right)}{\left(r_P + r_N\right)^3 + r_N^3 r_P^3 g_{mP} g_{mN} \left(g_{m4} + g_{m3}\right)} \approx 1 \quad (27)$$

The current transfer ratio α is equal to

$$\alpha \approx 1 \quad (28)$$

The parasitic resistance of the X terminal is given by

$$R_X = \frac{V_X}{I_X} = \frac{r_N r_P \left(r_N + r_P\right)^2}{\left(r_N + r_P\right)^3 + r_N^3 r_P^3 g_{mN} \left(g_{mP} g_{m4} + g_{mN} g_{m3}\right)} \quad (39)$$

In order to stabilize the bandwidth of proposed DDCC circuit, compensation impedances in form of a resistance R in series with a capacitor C have been integrated as presented in Fig. 5. By considering the compensation impedances, the voltage transfer expression of proposed DDCC circuit is characterized by seven poles (ω_{p1}, ω_{p2}, ω_{p3}, ω_{p4}, ω_{p5}, ω_{p6}, ω_{p7}) and seven zeros (ω_{z1}, ω_{z2}, ω_{z3}, ω_{z4}, ω_{p5}, ω_{z6}, ω_{z7}), as given by

$$A_V = \frac{V_X}{V_{Y1} - V_{Y2} + V_{Y3}} = A_0 \frac{\prod_{i=z1}^{z7} \left(1 + \frac{s}{\omega_i}\right)}{\prod_{i=p1}^{p7} \left(1 + \frac{s}{\omega_j}\right)} \quad (30)$$

By substituting $s=j\omega$ and at $\omega=\omega_H$, the squared magnitude of transfer function is given by

$$\left|A_V\left(j\omega_H\right)\right|^2 = \frac{\prod_{i=z1}^{z7} \left(1 + \frac{\omega_H^2}{\omega_i^2}\right)}{\prod_{j=p1}^{p7} \left(1 + \frac{\omega_H^2}{\omega_j^2}\right)} = \frac{1}{2} \quad (31)$$

The expression of ω_H can be given by [21], [22]:

$$\omega_H \cong \frac{1}{\sqrt{\left(\sum_{i=p1}^{p7} \frac{1}{\omega_i^2}\right) - 2\left(\sum_{j=z1}^{z7} \frac{1}{\omega_j^2}\right)}} \quad (32)$$

By considering these approximations ($\omega_{p1}<<\omega_{p2}<<\cdots<<\omega_{p7}$ and $\omega_{z1}<<\omega_{z2}<<\cdots<<\omega_{z7}$), the cut-off frequency of proposed differential difference current conveyor DDCC is roughly equal to the cut-off frequency of the first pole.

$$f_H = f_{p1} = \frac{2 r_N^3 r_P^3 g_{mN}^3}{2\pi \begin{pmatrix} \left(5Rr_P + 5Rr_N + 3r_N r_P\right)\left(r_N + r_P\right)^2 \\ +14 r_N^3 r_P^3 g_{mN}^3 R \end{pmatrix} C} \quad (33)$$

TABLE I. TRANSISTOR ASPECT RATIOS OF PROPOSED DDCC CIRCUIT

Transistor	W (μm)/L(μm)
M1, M2, M3, M4	5/0.18
M5, M6, M7, M8, M12, M13, M14, M15, M20	3/0.18
M9, M10, M11, M16, M17, M18, M19	10/0.18
M1a, M1b, M1c, M1d	2/0.18
M2a, M2b, M2c, M2d	40/0.18
M3a, M3b, M3c, M3d, M4a, M4b, M4c, M4d	0.27/0.3
M5a, M5b, M5c, M5d	0.4/0.18

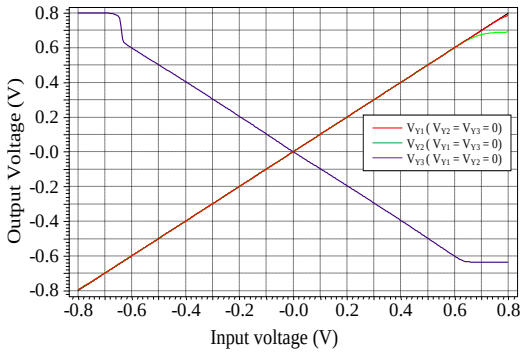

Fig. 6. DC transfer characteristic for voltage transfer.

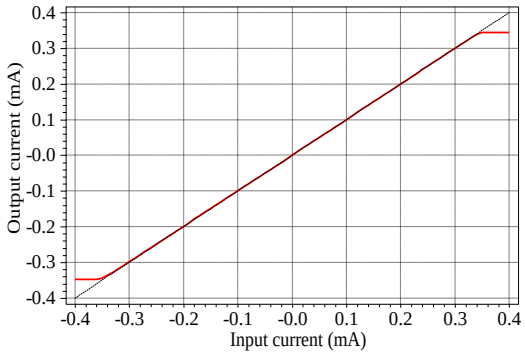

Fig. 7. DC transfer characteristic for current transfer.

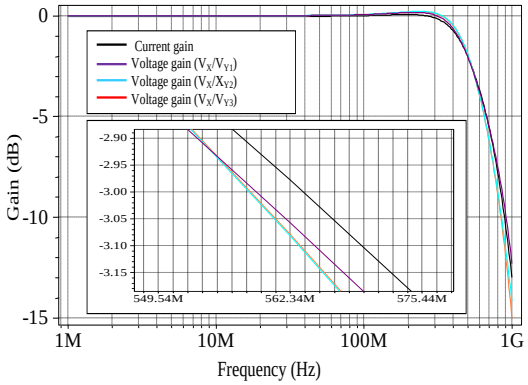

Fig. 8. Frequency responses of current and voltage gains.

B. Simulation Results

The performance of the proposed DDCC circuit is verified by performing TSPICE simulations with supply voltages ±0.8 V using 0.18 μm TSMC CMOS technology. The transistor aspect ratios are given in Table I.

The DC voltage characteristics between Y-terminals and X-terminal are presented in Fig. 6. The output voltages obtained to X-terminal according to $V_{Y1}-V_{Y2}+V_{Y3}$ show a common dynamic range extended from –0.62 V to 0.62 V with offset voltage less than 12 μV. The variation of output current I_Z versus the current I_X is shown in Fig. 7. With grounded Y terminals and a load resistance of about 1 kΩ, the current follower characteristic presents a maximum offset current of 12.2 nA with the boundary linear range from –350 μA to 350 μA.

The frequency response of voltage gains (V_X/V_{Y1}, V_X/V_{Y2}, V_X/V_{Y3}) and current gain (I_Z/I_X) are plotted in Fig. 8. The cutoff frequencies of the voltage gains obtained without load are about 558 MHz and unity gains at low

frequencies. The frequency response of current gain shows a unit gain and a cutoff frequency about 563 MHz with load resistance about 1 kΩ. The frequency characteristics of parasitic impedance at X terminal are presented in Fig 9. This circuit shows a resistive behaviors about 6.86 Ω up to 10 MHz. The power consumption of DDCC circuit is about 472 µW.

Fig. 10 shows the variations of total harmonic distortion (THD) of output voltage V_X for different peak

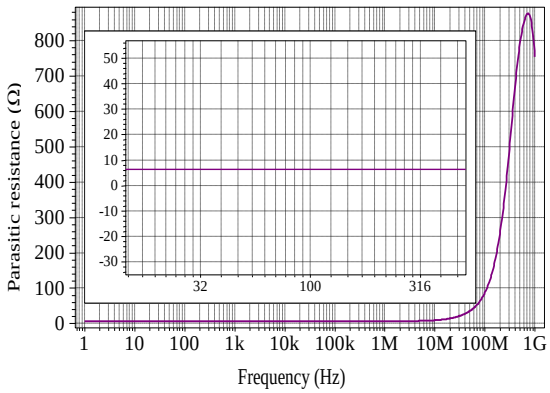

Fig. 9. Frequency response of parasitic impedance Z_X.

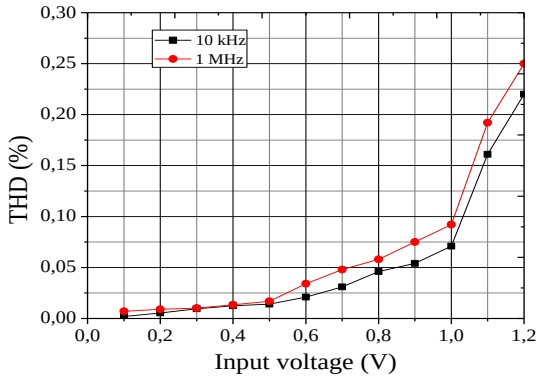

Fig. 10. THD of voltage follower with 10 kHz and 1 MHz.

to peak differential input voltage amplitudes with 10 kHz and 1 MHz frequency.

Table II shows an impartial comparison between the proposed DDCC circuit and other proposed in the literature. It is obvious that our circuit is characterized by a large dynamic range, good accuracy as well as low parasitic resistance at X-terminal.

IV. Controlled Voltage Mode Instrumentation Amplifier (VMIA)

A. Circuit Description

The schematic diagram for the proposed voltage mode instrumentation amplifier circuit is presented in Fig 11. It is composed of one differential difference current conveyor circuit (DDCC) and two grounded resistances.

Considering the ideal case for DDCC circuit, the routine analysis yields the following transfer function:

$$V_{OUT} = A_0 \left(V_{IN1} - V_{IN2} \right) \tag{34}$$

where the gain A_0 is equal to the ratio R_2/R_1.

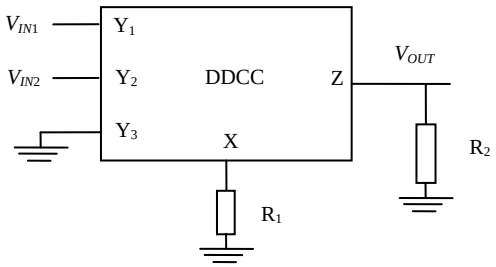

Fig. 11. Voltage mode instrumentation amplifier circuit (VMIA).

Taking into account the non-ideal gains of DDCC circuit, (34) becomes:

$$V_{OUT} = \alpha A_0 \left(\beta_1 V_{IN1} - \beta_2 V_{IN2} \right) \tag{35}$$

Table II. Performance Parameters Comparison of Proposed DDCC Circuit with Other Reported in the Literature

Parameters	Units	Differential difference current conveyor DDCC						
		[23] 2012	[24] 2013	[25] 2010	[26] 2010	[27] 2016	[28] 2011	Proposed circuit
Technology CMOS	µm	0.18	0.18	0.25	0.25	0.25	0.25	0.18
Supply voltage	V	±0.9	±0.3	±1.5	±1.5	±1.25	±1.25	±0.8
DC voltage range	V	---	±0.15	±0.9	---	---	±0.3	±0.62
Voltage offset	mV	---	<0.093	1.36	---	---	---	0.012
Bandwidth of voltage transfer gain VX/VY1, VX/VY2, VX/VY3	MHz	588.84 --- ---	27 --- ---	120 --- ---	80 --- ---	291 312 ---	100 --- ---	559.12 558.54 558.30
Voltage gain	----	0.99	1	1	---	---	1	1
DC current range	mA	---	±0.008	±1	---	---	±0.1	±0.35
Current offset	nA	---	<3	------	---	---		6.02
Bandwidth of current transfer gain	MHz	605.86	27	85	80	513	100	562.85
Current gain	----	0.99	1	1	---	---	1	1
Node X parasitic impedance: RX/LX	Ω/µH	150.2/4.16	1600/270	9/---	600/--	3/1.8	1-12k (0.1-100 µA)	6.36/237.9
Node Z parasitic impedance: RZ/CZ	MΩ/pF	5.03/24	10.38/0.13	-----	0.014/--	0.25 10-3, 50	---	6.23/31.5
Node Y1, Y2, Y3 parasitic impedances: RY/CY	GΩ/fF	29.08 103/3.86 --- ---	130/5 119/5 119/5	--- --- ---	--- --- ---	∞/15.5 ∞/21.5 ---	--- --- ---	∞/12.4 ∞/12.51 ∞/12.68
Power consumption	µW	462	18.6	1740	2000	930	1350	472

From this expression, the differential-mode gain (ADM) and the common-mode gain (ACM) are respectively given by

$$A_{DM} = \frac{\alpha}{2} A_0 \left(\beta_1 + \beta_2\right) \quad (36)$$

$$A_{CM} = \alpha A_0 \left(\beta_1 - \beta_2\right) \quad (37)$$

The common-mode rejection ratio CMRR is computed as follows:

$$CMRR = \left|\frac{A_{DM}}{A_{CM}}\right| = \frac{1}{2}\left|\frac{\beta_1 + \beta_2}{\beta_1 - \beta_2}\right| \quad (38)$$

It is clear from this expression that the CMRR is independent of gain, which is a desired situation. The active and passive element sensitivities are evaluated as

$$S_{V_{OUT}}^{A_0} = 1,\ S_{V_{OUT}}^{V_{IN1}} = \frac{V_{IN1}}{V_{IN1} - V_{IN2}},\ S_{V_{OUT}}^{V_{IN2}} = \frac{V_{IN2}}{V_{IN2} - V_{IN1}}$$

$$S_{V_{OUT}}^{\alpha} = 1,\ S_{V_{OUT}}^{\beta_1} = \frac{\beta_1 V_{IN1}}{\beta_1 V_{IN1} - \beta_2 V_{IN2}},$$

$$S_{V_{OUT}}^{V_{IN2}} = \frac{\beta_2 V_{IN2}}{\beta_2 V_{IN2} - \beta_1 V_{IN1}}$$

The presences of parasitic impedances include effects not only on the gain but also on the value of the bandwidth. The proposed VMIA circuit considering the present of parasitic elements is shown in Fig. 12.

If only parasitic impedances of DDCC are considered into account, the expression (34) is become

$$V_{OUT} = \frac{R_Z \,//\, R_2}{R_1 + R_X} \frac{1}{1 + sC_Z\left(R_Z \,//\, R_2\right)} \left(V_{IN1} - V_{IN2}\right) \quad (39)$$

where the gain A_V of instrumentation amplifier as well as the bandwidth ω_c, where it equal to infinity in the ideal case, are given respectively by

$$A_V = \frac{R_Z \,//\, R_2}{R_1 + R_X} \quad (40)$$

$$\omega_c = \frac{1}{C_Z\left(R_Z \,//\, R_2\right)} \quad (41)$$

In the order to make the gain of proposed VMIA controllable, the passive grounded resistances R_1 and R_2 are replaced by two active resistances structure based on MOS transistors, as shown in Fig. 13.

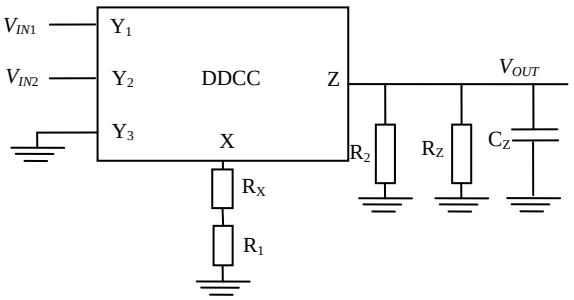

Fig. 12. Instrumentation amplifier circuit considering the present of parasitic elements

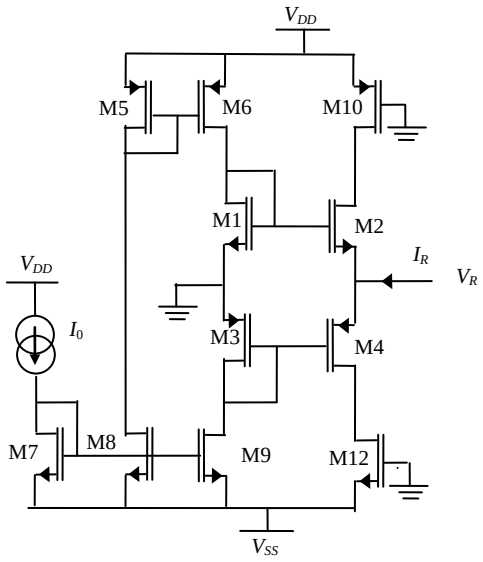

Fig. 13. Active resistance controlled by bias current I_0.

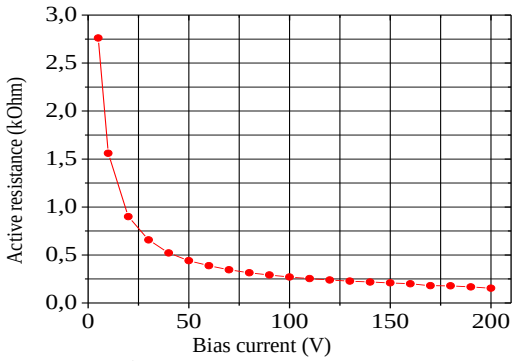

Fig. 14. Variation of active resistor values according by bias current I_0.

The active resistance circuit is composed by a mixed trans-linear loop (M1, M2, M3, M4), two current mirrors (M5, M6 and M7, M8, M9), two current sources (M10, M12) and a bias current I_0 [29]. Assuming that all transistors are operated in saturation region, the relationship between current I_R and voltage V_R is given by:

$$\frac{V_R}{I_R} = R = \frac{1}{\sqrt{2I_0 C_{ox}}\left(\sqrt{\mu_p\left(\frac{W}{L}\right)_{M4}} + \sqrt{\mu_p\left(\frac{W}{L}\right)_{M2}}\right)} \quad (42)$$

In the above equation, the resistance variation is inversely proportional to the variation of bias current I_0. To confirm this result, the active resistance circuit is simulated by ±0.8 V supply voltage and the aspect ratios (W/L) of the MOS transistors were taken as 30 µm/0.18 µm for M1-M2, 60 µm/0.18 µm for M3-M4, 0.27 µm/0.18 µm for M7-M9 and 10 µm/0.18 µm for M5-M6. Fig. 14 shows the variation of the resistance as a function of the bias current I_0.

The proposed instrumentation amplifier is simulated for differential voltage gain by fixed the bias current of resistance R_2 to 5µA and varied the bias current of resistance R_1 by 5 µA, 10 µA, 20 µA, 40 µA, 60 µA, 80 µA, and 100 µA, respectively. The variation of the differential gains as a function of frequency is shown in Fig. 15. It is clear that the simulated gains are equal to 0

dB, 4.95 dB, 9.73 dB, 12.46 dB, 15.01 dB, 17.67 dB and 19.15 dB, respectively. Also, these variations have a wide bandwidth equal to 83 MHz and independent to gain variations.

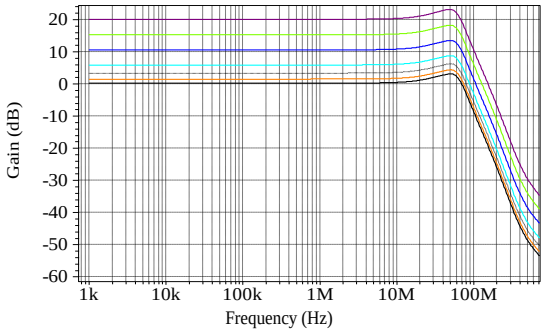

Fig. 15. Magnitude frequency response of VMIA.

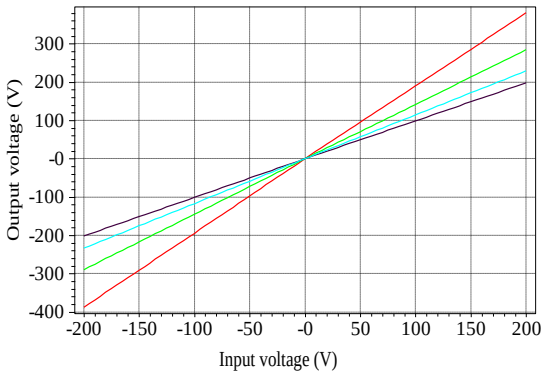

Fig. 16. DC transfer characteristics of VMIA.

Fig. 16 displays the DC gain of the instrumentation amplifier where a bias current of transistor R_1 fixed to 100 µA and the bias current of resistance R_2 varied of 40 µA, 60 µA, 80 µA and 100 µA.

The CMRR frequency response is shown in Fig. 17. In this figure, we see that the CMRR has a high value equal to 146 dB for low frequency at 100 kHz.

To observe the incompatibility of active resistance on the instrumentation amplifier's gain, a Monte-Carlo analysis is performed by selecting the bias current values of two resistances R_1 and R_2 to 100 µA with a 10% Gaussian deviation for 100 simulation runs. The statistical result in histogram is shown in Fig. 18 where the maximum, median and minimum numbers of circuit were found as 1, 0.98 and 0.97, respectively.

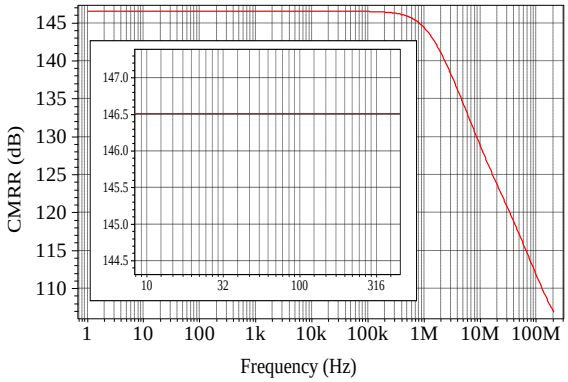

Fig. 17. CMRR frequency response of VMIA.

A comparison between the proposed circuit and others structures of instrumentation amplifiers presented in the literature is given in Table III.

Our amplifier has remarkable advantages over other circuits at the wide bandwidth, and the low supply voltage while maintaining a simple structure and a current controlled gain. Also the CMRR of the proposed circuit is higher than those of [30] but it is smaller than those of [31] while keeping a low consumption power.

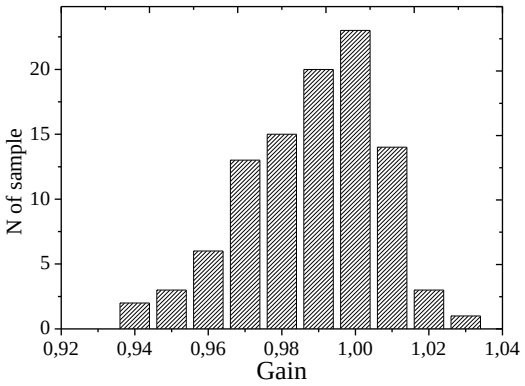

Fig. 18. Statistical results of Monte-Carlo analysis for VMIA with 10% deviation bias current I_0.

TABLE III. COMPARISON BETWEEN PROPOSED INSTRUMENTATION AMPLIFIER AND OTHERS PRESENTED IN THE LITERATURE

Reference	Technology CMOS	Supply voltage (V)	Bandwidth (MHz)	CMRR (dB)	Power consumption (mW)	Nr. of active devises	Passive component
[30]	0.35 µm TSMC	±3.3	70	142	0.519	2 CCCII	No
[31]	0.35 µm TSMC	±0.75	90	200	3.5	3 CCCII	Yes
[32]	0.25 µm TSMC	±1.5	8	---	1.74	1 DVCC	Yes
[33]	1.5 µm AMS	±2.5	0.11	150	---	3 OPA	Yes
Proposed IA	0.18 µm TSMC	±0.8	83	146	0.492	1 DDCC	No

V. CONCLUSION

A new CMOS realization for differential difference current conveyor circuit DDCC has presented in this paper. By using adaptive biasing circuit instead of use simple the constant bias current source, this circuit is characterized by large voltage mode and current mode dynamic ranges about ±0.62 V and ±0.35 mA respectively with low parasitic resistance R_X (6.86 Ω). The frequency responses of DDCC circuit show cut-off frequencies around 560 MHz with unity gain. The power consumption of circuit is about 472 µW.

As application, a voltage mode instrumentation amplifier circuit composed by one DDCC circuit and two grounded active resistances has proposed. This VMIA circuit is characterized by controllable gain, wide bandwidth (83 MHz), a high common-mode rejection ratio (CMRR) about 146 dB for different values of gain.

The simulation results of proposed controlled VMIA are verified with TSPICE using 0.18 μm TSMC CMOS technology. It has a good accuracy with the theoretical results where the power consumption is about 0.492 mW.

CONFLICT OF INTEREST

Please declare whether or not the submitted work was carried out with a conflict of interest. If yes, please state any personal, professional or financial relationships that could potentially be construed as a conflict of interest. If no, please add "The authors declare no conflict of interest".

AUTHOR CONTRIBUTIONS

Please state each author's contribution to this work, it can be up to several sentences long and should briefly describe the tasks of individual authors. e.g., Author A and Author B conducted the research; Author C and Author D analyzed the data; Author A and Author B wrote the paper; ...; all authors had approved the final version.

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