

# A Differential Cross-Coupling Common Gate Low Noise Amplifier (LNA) for MedRadio Band Application

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**Abstract**—In this paper, we present an ultra-low-power Low Noise Amplifier (LNA) for MedRadio band application. The LNA in this paper is known as differential cross-coupling common gate amplifier. The main structure of the design is the common gate configuration amplifier. A new technique such as cross-coupling technique is integrated to improve the gain and noise figure of the amplifier. The differential topology is finally implemented to improve the overall performance of the LNA. The final LNA is implemented in CMOS by using Silterra's CMOS 180 nm technology. The LNA is designed with voltage supply equal to 1 V. The current consumption is equal to 0.2 mA. Therefore, the overall power consumption of the LNA is equal to 0.2 mW. Apart from this, the final simulated power gain for complete differential cross-coupling common gate amplifier is equal to 17.2 dB, and the simulated noise figure is equal to 5.4 dB. The designed LNA can operate from 80 MHz to 800 MHz. In addition, MOSCAPs are used to replace all the conventional passive capacitors in order to reduce the overall area of the LNA.

**Index Terms**—CMOS, integrated circuit, low noise amplifier, MedRadio

## I. INTRODUCTION

There have been some extensive research and development activities on wireless communications for biomedical purposes, especially for diagnostic and therapeutic medical implants and body-worn medical devices. All wireless communication for biomedical devices is operated in a standard frequency band which is known as medical device radio communications service (MedRadio) frequency band. These frequency bands are 401-406 MHz, 413-419 MHz, 426-432 MHz, 438-444 MHz, and 451-457 MHz.

In wireless devices, Low-Noise Amplifier (LNA) is an important component to ensure a sufficient gain is provided for the received signals. This is to ensure the wireless devices can receive a low and weak signal. One critical issue for all the biomedical devices is human body exposure to excessive Radio Frequency (RF) radiation. Hence, proper handling of the RF signal is essential.

Besides, for the wireless application, low power consumption and small size are a must.

In 2015, a 1.3 mW current-reuse RF front-end for MICS (medical implant communication services) band (from 402 MHz to 405 MHz) was reported [1]. This is a wide-band low-power super-heterodyne RF receiver front-end, and its main components are a LNA and a mixer. It was implemented in a 0.18  $\mu\text{m}$  standard CMOS process with an area of less than 1.7  $\text{mm}^2$ . Based on measurements results, maximum conversion gain of 30 dB, the noise figure of 11.6 dB and 13.2 dB when operating at 1.3 mW and 2.9 mW respectively, and minimum sensitivity of  $-97\text{dBm}$  had been achieved.

Common gate topology has been widely investigated in LNA design recently. This is because it has shown its significant advantages over other topologies such as common source topology. The common gate LNA can provide wider bandwidth, better linearity, higher stability, and less dependency on the process, voltage, and temperature (PVT) variations [2], [3]. The main attractive characteristic of the common gate topology is that the input impedance is equal to  $1/g_m$  [4]. Since the input impedance is  $1/g_m$ , by increasing  $g_m$  value, the gain and input impedance can be set simultaneously. However, this characteristic also contributes to some drawbacks [4]. It causes the common gate circuit to have a higher noise figure. Although it shows bad noise handling, common gate circuit still provides some good characteristic such as good linearity. Hence, some appropriate techniques, such as cross-coupling technique [5], is usually implemented to overcome this limitation.

There are several feedback techniques [6] which can be used to improve the performance of the common gate topology. Positive-negative feedback technique is used to boost the gain, reduce noise figure, and reduce the power consumption of the common gate circuit. Two feedback paths are introduced in the common gate low-noise amplifier [7]. The first feedback path is capacitive cross-coupling. The technique can provide a high gain and low noise figure. The second feedback path is the cross connection between the drain and the source of the differential pair. The second feedback path can improve the linearity of the amplifier. However, the overall gain may be affected by the first feedback path.

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Other than improving the linearity of an LNA by using a feedback technique, it can also be used to reduce the input and output impedance. It is a popular method of impedance matching. Some works [8]-[10] had used this approach, but in all these works, the LNA power consumption is approximately 2 mW or greater.

Specific biasing approach for power consumption reduction such as subthreshold region biasing was employed in [8]. Although subthreshold region biasing can significantly reduce the power consumption of the amplifier, it is a sensitive region. Since it is operated at a voltage lower than the threshold voltage, a slight deviation of the voltage may affect the overall result of the amplifier. Besides, the subthreshold region will also reduce the gain and increase the noise figure of the amplifier if the current remains low [11]. Apart from these drawbacks, there are few additional drawbacks mentioned in [12]. In the subthreshold region, the frequency response and linearity of the amplifier are poor.

Consequently, the complexity of the amplifier is increased. The subthreshold region concept is also used with the differential common gate topology to provide average 17 dB gain, 4.2 dB noise figure and 0.2 mW power consumption [13]. The supply voltage is 1 V, and the operating frequency is from 400 MHz to 1 GHz.

In this paper, a differential cross-coupling common gate amplifier low noise amplifier is proposed, which has been simulated successfully. It is targeted for applications with low power consumption and small size.

## II. METHODOLOGY

### A. Research Flow

In designing the LNA, several techniques or topologies must be combined to achieve the desired power, noise, and gain. All the techniques have their advantages and disadvantages in handling the power, noise, gain, and operating frequency. Even though some techniques can significantly improve one of the factors stated above, they may have a trade-off with other factors. So, throughout the design of LNA circuitry, some factors need to be considered carefully, such as power consumption, amplifier gain, frequency, voltage level, and numerous others. The general design flow for the low noise amplifier is shown in Fig. 1.

The first step is a single-stage common gate amplifier design. In this step, a single-ended input is applied to the single-stage common gate amplifier to generate a single-ended output signal. The design is started with an ideal current source. After all the parameters value is determined, the ideal current source is replaced with the non-ideal current source.

The second step is the implementation of capacitive cross-coupling technique. Conventionally, the idea of capacitive cross-coupling technique is applied to the differential pair. However, to simplify the design, the technique is first implemented in the single-stage common gate amplifier. The differential input signals are inserted to the amplifier to generate a single-ended output signal. The first input signal is inserted into the source

terminal of the transistor, while the second input signal is inserted into the gate terminal of the transistor.

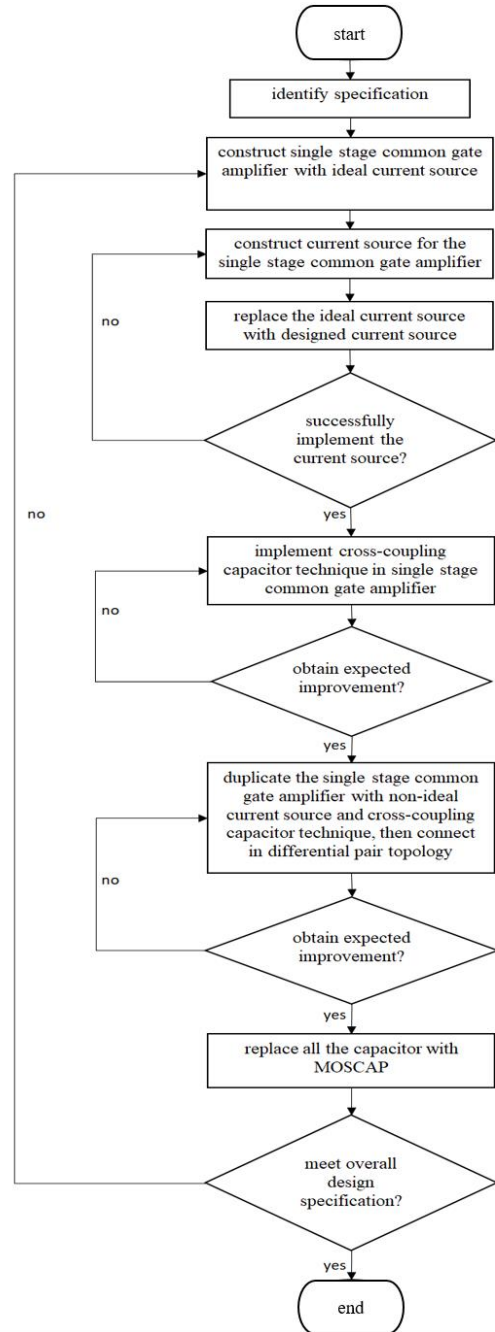


Fig. 1. Flow chart.

The third step is the implementation of differential cross-coupling common gate amplifier. In this step, two common-gate amplifiers are configured as a differential pair. The differential input signals are inserted at each common gate amplifier to generate differential output signals.

The last step is the final or complete LNA design. Size of the LNA is also an important aspect. All the passive capacitors used in the previous amplifier are replaced with the MOSCAP. This is because the conventional passive capacitor consumes a bigger area compared to MOSCAP with the same capacitance value. By referring to work [14], the detail explanation about the properties

of MOSCAP at different operation regions can be obtained.

### B. Circuit Design and Analysis

As discussed in the previous section, before the final LNA is designed, two amplifiers are initially designed. The design and analysis of these amplifiers are discussed in the next sections.

1) *Common Gate Amplifier*: The attractive feature of the single-stage common gate amplifier topology (Fig. 2) is low input resistance. The input resistance is given by

$$R_{in} = \frac{1}{G_m} = \frac{1}{(1/r_{o1} || r_{o2}) + g_m + g_{mb}} \quad (1)$$

where  $g_m$  is the transconductance,  $g_{mb}$  is the body-effect transconductance,  $r_{o1}$  is the output resistance of common gate transistor (M1), and  $r_{o2}$  is the output resistance of the current source (M2).

The basic transconductance is

$$g_m = \frac{2I_D}{V_{gs} - V_{th}} \quad (2)$$

where the  $I_D$  is common gate current consumption,  $V_{gs}$  and  $V_{th}$  are gate-source voltage and the threshold voltage of common gate transistor respectively.

$$g_{mb} = \gamma \sqrt{\frac{k(W/L)I_D}{2(2\phi_F + V_{sb})}} \quad (3)$$

where  $\gamma$  is bulk threshold parameter,  $k$  is transconductance parameter,  $W/L$  is the ratio of width over length of the transistor,  $\phi_F$  is surface potential, and  $V_{sb}$  is source-body voltage.

The small-signal output resistance of common gate transistor and the current source is:

$$r_{o1} \text{ or } r_{o2} = \frac{1}{\lambda I_D} \quad (4)$$

where  $\lambda$  is the channel length modulation parameter. When  $I_D$  is set at 0.1 mA,  $V_{gs}$  is 0.6 V, and  $V_{th}$  is 0.55 V,  $g_m$  is, therefore, equal to 4 mS. When  $k$  is equal to 110  $\mu\text{A V}^{-2}$ ,  $\gamma$  is equal to 0.48,  $\phi_F$  is equal to 0.3 V, and  $V_{sb}$  is equal to 0.1 V. Hence  $g_{mb}$  is 0.32 mS. When  $\lambda$  value is equal to 450  $\text{mV}^{-1}$ ,  $r_{o1}=r_{o2}=22.22 \text{ k}\Omega$ . By using (1), the input resistance is, therefore 226.7  $\Omega$ .

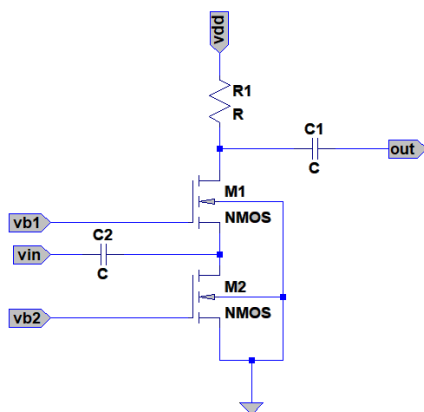


Fig. 2. Single stage common gate amplifier.

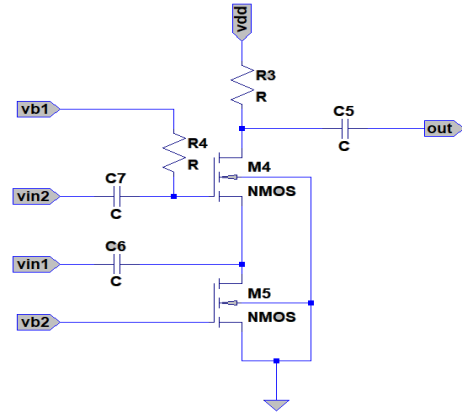


Fig. 3. Single stage common-gate amplifier with cross-coupling capacitor technique.

The output resistance of the single-stage common gate amplifier,  $R_{out}$  is 4.08 k $\Omega$  ( $r_{o1}$  is in parallel with  $R_D$ ). Therefore it is easy to calculate the gain ( $G_m \times R_{out}$ ) of the single-stage common gate amplifier, which is approximately equal to 27 dB.

2) *Cross-Coupling Amplifier*: By using the cross-coupling technique, the transconductance of the single-stage common gate amplifier is increased by a factor of 2. The coupling capacitor is equal to 23 pF. The coupling capacitor value is chosen based on the operating frequency. The amplifier is shown in Fig. 3.

3) *Differential Cross-Coupling Common Gate Amplifier*: Differential topology has also doubled the gain due to the doubling of transconductance (of a single stage common gate amplifier with capacitive cross-coupling technique). The noise factor of the LNA is

$$F = 1 + \frac{1}{\alpha g_m R_s} \Big|_{\alpha} \quad (5)$$

where  $\alpha$  is a cross-coupling factor, and  $R_s$  is source resistance. So by increasing the  $g_m$ ,  $F$  will be reduced.

The cross-coupling may cause the LNA to become unstable, so the stability must be investigated. The complete LNA is depicted in Fig. 4.

### C. Test Bench

The test bench of the LNA is shown in Fig. 5. A transformer is used to convert the single-ended signal to a differential signal and vice versa. The test buffer (common drain buffer) is connected to the output of the LNA. The schematic of test buffer is shown in Fig. 6.

As the test buffer is connected at the output of the LNA, it is now can be considered two amplifiers in a cascade topology. The simplified total noise factor is then given by

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} \quad (6)$$

where  $F_1$  and  $G_1$  are the noise factor and power gain of the LNA, respectively. The  $F_2$  is the noise factor of the test buffer. Hence, by using (6), the noise figure of the test buffer has no significant influence on the overall performance of the LNA noise figure when the LNA power gain is high.

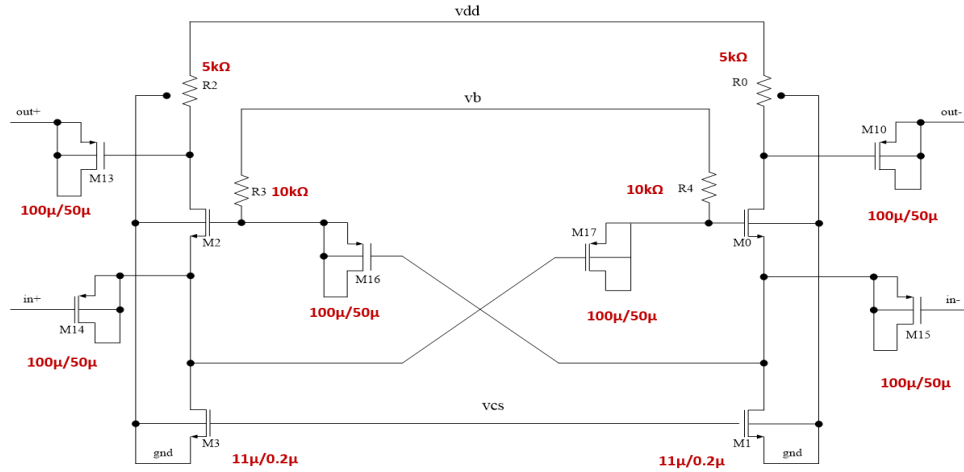


Fig. 4. LNA schematic.

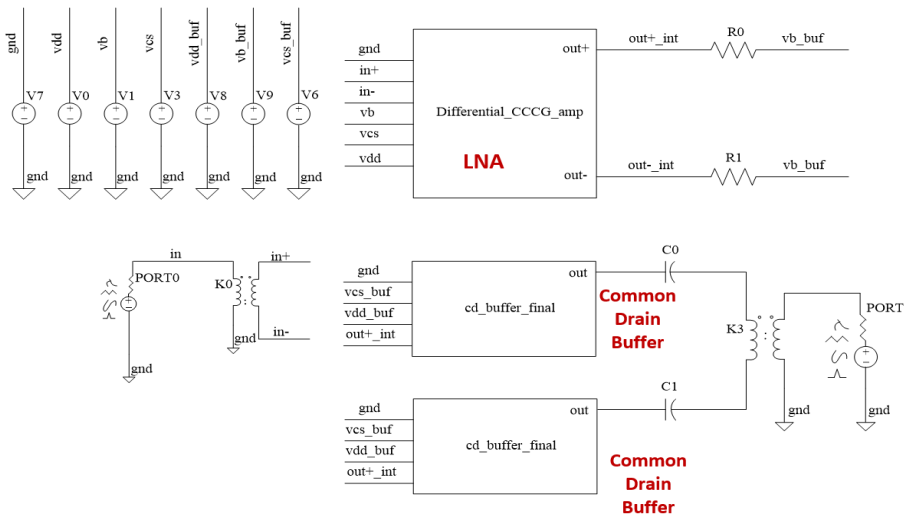


Fig. 5. The LNA and common drain buffer test bench

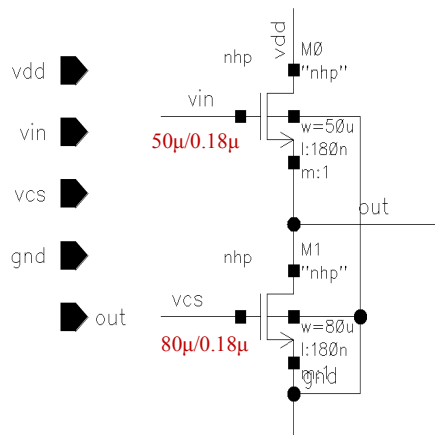


Fig. 6. Common Drain Buffer Schematic.

The total current consumed by the buffer is equal to 5.81 mA, and the voltage supply to the buffer is equal to 2 V. Therefore, the total power consumption of the test buffer is equal to 11.62 mW. Apart from that,  $r_o$  resistance of the buffer is equal to 382.48  $\Omega$ ,  $g_m$  value is equal to 46.48 mS, and  $g_{mb}$  of the buffer is equal to 3.58 mS. Hence, by substituting these values into (1), the output resistance of the buffer is 18  $\Omega$ .

TABLE I. THE SIMULATED PERFORMANCE OF AMPLIFIERS

Amplifier Topology	Peak power gain (dB)	Noise figure (dB) at 450 MHz	Frequency bandwidth (MHz)
Single stage common gate amplifier	11.09	11.37	70-800
Single stage common gate amplifier with cross-coupling technique	14.48	7.65	80-800
Differential cross-coupling common-gate amplifier (the LNA)	17.19	5.39	100-800

### III. RESULTS

All three amplifiers results were simulated by using Silterra's CMOS 180 nm technology model. Table I summarizes the three amplifiers results.

From Table I, the capacitive cross-coupling technique has increased the gain by 3.39 dB (from the single-stage common gate amplifier). The noise figure (NF) is also improved by 3.72 dB. Furthermore, the performance is further improved using differential topology. After implementing the differential topology, the gain is further

increased by 2.71 dB, and the noise figure (NF) is reduced by 2.26 dB. Overall frequency bandwidth remains the same at around 80 MHz to 800 MHz.

After integrating the cross-coupling technique, the gain is increased because the additional differential input is applied to the single-stage common gate configuration. With the additional differential input, the transconductance of the amplifier is doubled. Originally, with conventional common gate configuration, the transconductance,  $G_m$  is equal to the transconductance of the transistor.

Due to the effect of parasitic capacitances and the input capacitance of the buffer not included in the calculated voltage gain, there is a big difference between the calculated open-circuit voltage gain and  $S_{21}$  (power gain).

Fig. 7 and Fig. 8 show the simulated  $S$  parameters responses and noise figure of the LNA, respectively. From the plotted results, the response is from 400 MHz to 900 MHz. The simulated input return loss ( $|S_{11}|$ ) is less than 5 dB while the simulated output return loss ( $|S_{22}|$ ) is less than 10 dB at the MedRadio band frequency range. The achieved simulated  $S_{12}$  is  $-60$  dB at the same frequency range. The  $S_{21}$  is 17.2 dB at the same frequency range.

From (7), the stability factor ( $k_f$ ) of the LNA is equal to 52.774. Since  $k_f$  is greater than 1, the LNA is therefore stable.

$$k_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{21}S_{12}|^2}{2|S_{21}||S_{12}|} \quad (7)$$

The achieved NF is less than 5.6 dB at the interested frequencies. The NF is less than 5.39 dB at 450 MHz and higher.

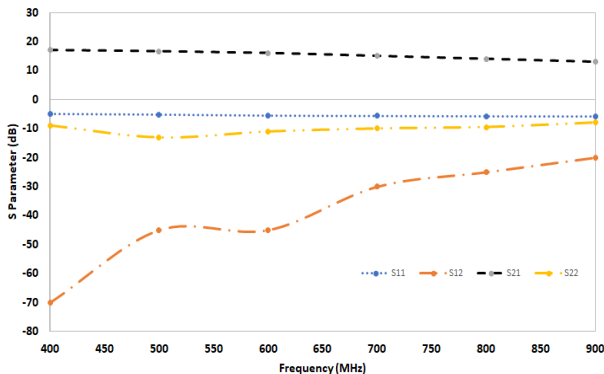


Fig. 7. Simulated  $S$ -parameters results of the LNA

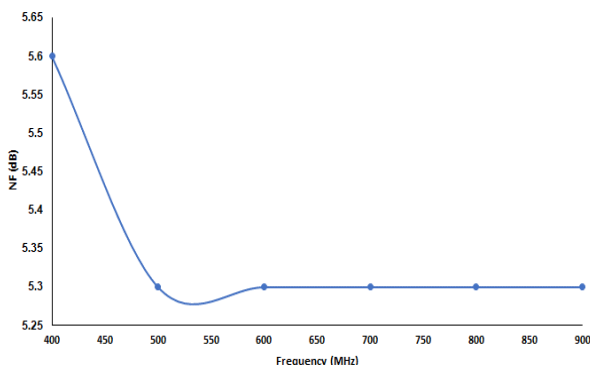


Fig. 8 Simulated noise figure LNA.

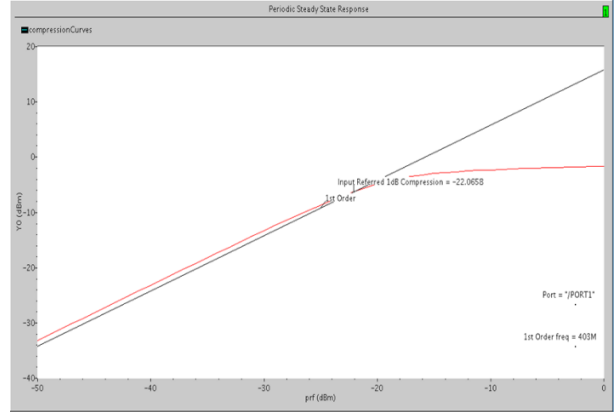


Fig. 9. IP1dB plot at 402 MHz for differential cross-coupling common gate amplifier.

TABLE II. PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

Method	BW (GHz)	Power Gain (dB)	IIP3 (dBm)	Pdc (mW)	NF (dB)	Area (mm <sup>2</sup> )
This Work	0.7	17.19	-11.85	0.2	5.39@450 MHz	0.037
[6]	0.62	21	-3.2	3.6	2	0.33
[13]	0.6	18	-21	0.2	4.2	0.27
[15]	-	18.5	-19	0.6	4.6	0.06
[16]	2.1	12.3	-11.5	0.4	4.9	0.005
[17]	1.35	16.9	-5.5	9.3	2.5	0.075

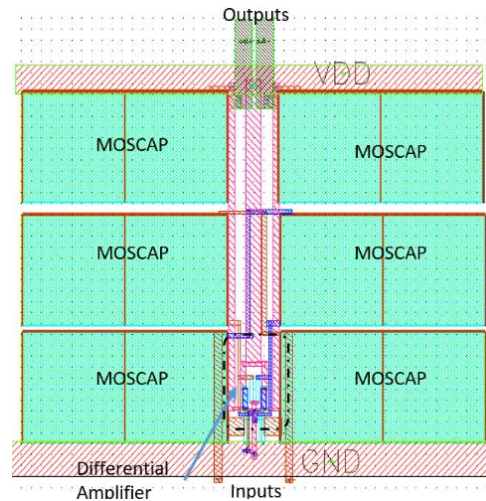


Fig. 10. Cross-coupling common gate amplifier layout.

The linearity of the LNA is shown in Fig. 9. From the figure, the IP1dB is equal to  $-22.065$  dBm.

From Table II, the proposed LNA is comparable with current works. The IIP3 is approximate  $-11$  dBm, which is acceptable for a low noise amplifier. The achieved power consumption, which is 0.2 mW is quite low and comparable to some of the works.

The area of the proposed LNA is estimated to be  $177 \mu\text{m} \times 210 \mu\text{m}$ . The size of the LNA is quite small compared to other works. The layout of the proposed LNA is shown in Fig. 10.

#### IV. CONCLUSIONS

The proposed LNA employs a common gate configuration as the main structure of the LNA. A cross-coupling technique is employed with the main structure



to improve the gain and noise figure of the LNA. Finally, the differential topology is implemented to improve the overall performance of the LNA further. The proposed LNA is designed with a supply voltage of 1 V. The current consumption is 0.2 mA. Hence, overall power consumption for the LNA is equal to 0.2 mW. Apart from this, the simulated power gain of the proposed LNA is 17.19 dB. The simulated noise figure of the proposed LNA is 5.39 dB. The small size of LNA is accomplished by replacing the conventional passive capacitors with MOSCAPs. The common gate topology is employed to reduce the potential of PVT variation.

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