Clock Generator with Exponentially Increasing Frequency Using Switched-Capacitor Circuit

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***Abstract*—Charging and discharging waveforms in an RC circuit are changed exponentially. The change gradually decreases over time and approaches a steady-state value, since the power of the exponential is negative. However, depending on applications, a diverging signal may be required. In this case, the power of the exponential is positive, and the signal gradually increases over time. In this paper, a clock generator is proposed whose frequency is increased exponentially over time. The proposed circuit can generate exponentially increasing voltage and clock signals with high accuracy over a wide operating range by using Switched-Capacitor (SC) technique. The generated voltage and the clock frequency are derived theoretically. Moreover, the design formulas for finding the circuit parameters with the initial value and the final value are also derived. The theoretical analysis of the proposed circuit is confirmed by experiments and SPICE simulations. From the experiments and the simulations, the clock frequency and the voltage are changed exponentially 1 kHz ~ 20 kHz and 0.4 V ~ 7.9 V, respectively. As an application, the Cockcroft-Walton circuit is driven by the proposed clock generator.**

***Index Terms*—charge pump circuit, clock generator, exponential increase, fast start-up, small inrush-current, switched-capacitor**

I. Introduction

When a capacitor is charged by using a charge pump circuit [1], the charging voltage changes exponentially. Since the power of the exponential is negative, the charging voltage increases rapidly at startup, but the increase rate decreases as time passes and finally reaches a steady state value. If the value of the capacitance is large, the inrush-current becomes large and the charging time become longer as well. Usually, the clock frequency of a charge pump circuit is constant.

In this paper, a clock generator is proposed whose frequency is increased exponentially over time. The proposed circuit can generate exponentially increasing voltage and clock signals with high accuracy over a wide operating range by using switched-capacitor (SC) [2]-[15] technique. A conventional method to increase the clock frequency exponentially is as follows. First, a linearly increasing voltage is obtained by a sawtooth wave generator, and the voltage is added to an exponential-gain amplifier to obtain the exponentially increasing voltage [16], [17]. Next, the voltage is applied to a voltage controlled oscillator (VCO) to generate a clock with an exponentially increasing frequency. This method is complicated and has low accuracy, since the exponential voltage generator generates pseudo exponential voltage by using the nonlinear characteristic of MOSFET or diode.

In order to obtain a high accurate exponential signal, Section II explains a conventional circuit [18] using digital method. In Section III, the proposed VCO and its operation are explained before describing the whole circuit. Section IV describes the parameter of the ideal exponential function to compare with the exponential characteristic of the proposed circuit. In Section V, the circuit configuration and the operating principle of the proposed exponential clock generator are described, and the theoretical expressions of the generated voltage and the clock frequency are derived. In Section VI, the theoretical equations are derived for determining the circuit parameters with the minimum frequency at startup and the maximum frequency at final time. Section VII graphs the theoretical expressions of the generated voltage and the clock frequency, and shows that they almost match the characteristics of the ideal exponential function. In Section VIII., the theoretical characteristics are confirmed by measuring a test circuit and by simulation program with integrated circuit emphasis (SPICE). In Section IX, as an example of the application of the proposed circuit, the charging characteristics of the Cockcroft-Walton circuit [1] driven by the proposed clock generator is described. Finally, the results of this study are summarized in Section X.

II. Conventional Exponential Voltage Generator

Fig. 1 shows the conventional exponential voltage generator [18] using digital method. This circuit has a wide operating range and is stable and accurate. By the

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adder circuit composed of the operational amplifier and the 10 kΩ resistors, the output voltage v_o is given by

$$v_o = V_o + V_{DA} \tag{1}$$

When the output of the counter is n in decimal and the minimum step voltage corresponding to the LSB of the D-A converter is Δv, v_o is expressed by

$$v_o = V_o + n\Delta v \tag{2}$$

Assuming the coefficient of the V-F converter is α, the output frequency f_o is αv_o, the nth-clock frequency f_n and the clock period T_n are given as follows, respectively.

$$f_n = \alpha\left(V_o + n\Delta v\right) \tag{3}$$

$$T_n = \frac{1}{\alpha\left(V_o + n\Delta v\right)} \tag{4}$$

The waveforms of f_o and v_o in Fig. 1 are as shown in Fig. 2. From the figure the time t is given by

$$t = \sum_{m=0}^{n}\frac{1}{T_m} = \sum_{m=0}^{n}\frac{1}{\alpha\left(V_o + m\Delta v\right)} \tag{5}$$

The above equation can be approximated as follows if n is sufficiently large.

$$t \simeq \frac{1}{\alpha\Delta v}\ln\left(\frac{V_o + n\Delta v}{V_o}\right) = \frac{1}{\alpha\Delta v}\ln\left(\frac{v_o}{V_o}\right) \tag{6}$$

Therefore, the output voltage v_o and the output frequency f_o are increased exponentially, given in (7) and (8). The powers of the exponential are positive.

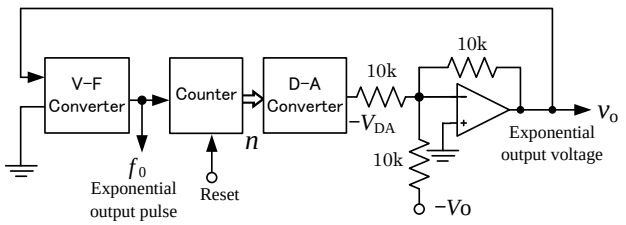

Fig. 1. Conventional exponential voltage generator.

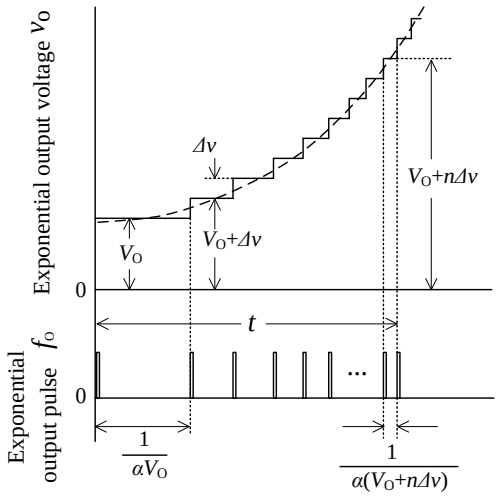

Fig. 2. Waveforms in Fig. 1.

$$v_o \simeq V_o\varepsilon^{\alpha\Delta vt} \tag{7}$$

$$f_o = \alpha v_o \simeq \alpha V_o\varepsilon^{\alpha\Delta vt} \tag{8}$$

III. Proposed VCO

In this Section, the circuit configuration and its operation of the proposed VCO (voltage controlled oscillator) will be explained, before describing the whole circuit. Fig. 3 and Fig. 4 show the circuit configuration and the waveforms of the proposed VCO, respectively. The squared symbols 1 and 2 in Fig. 3 are CMOS analog switches, they are turned on during the clocks Φ_1, and Φ_2 are in a high level "H", respectively. The input voltage V_2 is a positive DC voltage. Since the initial charge of the capacitor C_3 is 0 at t=0, the output voltage V_3 of the operational amplifier Op3 is 0, and the output voltage V_4 of the comparator Op4 is saturated at V_{SS}. When the outputs Φ_1 and Φ_2 of the T-FF are "H" and "L" respectively, the switch 1 is turned on and the switch 2 is turned off. Thus, V_3 is

$$V_3 = -\frac{V_2}{C_3R_3}t \tag{9}$$

As shown in Fig. 4, V_3 decreases linearly. When V_3 falls below $-E_r$, V_4 saturates at V_{DD}, and the output clocks Φ_1 and Φ_2 are inverted. At this timing, since the capacitor C_3 is connected in the reverse direction, the voltage V_3 drops linearly from $+E_r$, and the above operation is repeated.

From Fig. 4 pulse width T_3 is determined as

$$T_3 = \frac{2C_3R_3E_r}{V_2} \tag{10}$$

Therefore, the clock frequency f of VOC is proportional to the input voltage V_2 as follows:

$$f = \frac{1}{2T_3} = \frac{1}{4C_3R_3E_r}V_2 \tag{11}$$

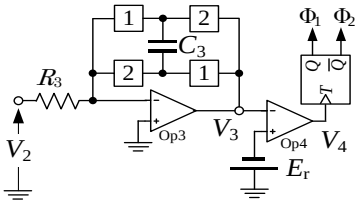

Fig. 3. Proposed VCO.

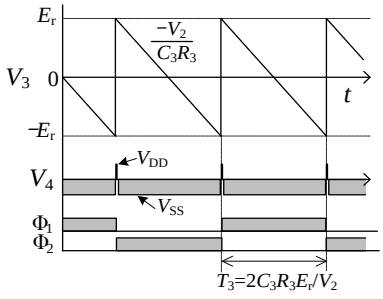

Fig. 4. Waveforms in VCO of Fig. 3.

When $V_2 = V_{2\min}$ and $V_{2\max}$, $f = f_{\min}$ and $f_{\max}$, respectively, then,

$$f_{\min} = \frac{1}{4C_3R_3E_r}V_{2\min} \tag{12}$$

$$f_{\max} = \frac{1}{4C_3R_3E_r}V_{2\max} \tag{13}$$

From the above equations, R_3 and $V_{2\min}$ are determined as follows.

$$R_3 = \frac{V_{2\max}}{4C_3E_r f_{\max}} \tag{14}$$

$$V_{2\min} = \frac{f_{\min}}{f_{\max}}V_{2\max} \tag{15}$$

Here, $V_{2\min}$ cannot be arbitrarily selected from the above equation, however, there is no problem in the case of using only the exponential clock f. The resistor R_3 can be replaced by an SC resistor. In this case, the circuit can be configured completely by SC.

IV. Specifications for Ideal Exponential Siglal

In this section, the ideal circuit parameters for designing an exponential signal are described. Table I shows the specifications of the exponential signal to be designed. In this table, the values of black character are given, and the red ones are calculated using the equations of the right column in the table. Assuming that the output clock frequency $f(t)$ and the output voltage $V_2(t)$ are $f_{\min}$ and $V_{2\min}$ at $t=0$, respectively, and the time constants of the frequency and the voltage are τ_f and τ_v, then the both are expressed as

$$f(t) = f_{\min}e^{\frac{t}{\tau_f}} \tag{16}$$

$$V_2(t) = V_{2\min}e^{\frac{t}{\tau_v}} \tag{17}$$

Since $f(t)$ and $V_2(t)$ are exponentially increased, and they reach $f_{\max}$ and $V_{2\max}$ at $t=t_{\max}$, respectively, the time constants τ_f of the frequency is given by

$$f_{\max} = f_{\min}e^{\frac{t_{\max}}{\tau_f}} \tag{18}$$

$$\tau_f = \frac{t_{\max}}{\ln(f_{\max}/f_{\min})} \tag{19}$$

Table I. Specifications of Ideal Exponential Signal.

ITEMS	SYMBOL	VALUES*	Eq.
Minimum frequency	$f_{\min}$	1 kHz	
Maximum frequency	$f_{\max}$	20 kHz	
Minimum output voltage	$V_{2\min}$	0.10 V	
Maximum output voltage	$V_{2\max}$	10.00 V	
Maximum time of t	$t_{\max}$	0.50 s	
Frequency time constant	τ_f	0.109 s	(19)
Voltage time constant	τ_v	0.109 s	(21)

*The red values are calculated by equations of the right column.

In the same way the time constant τ_v of the voltage is

$$V_{2\max} = V_{2\min}e^{\frac{t_{\max}}{\tau_v}}, \tag{20}$$

$$\tau_v = \frac{t_{\max}}{\ln(V_{2\max}/V_{2\min})} \tag{21}$$

V. Proposed Exponential Clock Generator

Fig. 5 shows the circuit configuration of the proposed clock generator. In Fig. 5, the voltage V_1 is a small negative DC voltage $-\Delta V$. The upper half of the figure is SC integrator, and the lower half is the proposed VCO in Fig. 3. If the initial voltages of all capacitors $C_1 \sim C_3$ at $t=0$ are 0, V_2 and V_3 are always 0 and the clocks Φ_1 and Φ_2 do not start. Thus, to start the clocks, the DC voltage $V_{2\min}$ and the clock Φ_0 are added to the circuit. As shown in Fig. 5, when $t<0$, Φ_0 is "H" and at $t=0$, Φ_0 changes "L". Therefore, at $t=0$ the initial voltage of C_2 is set to $V_{2\min}$.

In the upper half of the circuit, when the switch 1 is turned on, C1 is charged up to V1= – V. When the switch 2 is turned on, C_1 is discharged, and all charge of C_1 move to C_2, since the inverting input terminal of the operational amplifier Op2 is virtually grounded. Therefore, at $t=T^-$ the final V_2 in the first cycle of the clock is given by

$$V_2(t=T^-) = \frac{(C_2V_{2\min} + C_1\Delta V)}{C_2} = V_{2\min} + \frac{C_1}{C_2}\Delta V \tag{22}$$

In the same way, during next cycle, the all charge ΔVC_1 of C_1 is moved to C_2. Therefore,

$$\begin{aligned} V_2(t=2T^-) &= \frac{(C_2V_{2\min} + 2C_1\Delta V)}{C_2} \\ &= V_{2\min} + 2\frac{C_1}{C_2}\Delta V \end{aligned} \tag{23}$$

The above steps are repeated, and V_2 in the n-th cycle is

$$V_2(t=nT^-) = V_{2\min} + n\frac{C_1}{C_2}\Delta V \tag{24}$$

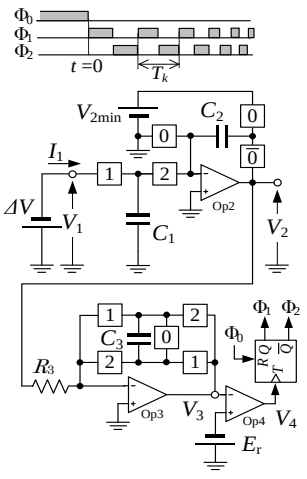

Fig. 5. Proposed exponential clock generator.

The lower half of Fig. 5 during $t > 0$ is the same as the VCO of Fig. 3. From (11), the clock frequency f_n of the n-th cycle is

$$f_n = \frac{1}{4C_3R_3E_r}V_2\left(t = nT^-\right) \tag{25}$$

From (24) and (25), the clock cycle T_n of the n-th cycle is

$$T_n = \frac{1}{f_n} = \frac{4C_3R_3E_r}{V_{2\min} + n\dfrac{C_1}{C_2}\Delta V} \tag{26}$$

Therefore, the time t is expressed as follows by adding the period T_n of the above equation:

$$t = \sum_{m=0}^{n} T_m \tag{27}$$

$$t = \frac{4C_3R_3E_r}{V_{2\min}}\sum_{m=0}^{n}\frac{1}{1+\dfrac{C_1\Delta V}{C_2V_{2\min}}m} \tag{28}$$

Here, the above equation can be approximated as follows if n is sufficiently large:

$$t \simeq \frac{4C_3R_3E_r}{V_{20}\dfrac{C_1\Delta V}{C_2V_{2\min}}}\ln\left(1+\frac{C_1\Delta V}{C_2V_{2\min}}n\right) \tag{29}$$

From (24),

$$t \simeq \frac{4C_2C_3R_3E_r}{C_1\Delta V}\ln\left\{\frac{1}{V_{2\min}}V_2(t)\right\} \tag{30}$$

From the above equation, $V_2(t)$ is obtained as follows:

$$V_2(t) \simeq V_{2\min}\varepsilon^{\frac{C_1\Delta V}{4C_2C_3R_3E_r}t} = V_{2\min}\varepsilon^{\frac{t}{\tau}} \tag{31}$$

where the voltage time constant τ is

$$\tau = \frac{4C_2C_3R_3E_r}{C_1\Delta V} \tag{32}$$

Substituting (31) into (11), the clock frequency f is given by

$$f = \frac{1}{4C_3R_3E_r}V_{20}\varepsilon^{\frac{C_1\Delta V}{4C_2C_3R_3E_r}t} = f_{\min}\varepsilon^{\frac{t}{\tau}} \tag{33}$$

where

$$f_{\min} = \frac{1}{4C_3R_3E_r} \tag{34}$$

The time constants of the voltage and the frequency are the same and cannot be set independently, however, there is no problem in the case of using only the exponential clock.

VI. Method of Determining Element Value of Proposed Circuit

In this section, the method of determining the circuit parameter is described from the circuit operation and the theoretical analysis described above. Table II shows examples of the circuit parameters of Fig. 5. In Table II, the values of the black character are given, and the red ones are calculated using the equations of the right column in the table.

Assuming that $t = t_{\max}$ at the $n_{\max}$-th clock, from (24), $V_{2\max}$ is

$$V_{2\max} = V_{2\min} + n_{\max}\frac{C_1}{C_2}\Delta V \tag{35}$$

Then, the capacitor C_1 is

$$C_1 = \frac{V_{2\max} - V_{2\min}}{n_{\max}\Delta V}C_2 \tag{36}$$

The time constant τ in (32) is determined to match (21) of the ideal exponential function, then τ is

$$\tau = \frac{4C_2C_3R_3E_r}{C_1\Delta V} = \frac{t_{\max}}{\ln\left(f_{\max}/f_{\min}\right)} \tag{37}$$

From (36) and (37), $n_{\max}$ is given by

$$n_{\max} = \frac{V_{2\max} - V_{2\min}}{4C_3R_3E_r}\tau \tag{38}$$

TABLE II. Determination of Proposed Circuit Parameters

Items	Symbol	Values*	Eq.
Capacitor	C_1	0.01 nF	(36)
Capacitor	C_2	1.0 nF	
Capacitor	C_3	2.0 nF	
Resistor	R_3	1.25 kΩ	(14)
Step voltage of V_2	ΔV	0.10 V	
Comparison voltage	E_r	10.0 V	
Minimum voltage of V_2	$V_{2\min}$	0.10 V	(15)
Maximum voltage of V_2	$V_{2\max}$	10.0 V	
Minimum clock frequency	$f_{\min}$	1 kHz	
Maximum clock frequency	$f_{\max}$	100 kHz	
Maximum time of t	$t_{\max}$	0.50 s	
Number of clock iterations at $t=t_{\max}$	$n_{\max}$	10,749	(38)
Time constant	τ	0.109 s	(19)

*The red values are calculated by equations of the right column.

VII. Characteristics Analysis of Proposed Circuit

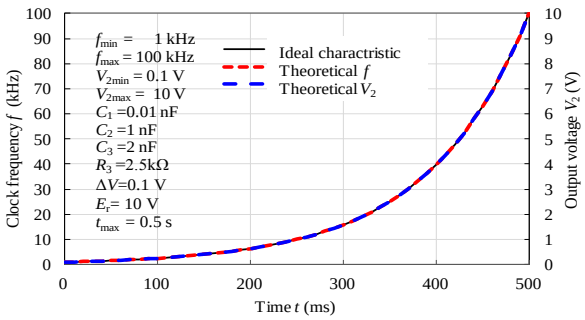

Fig. 6. Time change of clock frequency f and output voltage V_2.

From the above results, the characteristics of the proposed circuit are obtained by using the parameters in Table II. Without using (29) in the approximation of $\log_e$, the period T_n of each state is calculated by (26) and the

time t is exactly calculated by adding of (27). Fig. 6 show the changes of f and V_2 from t = 0 to t_{max}=0.5 s. As shown in this figure, f and V_2 of the proposed circuit agree well with the ideal exponential functions. In this theoretical analysis, time t is calculated using the exact expression represented by Σ in (28). On the other hand, since the ideal exponential functions given by (16) and (17) approximate Σ by $\log_e$, the error occurs at startup (when n is small). The theoretical error rates of f and V_2 of the proposed circuit for the ideal exponential functions are almost the same, as small as –0.46 % to –0.92 %.

VIII. Experimental Results and SPICE Simulations

In this section, the results of the theoretical analysis are verified by experiments using a test circuit of Fig. 5 with discrete components. The obtained waveforms are simulated by SPICE. The operational amplifiers (Op2 and Op3) and the comparator (Op4) used in the experiment are LM318N and LM311N, respectively. The CMOS analog switches used are TC4066, and the T-FF is configured using TC4013. First, the limitations of the element values are described as follows.

(a) The value of each capacitor should be greater than a few hundred nF, so that the input capacitance (about 10 pF) of an oscilloscope probe can be sufficiently ignored.

(b) The maximum value of each voltage should be less than the power supply voltage of the CMOS IC. Here, the power supply voltages V_{DD} and V_{SS} are set to the maximum specifications of the used operational amplifiers which are +9 V and–9 V, respectively.

(c) The V_{2max} is set to 7.9 V which is the positive saturation voltage of the operational amplifier Op2.

(d) As shown in Fig. 4, the comparison voltage $-E_r$ of the comparator Op4 is determined the amplitude of the sawtooth wave V_3. The closer E_r is to V_{SS}, the wider the operating range of T_3. However, the delay time of the comparator Op4 is increased when $-E_r$ is close to V_{SS}. Therefore, $-E_r$ is set to –3 V in the test circuit.

(e) Although the operational amplifiers (Op2 and Op3) and the comparator Op4 can operate until hundreds kHz of maximum frequency f_{max}, the distortion of the sawtooth wave V_3 and the delay time of Op4 becomes large. This mainly caused the error rates between the measured results and the theoretical analysis become large. Hence, f_{max} is set to 20 kHz.

Table III. Circuit Parameters Used in Experiment.

Items	Symbol	Values
Capacitor	C_1	0.10 nF
Capacitor	C_2	4.7 nF
Capacitor	C_3	47.8 nF
Resistor	R_3	0.95 kΩ
Step voltage of V_2	ΔV	0.40 V
Comparison voltage	E_r	3.0 V
Minimum voltage of V_2	V_{2min}	0.4 V
Maximum voltage of V_2	V_{2max}	7.9 V
Minimum clock frequency	f_{min}	1 kHz
Maximum clock frequency	f_{max}	20 kHz
Maximum time of t	t_{max}	50 ms

Due to the limitations of the element values described above, the circuit parameters in the theoretical analysis in Table II are changed as shown in Table III of the prototyped circuit. Fig. 7 and Fig. 8 show the measured and simulated waveforms, respectively. When the start clock Φ_0 falls (t=0), V_2 increases exponentially from V_{2min} (=0.4 V) and reaches V_{2max} (=7.9 V) at t= t_{max} (=50 ms). After t=50 ms, the start clock Φ_0 becomes high again and repeats. The amplitude of the sawtooth wave V_3 is E_r(=3 V), and it can be seen that the period of the clock Φ_1 becomes gradually shorter. By zooming at t=0, the clock frequency f {=1/(2T_3)} is 1 kHz (=f_{min}), since the pulse width T_3 of Φ_1 is 0.5 ms. In the same way, by zooming at t=50 ms, f is 20 kHz (=f_{max}), since the pulse width T_3 of Φ_1 is 25 μs.

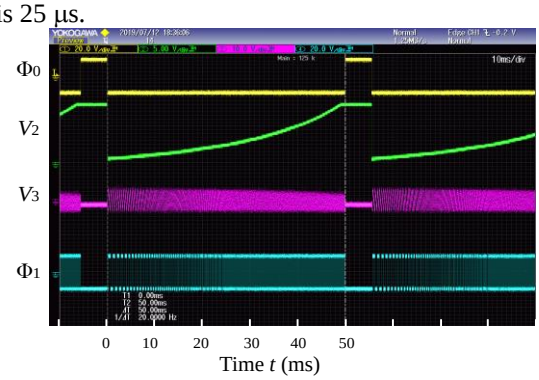

Fig. 7. Measured waveforms.

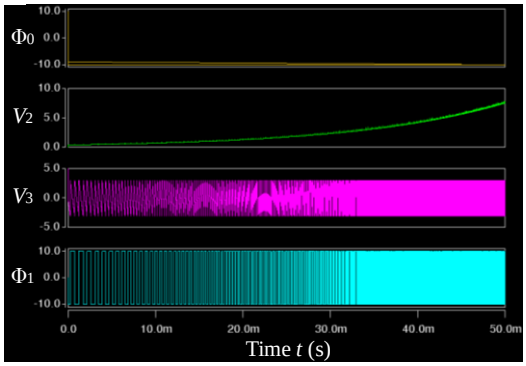

Fig. 8. Simulated waveforms.

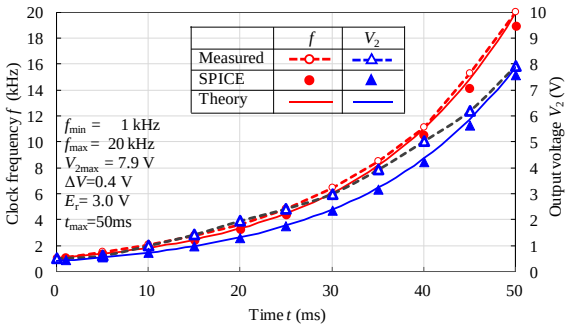

Fig. 9. Comparison of measured and simulated results.

Fig. 9 shows the comparison of the measured and simulated clock frequencies f and the output voltage V_2. From Fig. 9, both the measured and simulated f agree well with theoretical characteristics. Although the simulated V_2 close to the theoretical characteristic, the measured V_2 is larger than the theoretical value. The clock frequency of the test circuit is lower than the

theoretical value, since the on-resistance of each CMOS analog switch is about 100 Ω, and the operational amplifier and comparator have the delay time. In the experiment, ΔV is adjusted so that f_{max} is equal to 20 kHz. Therefore, the measured V_2 is larger than the theoretical value. Near the final time t_{max} (=50 ms) the measured V_2 is closed to the theoretical characteristics since V_{2max} is set to the saturation voltage of the operational amplifier Op2.

IX. An Application of Proposed Circuit

In this section, the charging characteristics of the Cockcroft-Walton (CW) circuit [1] driven by the proposed clock generator is described as an example of the application of the proposed circuit. Fig. 10 shows the circuit configuration of the CW circuit. The switches 1 and 2 are power MOSFETs and constitute a full bridge. The output of the full bridge is a square wave with the amplitude V_{in} and its clock frequency is f. The square wave is rectified by the diodes D_1 ~ D_4, and in a steady state, the capacitor C_{W1} is charged up to V_{in} and C_{W2} ~ C_{W4} are charged up to $2V_{in}$. Therefore, the output voltage V_{out} is $4V_{in}$.

Fig. 11 shows the waveforms of the output voltage V_{out} and the input current I_{in} of the CW circuit driven by the proposed clock and a fixed clock. The circuit parameters of the CW circuit are shown in the figure. From Fig. 11, V_{out} rises rapidly in the case of the fixed clock, but the increasing rate decreases over time. On the other hand, in the case of the proposed clock, it increases slowly and reaches the steady-state value $4V_{in}$ (=564 V) faster than that of the constant clock. At t=0, the input current I_{in} (inrush current) by the proposed clock is reduced to 1/8, and the maximum value of I_{in} is less than half.

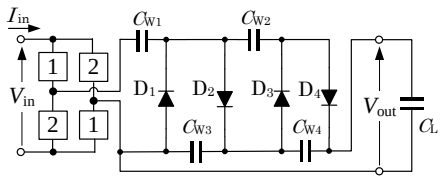

Fig. 10. Two-stage Cockcroft–Walton multiplier.

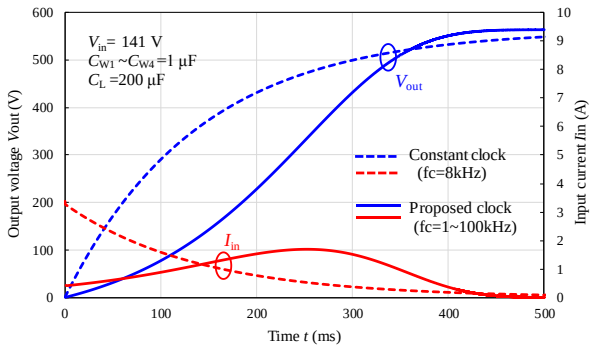

Fig. 11. Output voltage and input current waveforms of CW circuit driven by proposed clock and fixed clock.

X. Conclusions

In this paper, an exponential clock generator has been proposed whose exponent part is positive. The generated clock frequency f and the output voltage V_2 are exponentially increase over time.

The following results are clarified from the theoretical analyses. 1) The theoretical expressions of the generated f and V_2 are derived. 2) The design formulas to determine the circuit parameters with the initial value and the final value are also derived. 3) The theoretical error rates of f and V_2 of the proposed circuit for the ideal exponential functions are almost the same, as small as –0.46 % to –0.92 %.

The following results are obtained by measuring a test circuit and by SPICE simulations. 1) The error between the measured voltage V_2 and the theoretical V_2 slightly increases due to the on-resistances of the analog switches and the delay time of the operational amplifiers. 2) However, the clock frequencies f obtained by the experiment and the SPICE simulation are both close to the theoretical characteristics. 3) In this experiment, the maximum clock frequency f_{max} is reduced to 20 kHz so that the operational amplifiers can operate close to ideal, however it is confirmed that f_{max} can be increased up to several hundreds kHz.

As an application, the Cockcroft-Walton circuit is driven by the proposed clock generator. The charging characteristics is improved so that the inrush current can be reduced to less than 1/8 of that of the fixed clock and the maximum input current is half.

In future, the charging characteristics of the CW circuit driven by the proposed clock generator will be tested and simulated.

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