Clock Generator with Exponentially Increasing Frequency Using Switched-Capacitor Circuit

Aatiqah Aziz\textsuperscript{1}, Shinya Terada\textsuperscript{2}, Kei Eguchi\textsuperscript{3}, and Ichirou Oota\textsuperscript{1}

\textsuperscript{1}Department of Information, Communication and Electronic Engineering, National Institute of Technology, Kumamoto College, Kumamoto 861-1102, Japan
\textsuperscript{2}Department of Control and Information Systems Engineering, National Institute of Technology, Kumamoto College, Kumamoto 861-1102, Japan
\textsuperscript{3}Department of Information Electronic Fukuoka Institute of Technology, Fukuoka 811-0295, Japan

Email: \{terada; oota-i\}@kumamoto-nct.ac.jp; eguti@fit.ac.jp

Abstract—Charging and discharging waveforms in an RC circuit are changed exponentially. The change gradually decreases over time and approaches a steady-state value, since the power of the exponential is negative. However, depending on applications, a diverging signal may be required. In this case, the power of the exponential is positive, and the signal gradually increases over time. In this paper, a clock generator is proposed whose frequency is increased exponentially over time. The proposed circuit can generate exponentially increasing voltage and clock signals with high accuracy over a wide operating range by using Switched-Capacitor (SC) technique. The generated voltage and the clock frequency are derived theoretically. Moreover, the design formulas for finding the circuit parameters with the minimum frequency at startup, small inrush-current, and the maximum frequency at final time. Section VII describes the parameter of the ideal circuit configuration and the operating principle of the proposed circuit. In Section V, the circuit parameters with the minimum frequency at startup, small inrush-current, and the maximum frequency at final time. Section VII describes the parameter of the ideal circuit configuration and the operating principle of the proposed circuit. In Section V, the circuit configuration and the operating principle of the proposed exponential clock generator are described, and the theoretical expressions of the generated voltage and the clock frequency are derived. In Section VI, the theoretical equations are derived for determining the circuit parameters with the minimum frequency at startup, large, the inrush-current becomes large and the charging voltage increases rapidly at startup, but the increasing rate decreases as time passes and finally reaches a steady state value. If the value of the capacitance is large, the inrush-current becomes large and the charging time become longer as well. Usually, the clock frequency of a charge pump circuit is constant.

In this paper, a clock generator is proposed whose frequency is increased exponentially over time. The proposed circuit can generate exponentially increasing voltage and clock signals with high accuracy over a wide operating range by using switched-capacitor (SC) [2]-[15] technique. A conventional method to increase the clock frequency exponentially is as follows. First, a linearly increasing voltage is obtained by a sawtooth wave generator, and the voltage is added to an exponential-gain amplifier to obtain the exponentially increasing voltage [16], [17]. Next, the voltage is applied to a voltage controlled oscillator (VCO) to generate a clock with an exponentially increasing frequency. This method is complicated and has low accuracy, since the exponential voltage generator generates pseudoeXponential voltage by using the nonlinear characteristic of MOSFET or diode.

In order to obtain a high accurate exponential signal, Section II explains a conventional circuit [18] using digital method. In Section III, the proposed VCO and its operation are explained before describing the whole circuit. Section IV describes the parameter of the ideal exponential function to compare with the exponential characteristic of the proposed circuit. In Section V, the circuit configuration and the operating principle of the proposed exponential clock generator are described, and the theoretical expressions of the generated voltage and the clock frequency are derived. In Section VI, the theoretical equations are derived for determining the circuit parameters with the minimum frequency at startup and the maximum frequency at final time. Section VII graphs the theoretical expressions of the generated voltage and the clock frequency, and shows that they almost match the characteristics of the ideal exponential function. In Section VIII, the theoretical characteristics are confirmed by measuring a test circuit and by simulation program with integrated circuit emphasis (SPICE). In Section IX, as an example of the application of the proposed circuit, the charging characteristics of the Cockcroft-Walton circuit [1] driven by the proposed clock generator is described. Finally, the results of this study are summarized in Section X.

II. CONVENTIONAL EXPONENTIAL VOLTAGE GENERATOR

Fig. 1 shows the conventional exponential voltage generator [18] using digital method. This circuit has a wide operating range and is stable and accurate. By the
The minimum step voltage corresponding to the LSB of the D-A converter is \( v_o = V_o + V_{DA} \) (1).

When the output of the counter is \( n \) in decimal and the maximum step voltage corresponding to the LSB of the D-A converter is \( \Delta v \), then \( v_o \) is expressed by

\[
v_o = V_o + n\Delta v
\] (2).

Assuming the coefficient of the V-F converter is \( \alpha \), the output frequency \( f_o \) is \( \alpha v_o \), the \( n \)th-clock frequency \( f_n \) and the clock period \( T_n \) are given as follows, respectively.

\[
f_o = \alpha v_o \\
T_n = f_n = \frac{1}{\alpha (V_o + n\Delta v)}
\] (3) (4).

The waveforms of \( f_o \) and \( v_o \) in Fig. 1 are as shown in Fig. 2. From the figure the time \( t \) is given by

\[
t = \sum_{m=0}^{n} \frac{1}{f_m} = \frac{1}{\alpha \Delta v} \sum_{m=0}^{n} \frac{1}{V_o + m\Delta v}
\] (5).

The above equation can be approximated as follows if \( n \) is sufficiently large.

\[
t = \frac{1}{\alpha \Delta v} \ln \left( \frac{V_o + n\Delta v}{V_o} \right) = \frac{1}{\alpha \Delta v} \ln \left( \frac{v_o}{V_o} \right)
\] (6).

Therefore, the voltage \( v_o \) and the output frequency \( f_o \) are increased exponentially, given in (7) and (8).

The powers of the exponential are positive.

\[
v_o \approx V_o e^{\alpha \Delta v t}
\] (7).

\[
f_o = \alpha v_o \approx \alpha V_o e^{\alpha \Delta v t}
\] (8).

III. PROPOSED VCO

In this Section, the circuit configuration and its operation of the proposed VCO (voltage controlled oscillator) will be explained, before describing the whole circuit. Fig. 3 and Fig. 4 show the circuit configuration and the waveforms of the proposed VCO, respectively. The squared symbols 1 and 2 in Fig. 3 are CMOS analog switches, they are turned on during the clocks \( \Phi_1 \) and \( \Phi_2 \) are in a high level “H”, respectively. The input voltage \( V_2 \) is a positive DC voltage. Since the initial charge of the capacitor \( C_3 \) is 0 at \( t=0 \), the output voltage \( V_3 \) of the operational amplifier Op3 is 0, and the output voltage \( V_4 \) of the comparator Op4 is saturated at \( V_{SS} \). When the inputs \( \Phi_1 \) and \( \Phi_2 \) of the T-FF are “H” and “L” respectively, the switch 1 is turned on and the switch 2 is turned off. Thus, \( V_3 \) is

\[
V_3 = -\frac{V_2}{C_3R_1}t
\] (9).

As shown in Fig. 4, \( V_3 \) decreases linearly. When \( V_3 \) falls below \(-E_4\), \( V_4 \) saturates at \( V_{DD} \), and the output clocks \( \Phi_1 \) and \( \Phi_2 \) are inverted. At this timing, since the capacitor \( C_3 \) is connected in the reverse direction, the voltage \( V_3 \) drops linearly from \(+E_4\), and the above operation is repeated.

From Fig. 4 pulse width \( T_3 \) is determined as

\[
T_3 = \frac{2C_3R_1E_4}{V_2}
\] (10).

Therefore, the clock frequency \( f \) of VCO is proportional to the input voltage \( V_2 \) as follows:

\[
f = \frac{1}{2T_3} = \frac{1}{4C_3R_1E_4}V_2
\] (11).

Fig. 1. Conventional exponential voltage generator.

Fig. 2. Waveforms in Fig. 1.

Fig. 3. Proposed VCO.

Fig. 4. Waveforms in VCO of Fig. 3.
When \( V_2 = V_{2\text{min}} \) and \( V_{2\text{max}} \), \( f = f_{\text{min}} \) and \( f_{\text{max}} \), respectively, then,

\[
f_{\text{min}} = \frac{1}{4CR_1E_1} V_{2\text{min}}
\]

\[
f_{\text{max}} = \frac{1}{4CR_1E_1} V_{2\text{max}}
\]

From the above equations, \( R_1 \) and \( V_{2\text{min}} \) are determined as follows.

\[
R_1 = \frac{V_{2\text{max}}}{4C_1E_1 f_{\text{max}}}
\]

\[
V_{2\text{min}} = \frac{f_{\text{min}}}{f_{\text{max}}} V_{2\text{max}}
\]

Here, \( V_{2\text{min}} \) cannot be arbitrarily selected from the above equation, however, there is no problem in the case of using only the exponential clock \( f \). The resistor \( R_1 \) can be replaced by an SC resistor. In this case, the circuit can be configured completely by SC.

IV. SPECIFICATIONS FOR IDEAL EXPONENTIAL SIGNAL

In this section, the ideal circuit parameters for designing an exponential signal are described. Table I shows the specifications of the exponential signal to be designed. In this table, the values of black character are given, and the red ones are calculated using the equations of the right column in the table. Assuming that the output clock frequency \( f(t) \) and the output voltage \( V_2(t) \) are \( f_{\text{min}} \) and \( V_{2\text{min}} \) at \( t=0 \), respectively, and the time constants of the frequency and the voltage are \( \tau_f \) and \( \tau_v \), then the both are expressed as

\[
f(t) = f_{\text{min}} e^{\frac{t}{\tau_f}}
\]

\[
V_2(t) = V_{2\text{min}} e^{\frac{t}{\tau_v}}
\]

Since \( f(t) \) and \( V_2(t) \) are exponentially increased, and they reach \( f_{\text{max}} \) and \( V_{2\text{max}} \) at \( t=t_{\text{max}} \), respectively, the time constants \( \tau_f \) of the frequency is given by

\[
f_{\text{max}} = f_{\text{min}} e^{\frac{\tau_{\text{max}}}{\tau_f}}
\]

\[
\tau_f = \frac{\tau_{\text{max}}}{\ln \left( \frac{f_{\text{max}}}{f_{\text{min}}} \right)}
\]

In the same way the time constant \( \tau_v \) of the voltage is

\[
V_{2\text{max}} = V_{2\text{min}} e^{\frac{\tau_{\text{max}}}{\tau_v}}
\]

\[
\tau_v = \frac{\tau_{\text{max}}}{\ln \left( \frac{V_{2\text{max}}}{V_{2\text{min}}} \right)}
\]

V. PROPOSED EXPONENTIAL CLOCK GENERATOR

Fig. 5 shows the circuit configuration of the proposed clock generator. In Fig. 5, the voltage \( V_1 \) is a small negative DC voltage \( -AV \). The upper half of the figure is SC integrator, and the lower half is the proposed VCO in Fig. 3. If the initial voltages of all capacitors \( C_1 \sim C_3 \) at \( t=0 \) are 0, \( V_2 \) and \( V_1 \) are always 0 and the clocks \( \Phi_1 \) and \( \Phi_2 \) do not start. Thus, to start the clocks, the DC voltage \( V_{2\text{min}} \) and the clock \( \Phi_0 \) are added to the circuit. As shown in Fig. 5, when \( t<0 \), \( \Phi_0 \) is "0" and at \( t=0 \), \( \Phi_0 \) changes "1". Therefore, at \( t=0 \) the initial voltage of \( C_3 \) is set to \( V_{2\text{min}} \).

In the upper half of the circuit, when the switch \( \Phi_1 \) is turned on, \( C_1 \) is charged up to \( V_1 = - AV \). When the switch \( \Phi_2 \) is turned on, \( C_1 \) is discharged, and all charge of \( C_1 \) move to \( C_2 \), since the inverting input terminal of the operational amplifier Op2 is virtually grounded. Therefore, at \( t=T \) the final \( V_2 \) in the first cycle of the clock is given by

\[
V_2 \left( t = T^- \right) = \frac{(C_2 V_{2\text{min}} + C_1 AV)}{C_2} = V_{2\text{min}} + \frac{C_1}{C_2} AV
\]

In the same way, during next cycle, the all charge \( AV \) of \( C_1 \) is moved to \( C_2 \). Therefore,

\[
V_2 \left( t = 2T^- \right) = \frac{(C_2 V_{2\text{min}} + 2C_1 AV)}{C_2} = V_{2\text{min}} + 2 \frac{C_1}{C_2} AV
\]

The above steps are repeated, and \( V_2 \) in the \( n \)-th cycle is

\[
V_2 \left( t = nT^- \right) = V_{2\text{min}} + n \frac{C_1}{C_2} AV
\]
The lower half of Fig. 5 during \( t > 0 \) is the same as the VCO of Fig. 3. From (11), the clock frequency \( f_n \) of the \( n \)-th cycle is
\[
f_n = \frac{1}{4C_3R_3E_r} V_2(t = nT) \tag{25}
\]
From (24) and (25), the clock cycle \( T_n \) of the \( n \)-th cycle is
\[
T_n = \frac{1}{f_n} = \frac{4C_3R_3E_r}{V_{2\text{min}} + nC_1\Delta V} \tag{26}
\]
Therefore, the time \( t \) is expressed as follows by adding the period \( T_n \) of the above equation:
\[
t = \sum_{m=0}^{n} T_n = 4C_3R_3E_r \left( \frac{1}{V_{2\text{min}}} + \frac{C_1\Delta V}{C_2V_{2\text{min}}} n \right) \tag{27}
\]
From (24),
\[
t \approx 4C_3C_4C_5R_5E_5 \left( \frac{1}{C_4V_{2\text{min}}} \right) V_{2\text{min}}(t) \tag{30}
\]
From the above equation, \( V_2(t) \) is obtained as follows:
\[
V_2(t) \approx V_{2\text{min}} e^{\frac{C_1\Delta V}{C_2V_{2\text{min}}} t} \tag{31}
\]
where the voltage time constant \( \tau \) is
\[
\tau = 4C_3C_4C_5R_5E_5 \left( \frac{1}{C_4V_{2\text{min}}} \right) \tag{32}
\]
Substituting (31) into (11), the clock frequency \( f \) is given by
\[
f = \frac{1}{4C_3R_3E_r} \frac{C_1\Delta V}{4C_3C_4C_5R_5E_5} = f_{\text{max}} e^{-\frac{t}{\tau}} \tag{33}
\]
where
\[
f_{\text{max}} = \frac{1}{4C_3R_3E_r} \tag{34}
\]
The time constants of the voltage and the frequency are the same and cannot be set independently, however, there is no problem in the case of using only the exponential clock.

VI. METHOD OF DETERMINING ELEMENT VALUE OF PROPOSED CIRCUIT

In this section, the method of determining the circuit parameter is described from the circuit operation and the theoretical analysis described above. Table II shows examples of the circuit parameters of Fig. 5. In Table II, the values of the black character are given, and the red ones are calculated using the equations of the right column in the table.

Assuming that \( t = t_{\text{max}} \) at the \( n_{\text{max}} \)-th clock, from (24), \( V_{2\text{max}} \) is
\[
V_{2\text{max}} = V_{2\text{min}} + n_{\text{max}} \frac{C_1}{C_2} \Delta V \tag{35}
\]
Then, the capacitor \( C_1 \) is
\[
C_1 \approx \frac{V_{2\text{max}} - V_{2\text{min}}}{n_{\text{max}} \Delta V} \tag{36}
\]
The time constant \( \tau \) in (32) is determined to match (21) of the ideal exponential function, then \( \tau \) is
\[
\tau = \frac{4C_3C_4C_5R_5E_5}{C_1\Delta V} = \ln\left(\frac{t_{\text{max}}}{t_{\text{max}}/f_{\text{max}}} \right) \tag{37}
\]
From (36) and (37), \( n_{\text{max}} \) is given by
\[
n_{\text{max}} = \frac{V_{2\text{max}} - V_{2\text{min}}}{4C_3R_3E_r} \tau \tag{38}
\]

| Table II. Determination of Proposed Circuit Parameters |
|---|---|---|---|
| Item | Symbol | Values* | Eq. |
| Capacitor | \( C_1 \) | 0.01 nF | (36) |
| Capacitor | \( C_2 \) | 1.0 nF | | |
| Capacitor | \( C_3 \) | 2.0 nF | | |
| Resistor | \( R_1 \) | 1.25 k\( \Omega \) | (14) |
| Step voltage of \( V_2 \) | \( \Delta V \) | 0.10 V | | |
| Comparison voltage | \( E_r \) | 10.0 V | | |
| Minimum voltage of \( V_2 \) | \( V_{2\text{min}} \) | 0.10 V | (15) |
| Maximum voltage of \( V_2 \) | \( V_{2\text{max}} \) | 10.0 V | | |
| Minimum clock frequency | \( f_{\text{min}} \) | 1 kHz | | |
| Maximum clock frequency | \( f_{\text{max}} \) | 100 kHz | | |
| Maximum time of \( t \) | \( t_{\text{max}} \) | 0.50 s | | |
| Number of clock iterations at \( t = t_{\text{max}} \) | \( n_{\text{max}} \) | 10.749 | (38) |
| Time constant | \( \tau \) | 0.109 s | (19) |

*The red values are calculated by equations of the right column.

VII. CHARACTERISTICS ANALYSIS OF PROPOSED CIRCUIT

From the above results, the characteristics of the proposed circuit are obtained by using the parameters in Table II. Without using (29) in the approximation of \( \log \) the period \( T_n \) of each state is calculated by (26) and the

Fig. 6. Time change of clock frequency \( f \) and output voltage \( V_2 \).
time \( t \) is exactly calculated by adding of (27). Fig. 6 show the changes of \( f \) and \( V_2 \) from \( t = 0 \) to \( t_{\text{max}}=0.5 \text{ s} \). As shown in this figure, \( f \) and \( V_2 \) of the proposed circuit agree well with the ideal exponential functions. In this theoretical analysis, time \( t \) is calculated using the exact expression represented by \( \Sigma \) in (28). On the other hand, since the ideal exponential functions given by (16) and (17) approximate \( \Sigma \) by \( \log_e \), the error occurs at startup (when \( n \) is small). The theoretical error rates of \( f \) and \( V_2 \) of the proposed circuit for the ideal exponential functions are almost the same, as small as \(-0.46 \% \) to \(-0.92 \% \).

VIII. EXPERIMENTAL RESULTS AND SPICE SIMULATIONS

In this section, the results of the theoretical analysis are verified by experiments using a test circuit of Fig. 5 with discrete components. The obtained waveforms are simulated by SPICE. The operational amplifiers (Op2 and Op3) and the comparator (Op4) used in the experiment are LM318N and LM311N, respectively. The CMOS analog switches used are TC4066, and the T-FF is configured using TC4013. First, the limitations of the element values are described as follows.

(a) The value of each capacitor should be greater than a few hundred nF, so that the input capacitance (about 10 pF) of an oscilloscope probe can be sufficiently ignored.

(b) The maximum value of each voltage should be less than the power supply voltage of the CMOS IC. Here, the power supply voltages \( V_{\text{DD}} \) and \( V_{\text{SS}} \) are set to the maximum specifications of the used operational amplifiers which are \(+9 \text{ V} \) and \(-9 \text{ V} \), respectively.

(c) The \( V_{\text{SS}} \) is set to 7.9 V which is the positive saturation voltage of the operational amplifier Op2.

(d) As shown in Fig. 4, the comparison voltage \(-E_c\) of the comparator Op4 is determined the amplitude of the sawtooth wave \( V_3 \). The closer \( E_c \) is to \( V_{\text{SS}} \), the wider the operating range of \( T_3 \). However, the delay time of the comparator Op4 is increased when \(-E_c\) is close to \( V_{\text{SS}} \). Therefore, \(-E_c\) is set to \(-3 \text{ V} \) in the test circuit.

(e) Although the operational amplifiers (Op2 and Op3) and the comparator Op4 can operate until hundreds kHz of maximum frequency \( f_{\text{max}} \), the distortion of the sawtooth wave \( V_3 \) and the delay time of Op4 becomes large. This mainly caused the error rates between the measured results and the theoretical analysis become large. Hence, \( f_{\text{max}} \) is set to 20 kHz.

<table>
<thead>
<tr>
<th>TABLE III. CIRCUIT PARAMETERS USED IN EXPERIMENT.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Items</strong></td>
</tr>
<tr>
<td>Capacitor</td>
</tr>
<tr>
<td>Capacitor</td>
</tr>
<tr>
<td>Capacitor</td>
</tr>
<tr>
<td>Resistor</td>
</tr>
<tr>
<td>Step voltage of ( V_1 )</td>
</tr>
<tr>
<td>Comparison voltage</td>
</tr>
<tr>
<td>Minimum voltage of ( V_2 )</td>
</tr>
<tr>
<td>Maximum voltage of ( V_2 )</td>
</tr>
<tr>
<td>Minimum clock frequency</td>
</tr>
<tr>
<td>Maximum clock frequency</td>
</tr>
<tr>
<td>Maximum time of ( t )</td>
</tr>
</tbody>
</table>

Due to the limitations of the element values described above, the circuit parameters in the theoretical analysis in Table II are changed as shown in Table III of the prototyped circuit. Fig. 7 and Fig. 8 show the measured and simulated waveforms, respectively. When the start clock \( \Phi_0 \) falls (\( t=0 \)), \( V_2 \) increases exponentially from \( V_{2\text{min}} \) (=0.4 V) and reaches \( V_{2\text{max}} \) (=7.9 V) at \( t = t_{\text{max}} \) (=50 ms). After \( t=50 \text{ ms} \), the start clock \( \Phi_0 \) becomes high again and repeats. The amplitude of the sawtooth wave \( V_3 \) is \( E_c (=3 \text{ V}) \), and it can be seen that the period of the clock \( \Phi_1 \) becomes gradually shorter. By zooming at \( t=0 \), the clock frequency \( f (=1/(2\pi T_3)) \) is 1 kHz (\( \approx f_{\text{min}} \)), since the pulse width \( T_3 \) of \( \Phi_1 \) is 0.5 ms. In the same way, by zooming at \( t=50 \text{ ms} \), \( f \) is 20 kHz (\( \approx f_{\text{max}} \)), since the pulse width \( T_3 \) of \( \Phi_1 \) is 25 ms.

![Fig. 7. Measured waveforms.](image)

![Fig. 8. Simulated waveforms.](image)

![Fig. 9. Comparison of measured and simulated results.](image)

Fig. 9 shows the comparison of the measured and simulated clock frequencies \( f \) and the output voltage \( V_2 \). From Fig. 9, both the measured and simulated \( f \) agree well with theoretical characteristics. Although the simulated \( V_2 \) close to the theoretical characteristic, the measured \( V_2 \) is larger than the theoretical value. The clock frequency of the test circuit is lower than the
theoretical value, since the on-resistance of each CMOS analog switch is about 100 Ω, and the operational amplifier and comparator have the delay time. In the experiment, ΔV is adjusted so that $f_{\text{max}}$ is equal to 20 kHz. Therefore, the measured $V_2$ is larger than the theoretical value. Near the final time $t_{\text{max}} (=50 \text{ ms})$ the measured $V_2$ is closed to the theoretical characteristics since $V_{2\text{max}}$ is set to the saturation voltage of the operational amplifier Op2.

IX. AN APPLICATION OF PROPOSED CIRCUIT

In this section, the charging characteristics of the Cockcroft-Walton (CW) circuit [1] driven by the proposed clock generator is described as an example of the application of the proposed circuit. Fig. 10 shows the circuit configuration of the CW circuit. The switches [1] and [2] are power MOSFETs and constitute a full bridge. The output of the full bridge is a square wave with the amplitude $V_{\text{in}}$ and its clock frequency is $f$. The square wave is rectified by the diodes D1 ~ D4, and in a steady state, the capacitor $C_{W1}$ is charged up to $V_{\text{in}}$ and $C_{W2} ~ C_{W4}$ are charged up to 2$V_{\text{in}}$. Therefore, the output voltage $V_{\text{out}}$ is 4$V_{\text{in}}$.

Fig. 11 shows the waveforms of the output voltage $V_{\text{out}}$ and the input current $I_{\text{in}}$ of the CW circuit driven by the proposed clock and a fixed clock. The circuit parameters of the CW circuit are shown in the figure. From Fig. 11, $V_{\text{out}}$ rises rapidly in the case of the fixed clock, but the increasing rate decreases over time. On the other hand, in the case of the proposed clock, it increases slowly and reaches the steady-state value 4$V_{\text{in}}$ (=564 V) faster than that of the constant clock. At $t=0$, the input current $I_{\text{in}}$ (inrush current) by the proposed clock is reduced to 1/8, and the maximum value of $I_{\text{in}}$ is less than half.

![Fig. 10. Two-stage Cockcroft-Walton multiplier.](image)

![Fig. 11. Output voltage and input current waveforms of CW circuit driven by proposed clock and fixed clock.](image)

X. CONCLUSIONS

In this paper, an exponential clock generator has been proposed whose exponent part is positive. The generated clock frequency $f$ and the output voltage $V_2$ are exponentially increase over time.

The following results are clarified from the theoretical analyses. 1) The theoretical expressions of the generated $f$ and $V_2$ are derived. 2) The design formulas to determine the circuit parameters with the initial value and the final value are also derived. 3) The theoretical error rates of $f$ and $V_2$ of the proposed circuit for the ideal exponential functions are almost the same, as small as $-0.46\%$ to $-0.92\%$.

The following results are obtained by measuring a test circuit and by SPICE simulations. 1) The error between the measured voltage $V_2$ and the theoretical $V_2$ slightly increases due to the on-resistances of the analog switches and the delay time of the operational amplifiers. 2) However, the clock frequencies $f$ obtained by the experiment and the SPICE simulation are both close to the theoretical characteristics. 3) In this experiment, the maximum clock frequency $f_{\text{max}}$ is reduced to 20 kHz so that the operational amplifiers can operate close to ideal, however it is confirmed that $f_{\text{max}}$ can be increased up to several hundreds kHz.

As an application, the Cockcroft-Walton circuit is driven by the proposed clock generator. The charging characteristics is improved so that the inrush current can be reduced to less than 1/8 of that of the fixed clock and the maximum input current is half.

In future, the charging characteristics of the CW circuit driven by the proposed clock generator will be tested and simulated.

ACKNOWLEDGMENT

The authors would like to thank Miss Ten Min Yang for helping the SPICE simulations. This work is supported by VLSI Design and Education Center (VDEC), The University of Tokyo with the collaboration with Synopsys Corporation.

REFERENCES

power applications,” WSEAS Trans. on Circuits and Systems, vol. 6, no. 9, pp. 545-552, Sept. 2007.


