Performance Analysis of High-k Dielectric Based Silicon Nanowire Gate-All-Around Tunneling FET

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***Abstract*—The Tunnel Field Effect Transistors (TFETs) are used as a promising candidate in low power applications at the nanometer scale primarily because the conventional Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) approaches the physical and thermal limits. In this research work, a TFET device with cylindrical gate-all-around structure (Si-nanowire as channel and HfO_2 as a high-k dielectric gate oxide) has been designed and simulated for the analyzing short channel effects. First, the effect of variation in channel lengths (100 nm to 180 nm) of the TFET is analyzed. Further, the gate oxide thickness variations in the ranging 3 nm to 6.5 nm at different channel length are presented. As a result, the device displays Drain Induced Barrier Lowering (DIBL) as low as of 7.1 mV/V to 10.26 mV/V, low Subthreshold Swing (SS) in the range of 19.91 mV/decade to 34.36 mV/decade and a reasonable current ratio (I_{ON}/I_{OFF}) in the ranges of 2.9×10^6 to 7.8×10^9 which suggest the usability of the device in ultra-low power switching applications.**

***Index Terms*—Band-to-band tunneling, GAA structure, nanotechnology, Si-nanowire, tunnel FET, VLSI**

I. Introduction

As the dimensions of the transistor are shrinking below 100 nm researches are very actively pointing towards nanometers regime, where the scaling makes it possible to package millions of transistors in a single chip following Moore's Law [1], [2]. However, the essential physical limitation of bulk metal-oxide-semiconductor field effect transistors (MOSFETs) to scale them in the submicron region is the adherence to strong Short Channel Effects (SCEs). ITRS reports that the Complementary Metal-Oxide-Semiconductor (CMOS) transistor technology enhancements are extensively widening the nano-scale design and operation primarily for the faster switching and lower power applications [3].

This rapid growth in downscaling of semiconductor device into the nano-regime is leading the short channel effects as the very severe problem such as increasing Drain Induced Barrier Lowering (DIBL) and leakage currents. In the last decade, various research has been done to find the alternative device channel and gate structures for pursuing improvements. Subsequently, device structures such as double-gate (DG), Surrounding-Gate (SG), Cylindrical Gate-All-Around (CGAA), cylindrical-surrounding double-gate, carbon nanotube (CNT), FinFETs and Graphene-Nano-Ribbon (GNR) transistors have been instigated for resolving the scaling issues of conventional transistors [4]-[9].

The silicon nanowire is among one of those structures that exhibit excellent gate control and highly influenced electrical behavior of Bulk-MOSFETs. In the past few years, various approaches utilizing nanowires as a channel with surrounding gate structures for different applications of switching [10]-[12] were reported. The voltage required to change the drain current by decade is specified by the term Subthreshold Swing (SS) and relates to the faster switching performance when the transistor operates in the sub-threshold region at low voltage. In MOSFET switching device [13], the sub-threshold swing is expressed as

$$\underbrace{\frac{dV_g}{d\psi_S}}_{m}\underbrace{\frac{d\psi_S}{d(\log I_d)}}_{n} \cong \left(1+\frac{C_d}{C_{ox}}\ln\frac{kT}{q}\right) \quad (1)$$

where V_g, I_d, and ψ_s are the gate voltage, drain voltage, and surface potential, respectively, and C_d and C_{ox} are the drain and oxide capacitance, respectively with

$$\ln\frac{kT}{q} \equiv 60 \text{ mV/decade}$$

To achieve a low subthreshold swing, reduced n is desirable for modifying the carrier-injection mechanism, but the MOSFET suffers from thermal limitation. Therefore, the Tunnel Field Effect Transistors (TFETs) have been introduced as a substitution of thermally limited MOSFETs in the technology nodes. The device gained more popularity since the quantum-mechanical band-to-band tunneling in TFET could give subthreshold slope value ≤ 60 mV/decade at threshold voltage below 1 V [14].

The structural similarity followed in TFETs from a MOSFET makes it suitable to fabricate with the standard CMOS processing techniques for implementations. Also, the capability of TFET in obtaining low OFF currents and reducing device leakage is another advantage for ultralow power applications [15]-[21].

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The Gate-All-Around (GAA) TFET with better electrostatic control, protection to the short channel effects [22], [23], and faithful sub-threshold have been proclaimed as a decent alternative to MOSFETs at reduced nanometer scales. However, the ON current of the device has been relatively low which results in low speed of switching and undergoes delayed saturation for analog applications [24]. Also, often the TFETs are affected by severe drain-induced barrier lowering and other technical distresses such as substantial contact area and high series resistance restraining them for ultra-low scale integration [24], [25]. The cylindrical geometry of the structure can help in obtaining higher ON current per unit area in comparison to a planar structure, and reasonable ON-OFF current ratio (I_{ON}/I_{OFF}) can be obtained using high-*k* dielectric gate oxide.

In this work, a cylindrical Si-nanowire gate-all-around (CSNWGAA) tunneling field effect transistor has been designed using Hafnium Oxide (HfO_2) as gate dielectric material. The designed TFET structure has been simulated with various channel lengths and thickness of gate-oxide to analyze the effects on the device electrical parameters. This paper is organized as follows. The structural description of the device given in Section II. Section III describes the simulation methodology of the proposed device. Section IV provides the simulated device results and discuss the obtained result. Finally, conclusion and future scope of the work is presented in Section V.

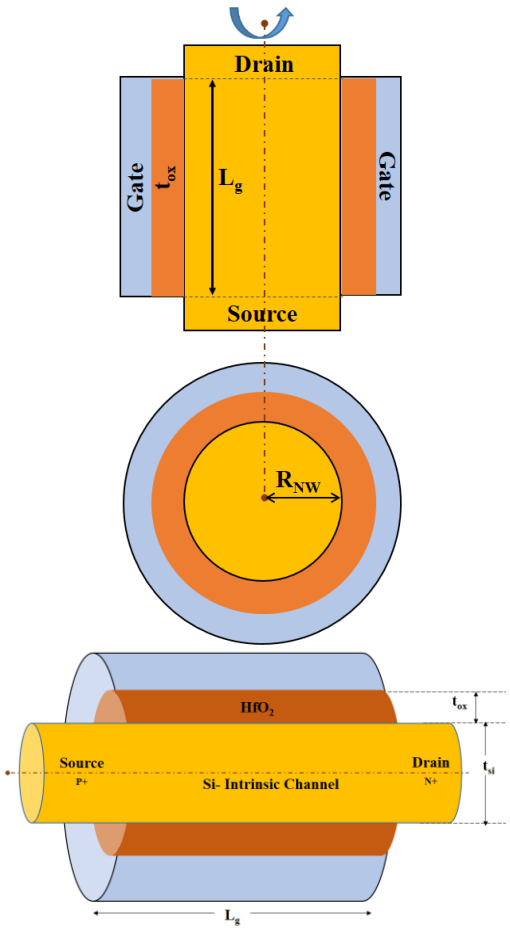


Fig. 1. Schematic of CSNWGAA TFET.

II. Device Structure

The CSNWGAA-TFET is a P-I-N structure in which an intrinsic semiconducting part is sandwiched between heavily doped source and the drain. By using band energy bending, gate all around controls the tunneling between the channel and the doped P+ and N+ regions.

Fig. 1 shows a cross-sectional schematic illustration of the geometric structure of the device. The silicon channel thickness is t_{si} for the gate length L_g with acceptors dopant concentration (10^{14} per cm^3) and donors dopant concentration (10^{18} per cm^3). We have used gate oxide thickness (t_{ox} =5 nm), and gate length (L_g =100 nm). The device simulation structure with the underlying physics in connection with the tunneling phenomena proposed by Kane [26] and the non-local BTBT tunneling model are explained in the subsequent section.

III. Device Simulation

A. Structure Design

The device has been structured using the electronic simulator in the scales of dimension specified. After that, the contacts are set, and the constant doping profile has been selected of 1E+18 and 1E+14 for the source and the drain, respectively. Fig. 2. shows the three-dimensional structure after the successful meshing of the device. The generation and recombination rates of the device are modeled using band-to-band tunneling current. Both the processes compute the probability of tunneling in the simulator as a variation of Kane or Keldysh's equation and further analyze the subsequent meshed structure.

The different models make use a different analysis of the band structure because it significantly affects the amount and region of the predicted tunnel current. Simulators have two models, namely local and non-local tunnel model. The non-local tunneling model has been used in the designed TFET which keeps subthreshold slope up to 60mV/decade. The model is bound to the quantum-mechanical tunneling of the electrons from source to the channel using carrier transport mechanism.

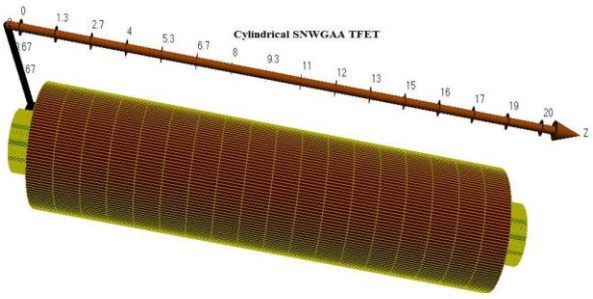


Fig. 2. 3D Mesh structure of the device.

B. Non Local Tunneling Model

The tunneling is the process of transfer electron or hole crossing the junction. The tunneling causes pairs of electrons and holes; hence the electron and hole transfer rates are opposite and equal [15]. The model is based on Landauer's equation. The primary default parameters of the model are listed in Table I.

TABLE I. NON-LOCAL-BTBT PARAMETERS

Constraint	Default value
MC	0.16
MV	0.24
METUNNEL	0.16
MHTUNNEL	0.24

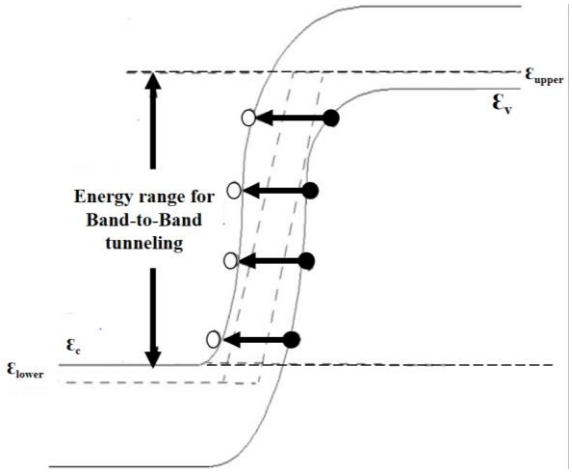


Fig. 3. Representation of non-local band-to-band tunneling (Atlas, 2014).

The values specified for conduction and valence band effective masses MC or MV are used only when the METUNNEL or MHTUNNEL are not defined. The METUNNEL and MHTUNNEL are the effective mass of electron and hole calculated from two band tunneling model.

As the tunneling is a process involving electron crossing the junction, the net current per unit area for an electron with longitudinal energy ε and transverse energy ε_t [27], can be written as

$$J(\varepsilon) = \frac{e}{\pi h}\iint P_t(\varepsilon)\left[\left\{ f_{\text{long}}(\varepsilon+\varepsilon_t) - f_{\text{trans}}(\varepsilon+\varepsilon_t)\right\}\rho(\varepsilon_t)\right] d\varepsilon d\varepsilon_t \quad (2)$$

where $P_t(\varepsilon)$ is the probability of tunneling of an electron with longitudinal energy ε, $\rho(\varepsilon_t)$ belongs to the two-dimensional density of state corresponding to the transverse wave vectors, f_{trans} and f_{long} are the quasi fermi-level of Fermi-Dirac-distribution function in the left and right side of the junction. The tunneling probability, $P_t(\varepsilon)$ is determined by the Wentzel-Kramers-Brillouin method [28]:

$$P_t(\varepsilon) = \exp\left[-2\int_{x_2}^{x_1}\kappa(x)dx\right] \quad (3)$$

The starting and ending points of the tunneling route can be referred to as x_1 and x_2 respectively, which are governed by the energy as shown in Fig. 3. The simulator calculates evanescent wave-vector at points in between from (4).

$$k(x) = \frac{k_e(x)k_h(x)}{\sqrt{k_e^{\,2}(x)+k_h^{\,2}(x)}} \quad (4)$$

where

$$\kappa_e(x) = \frac{1}{jh}\sqrt{2m_0 m_e(\varepsilon - \varepsilon_c)}$$

$$\kappa_h(x) = \frac{1}{jh}\sqrt{2m_0 m_e(\varepsilon_v - \varepsilon)}$$

h is the Planck's constant, m_0 is the mass at resting of an electron, m_e/m_h is the effective mass of the electron or holes, and $\varepsilon_c/\varepsilon_v$ is the conduction or valence band energy. The tunneling current density at given longitudinal energy can be obtained by substituting these values in (2). The resultant current is injected into the simulation at x_1 and x_2 and iterated for every tunnel slice in the regions for energy level between $\varepsilon_{\text{lower}}$ and $\varepsilon_{\text{upper}}$. The field lines of non-local band-to-band tunneling of the simulated device are shown in Fig. 4.

In the band-tunneling model, tunneling current depends on the edge profiling along the entire path between the concentrations which suggests the field developing progressively at all the points in the tunnel and makes the tunneling a non-neighborhood. The net gap recombination rate for band-to-band tunneling by the electric field is shown in Fig. 4.

When the positive gate voltage is applied, the dominant mode at the gate-source junction is band-to-band tunneling (BTBT). The non-local band to band electron energy rates at the ON and OFF states are shown Fig. 4. For this structured device, BTBT generation rate increases when the device is ON and finds its maximum value at the source channel junction.

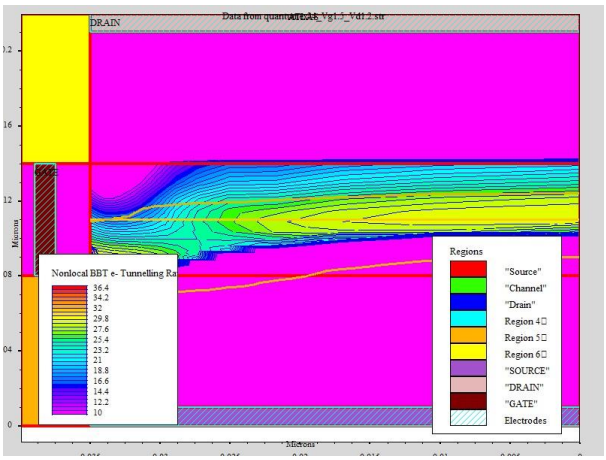
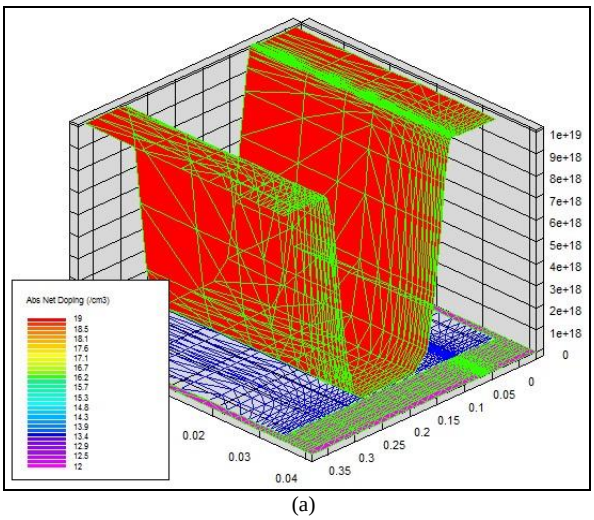
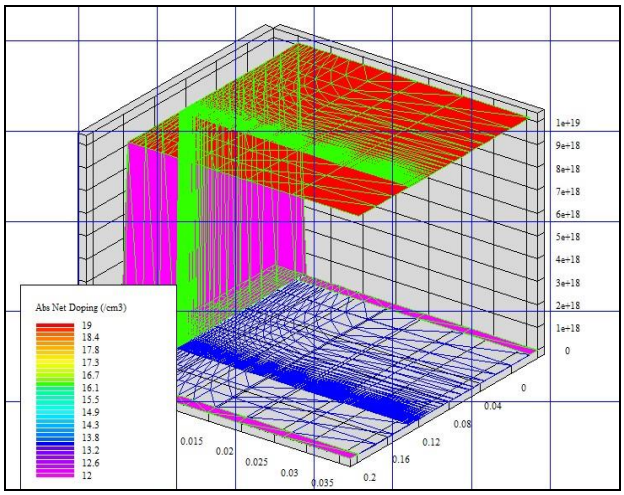


Fig. 4. Non-local BTBT electron tunneling rate in the device.



(a)



(b)

Fig. 5. (a) Doping profile (b) Contour (color plotting) of the structure.

Knowing the current mechanisms in the device makes it easier to understand the changes in performance based on variations in devices parameters. Fig. 5 (a) and (b) illustrate the electron distribution function trends concerning changes in the gate as a contour of visualized data in structure meshes and drain fields, respectively.

Both the contour plots and fringe plots are obtained with material naming and range control to limit the plot in a restricted subset of the data [29], [30].

IV. Results and Discussions

The current-voltage characteristics of the CSNWGAA TFET are obtained as results of the simulation of the device. DIBL and SS are the measures of performance of different devices.

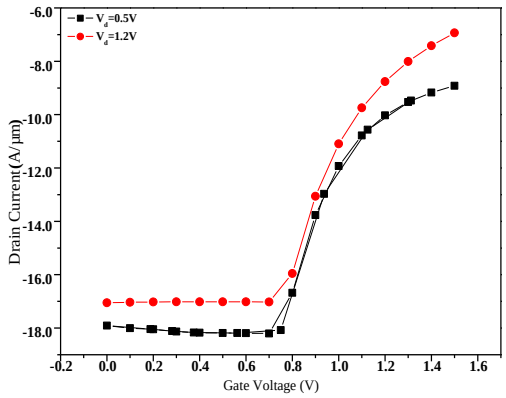


Fig. 6. I_d-V_g characteristics of CSNWGAA-TFET with gate length (L_g = 100 nm) and (t_{ox} = 5 nm).

The transfer characteristics (I_d-V_g) and drain characteristics (I_d-V_d) of the device are illustrated in Fig. 6 and Fig. 7 obtained at fixed gate length (L_g) and oxide thickness of 100 nm and 5 nm, respectively.

The drain characteristics of the simulated device are taken at increasing step gate voltage of 0.05 V, 0.3 V, and 0.8 V, respectively, as shown in Fig. 7. The subthreshold swing refers to the rate of increment in current with the applied gate voltage below its threshold, expressed in mV of the gate voltage for decibel rise of the drain current and a MOSFET defined as (5) [31]-[33].

$$\text{Subthreshold slope} = \frac{dV_G}{d(\log_{10} I_d)} \tag{5}$$

The body factor is known as the gate control efficiency on the channel potential which is equal to 1, at room temperature 300K) which makes to the value of SS=60 mV/decade. The gate does not just control the channel potential; it also depends on the length of the source to drain regions along with V_{ds} voltage.

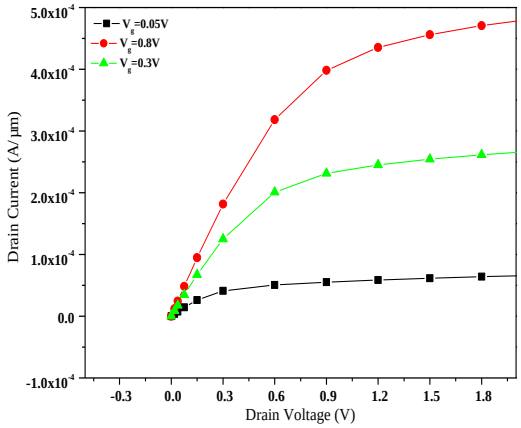


Fig. 7. I_d-V_d characteristics of CSNWGAA-TFET with gate length (L_g = 100 nm) and (t_{ox} = 5 nm).

An ultra-scaled CSNWGAA TFET has the value of DIBL [34] as shown in (6).

$$\frac{V_T\big|V_{ds=0.1\text{V}} - V_T\big|V_{ds=0.5\text{V}}}{0.5-0.1} \tag{6}$$

For analyzing the device performance DIBL, SS, and I_{ON}/I_{OFF} parameters have been extracted from the *I-V* characteristics of the simulated device. The results of the extracted parameters for the device with HfO_2 gate oxide for various gate length and oxide thickness are shown in Table II.

Table II. Extracted Parameters of CSNWGAA-TFET with HfO_2 Gate Oxide

t_{ox} (nm)	L_g (nm)	V_T (V)	SS (mV/decade)	I_{ON}/I_{OFF} V_d 0.05 V	I_{ON}/I_{OFF} V_d 1.2 V	DIBL (mV/V)
3	100	0.599	19.910	1.2×10^7	7.8×10^9	8.24
3	150	0.604	20.981	3.6×10^7	4.1×10^8	9.78
3	180	0.605	22.218	2.1×10^7	5.2×10^9	9.24
5	100	0.944	21.252	3.1×10^7	6.5×10^9	7.68
5	150	0.948	28.260	2.9×10^6	3.1×10^9	7.10
5	180	0.952	27.541	3.0×10^7	2.6×10^8	7.89
6.5	100	1.264	22.392	2.6×10^7	4.6×10^8	7.44
6.5	150	1.266	34.364	2.6×10^8	4.1×10^9	10.26
6.5	180	1.268	33.049	2.4×10^7	2.4×10^9	9.89

Further, to compare and insight the performance variation due to HfO_2 gate oxide, the device oxide material has been replaced with SiO_2 material. The numerical analysis expanded to extract the device performance for the similar gate length and thickness of SiO_2 gate-oxide as listed in Table III.

TABLE III. EXTRACTED PARAMETERS FOR CSNWGAA-TFET WITH SiO_2 GATE OXIDE

t_{ox} (nm)	L_g (nm)	V_T (V)	SS (mV/decade)	I_{ON}/I_{OFF} V_d 0.05 V	I_{ON}/I_{OFF} V_d 1.2 V	DIBL mV/V
3	180	0.032	43.372	2.8×10^{7}	2.1×10^{8}	16.83
3	150	0.002	47.187	1.0×10^{6}	3.1×10^{7}	19.99
3	100	0.100	67.326	1.6×10^{6}	2.9×10^{7}	28.11
5	180	0.551	52.362	5.9×10^{5}	3.0×10^{9}	15.68
5	150	0.542	65.535	8.3×10^{7}	4.1×10^{8}	26.30
5	100	0.438	91.540	1.2×10^{7}	6.6×10^{9}	16.13
6.5	180	0.551	52.362	2.6×10^{6}	1.4×10^{9}	15.58
6.5	150	0.542	65.535	2.6×10^{7}	1.2×10^{9}	20.95
6.5	100	0.438	91.540	3.3×10^{7}	3.6×10^{8}	23.47

Fig. 8 shows the comparison of transfer characteristics of CSNWGAA TFET with HfO_2 and SiO_2 gate oxide materials. The result shows that highest ON current difference achieved in the simulation design with two different gate oxide is the order of 10^{-2} A/μm.

Fig. 9 illustrate transfer characteristics obtained from the simulated device at various gate lengths with 6.5 nm radius of the nanowire. With increasing positive gate voltage in the device with gate length 180 nm, the drain current gradually increases. A good agreement in the drain current at the L_g = 100 nm could be achieved.

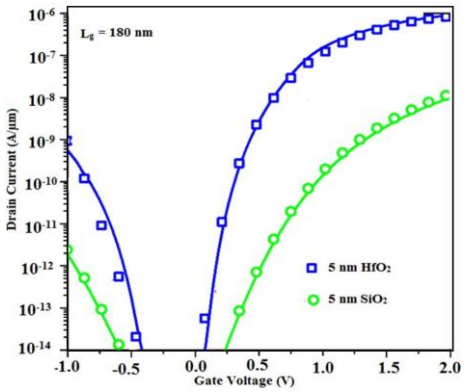


Fig. 8. Comparison of I_d-V_g characteristics of CSNW GAA TFET with two different gate oxide materials (L_g = 180 nm) and (t_{ox} = 5 nm).

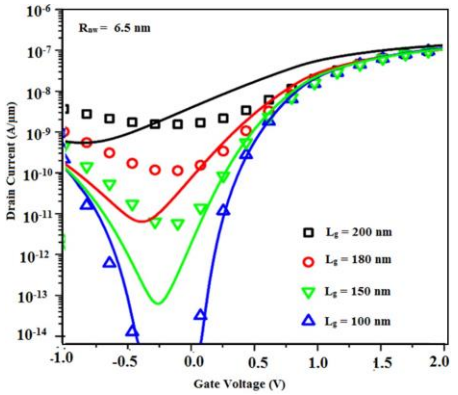


Fig. 9. I_d-V_g characteristics of CSNW GAA TFET at various channel lengths.

V. CONCLUSION AND FUTURE SCOPE

In this paper, the tunnel field effect transistor with Si-nanowire channel and cylindrical gate-all-around structure have been designed and simulated for the assessment of the impact of short channel effects (SCEs). The high-*k* material, i.e., Hafnium oxide (HfO_2; k = 25) has been used in the TFET structure as the gate oxide material. Firstly, the device simulation was intended to analyze the effect of channel length variation on device physics and further extended to study the effect of oxide-thickness variation at various channel length. As a result, it has been found that the electrical performance improves with the device using high-*k* gate oxide material in comparison to the conventional SiO_2 gate oxide.

The simulation results report the extracted parameter DIBL for HfO_2 ~ 7.6 mV/V (for SiO_2 ~ 16.13 mV/V), subthreshold swing (SS) for HfO_2 ~ 21.2 mV/decade (for SiO_2 ~ 91.5 mV/decade), and the I_{ON}/I_{OFF} of the order of 10^7~10^9. Due to the increased permittivity for high-*k* dielectric materials, equivalent oxide thickness decreases. The channel becomes isolated with high-*k* material for channel isolation effect as that of a much narrower oxide. Therefore, the gate control over the channel remains unchanged but the tunnel current is reduced. The DIBL reduces if the high-*k* material of low effective oxide thicknesses is used. In conclusion, the choice of high-*k* dielectric advances the device performance in the nanometer scales and the suitable for applications in logic and switching circuits. The effect of gate overlap distance from the source and drain terminal in the HFO_2 gate oxide device can be analyzed as the future scope of this work.

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