Analysis of Subthreshold Swing in Symmetric Junctionless Double Gate MOSFET Using high-k Gate Oxides

Hakkee Jung
Department of Electronic Engineering, Kunsan National University, Gunsan, Republic of Korea
Email: hkjung@kunsan.ac.kr

Abstract—**We observed the change of the subthreshold swings when the high-*k* material was used for the gate oxide of the junctionless double gate MOSFET (JLDG MOSFET). For this purpose, the analytical subthreshold swing model is proposed using the potential model derived from Poisson's equation. The subthreshold swing derived from the model proposed in this paper is in good agreement with the subthreshold swing value from the two-dimensional numerical simulation within the error of 5%. Using this model, we observed the change of subthreshold swing with respect to the channel length, silicon thickness and gate oxide thickness with a dielectric constant as a parameter. As a result, the subthreshold swing was greatly reduced and the changing rate of the subthreshold swing by the channel length, silicon thickness, and oxide thickness was 1 mV/dec-nm or less when the material with a dielectric constant of 30 or more was used as the gate oxide. Especially, it was found that the dielectric constant of the gate oxide for the JLDG MOSFET should be more than 30 in order to have a subthreshold swing of less than 65 mV/dec.**

Index Terms—**junctionless, subthreshold swing, dielectric constant, double gate, channel length**

I. Introduction

For high integration, low power consumption and high-speed operation, the size of transistors is continuously decreasing. In the case of conventional MOSFETs, due to the increase in short-channel effect with size reduction, a nano-structure transistor can no longer be used and a new structure transistor has been developed. A multi-gate structure transistor has been developed to solve problems for short-channel effects and commercialized [1], [2]. In addition, due to the ambiguity and depletion layer effect of the doping distribution occurring at the interface between the source/channel and the drain/channel as the transistor size is reduced by scaling, a junctionless structure multi-gate MOSFET has been developed [3]-[5]. However, the parasitic current through the gate oxide film increases because of the thinning of the oxide film due to the scaling effect when the size of the junctionless multi-gate structure is reduced. In the case of the SiO_2 layer, it can be found that parasitic current exceeding 1 A/cm^2 at 1 V flows into gate contact [6]. In order to solve this problem, it has been tried to reduce the gate parasitic current by using a material having a high dielectric constant in the gate oxide [7]. In addition, high-*k* gate oxide films must be used to reduce transistor size while reducing short-channel effects. In the case of SiO_2, Al_2O_3, Y_2O_3, HfO_2/ZrO_2, La_2O_3, and TiO_2 as gate oxide films, Priya et al. analyzed the subthreshold characteristics of junctionless tunnel transistors. Sakshi *et al.* used SiO_2, Al_2O_3, HfO_2, and Ta_2O_5 to analyze the threshold voltage [8], [9]. In addition, Xie et al. proposed a potential model using scale length to analyze short-channel effects on Junctionless Double Gate (JLDG) MOSFETs, but only analyzed for threshold voltage shift [10]. Nirmal et al. have also shown that the on-off current ratio is improved for high-*k* gate oxide by analyzing the on-off current when various gate oxide films are used in a double gate MOSFET [11]. Efforts are being made to improve the performance of the transistor using the high-*k* gate oxide film. In this paper, we use the Xie model to analyze the variation of the subthreshold swing when the gate oxide films are SiO_2, Al_2O_3, Y_2O_3, HfO_2/ZrO_2, La_2O_3, and TiO_2. To this end, we will present a new analytical subthreshold swing model using Xie's potential model.

In Section 2, we will explain the analytical potential distribution and subthreshold swing model of JLDG structure MOSFETs. In Section 3, we will analyze the obtained subthreshold swing according to dielectric constant, and conclude in Section 4.

II. The Structure and Subthreshold Swing Model of JLDG Mosfet

Fig. 1 shows a schematic diagram of a junctionless double-gate MOSFET used in this paper. The source and drain were heavily doped with 10^{20}/cm^3, and the channel was doped with 10^{19}/cm^3. The gate uses metal with a work function of 4.68 eV. The ε_{ox} is the dielectric constant of the oxide film, and SiO_2, Al_2O_3, Y_2O_3, HfO_2/ZrO_2, La_2O_3, and TiO_2 are used as gate oxide with dielectric constants of 3.9, 9, 15, 25, 30, and 80 respectively. The ε_{si} is the dielectric constant of silicon, L_g the gate length, t_{si} the silicon thickness, and t_{ox} the oxide

Manuscript received May 3, 2019; revised May 21, 2019; accepted June 6, 2019.
Corresponding author: Hakkee Jung (email: hkjung@kunsan.ac.kr).

©2019 Int. J. Elec. & Elecn. Eng. & Telcomm.

doi: 10.18178/ijeetc.8.6.334-339

film thickness. The potential distribution derived by Xie et al. can be expressed as the following series [10].

$$\phi(x,y) = -\frac{qN_d x^2}{2\varepsilon_{si}} + V_{gs} - \Delta\phi + \frac{qN_d t_{si}^2}{8\varepsilon_{si}}\left(1+\frac{4\varepsilon_{si}t_{ox}}{t_{si}\varepsilon_{ox}}\right) + \sum_{n=1}^{\infty}\frac{b_n \sinh\left[\frac{\pi(L_g-y)}{\lambda_n}\right] + c_n \sinh\left[\frac{\pi y}{\lambda_n}\right]}{\sinh\left[\frac{\pi L_g}{\lambda_n}\right]}\cos(\pi x/\lambda_n) \quad (1)$$

$$b_n = \left[\frac{\left(\frac{2\lambda_n^2}{\pi^2 t_{ox}}\right)\tan\left(\frac{\pi t_{ox}}{\lambda_n}\right)\sin\left(\frac{\pi t_{si}}{2\lambda_n}\right)\left(\frac{E_g}{2q}-\phi_0\right)+\left(\frac{\lambda_n^2 qN_d t_{si}}{\pi^2\varepsilon_{si}}\right)\times}{\cos\left(\frac{\pi t_{si}}{2\lambda_n}\right)\left(1-\frac{2\lambda_n}{\pi t_{si}}\tan\left(\frac{\pi t_{si}}{2\lambda_n}\right)+\left(\frac{t_{si}}{4t_{ox}}\right)\tan\left(\frac{\pi t_{si}}{2\lambda_n}\right)\tan\left(\frac{\pi t_{ox}}{\lambda_n}\right)\right)} \over \frac{t_{si}}{2}+t_{ox}\frac{\sin\left(\frac{\pi t_{si}}{\lambda_n}\right)}{\sin\left(\frac{2\pi t_{ox}}{\lambda_n}\right)}\right]$$

$$c_n = \left[\frac{\left(\frac{2\lambda_n^2}{\pi^2 t_{ox}}\right)\tan\left(\frac{\pi t_{ox}}{\lambda_n}\right)\sin\left(\frac{\pi t_{si}}{2\lambda_n}\right)\left(\frac{E_g}{2q}+V_{ds}-\phi_0\right)+\left(\frac{\lambda_n^2 qN_d t_{si}}{\pi^2\varepsilon_{si}}\right)\times}{\cos\left(\frac{\pi t_{si}}{2\lambda_n}\right)\left(1-\frac{2\lambda_n}{\pi t_{si}}\tan\left(\frac{\pi t_{si}}{2\lambda_n}\right)+\left(\frac{t_{si}}{4t_{ox}}\right)\tan\left(\frac{\pi t_{si}}{2\lambda_n}\right)\tan\left(\frac{\pi t_{ox}}{\lambda_n}\right)\right)} \over \frac{t_{si}}{2}+t_{ox}\frac{\sin\left(\frac{\pi t_{si}}{\lambda_n}\right)}{\sin\left(\frac{2\pi t_{ox}}{\lambda_n}\right)}\right]$$

$$\phi_0 = V_{gs} - \Delta\phi + \frac{qN_d t_{si}^2}{8\varepsilon_{ox}}\left(1+\frac{4\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\right)$$

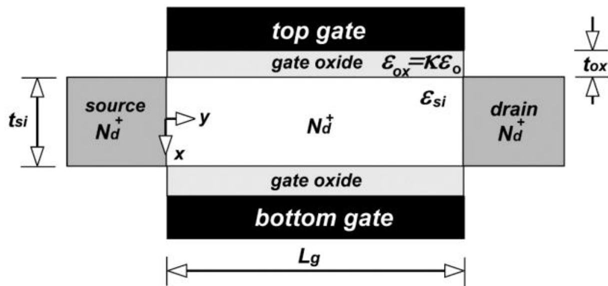

Fig. 1. Schematic cross-sectional diagram of Junctionless Double Gate (JLDG) MOSFET.

Here, the E_g is the energy bandgap of silicon, V_{ds} the drain voltage, V_{gs} the gate voltage, $\Delta\phi$ the difference between the work function of the gate metal and the channel, ϕ_0 the center potential at x=y=0. As shown in (1), they directly affect the potential distribution.

Fig. 2 shows the potential distribution along the center axis calculated using (1) in the subthreshold region. As can be seen in Fig. 2, the potential distribution varies greatly depending on the dielectric constant. As the dielectric constant increases, the potential distribution decreases further and the flow of carrier in the channel decreases. This will result in a decrease in on-off current, but the ratio of on-off current is known to increase as the dielectric constant increases [11]. The eigenvalue λ_n in (1) can be obtained by solving the following eigenfunction.

$$\varepsilon_{si}\tan\left(\frac{\pi t_{ox}}{\lambda_1}\right) - \varepsilon_{ox}\cot\left(\frac{\pi t_{si}}{2\lambda_1}\right) = 0$$
$$\lambda_n \approx \frac{\lambda_1}{n}\ (n = 1, 3, 5, \cdots\cdots\cdots) \quad (2)$$

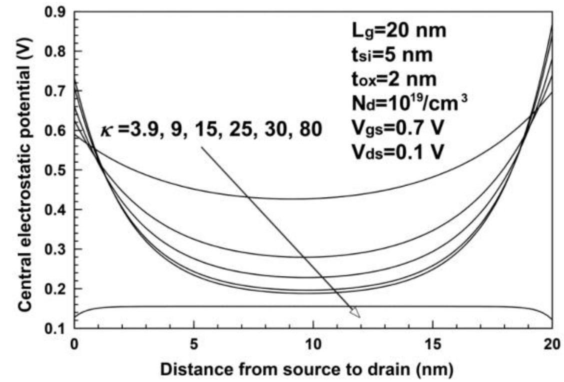

Fig. 2. Central electrostatic potentials for various dielectric constants in the junctionless double gate (JLDG) MOSFET.

In the case of a symmetrical double-gate MOSFET, the potential distribution can be obtained by substituting λ_1, λ_3, λ_5, ··· into (1) since the eigenvalues are not 0 only in the case of an odd number. The longest eigenvalue λ_1 is called the scale length. In general, it has been reported that only using n=1 in the case of L_g>1.5λ_1 is sufficient when analyzing short-channel effects [10]. Therefore, we want to obtain an analytical model of the subthreshold swing at n=1. In order to take into account the range of L_g>1.5λ_1, the change of scale length with respect to the change of the dielectric constant is shown in Fig. 3 while the oxide thickness is changed to 1, 2, and 3 nm with the channel length of 20 nm and the silicon thickness of 5 nm. Since the channel length is 20 nm, the subthreshold swing can be sufficiently analyzed from the potential distribution using n = 1 in (1) if the scale length is smaller than 13.3 nm. In Fig. 3, it can be found that all of the dielectric constants satisfy the condition of L_g>1.5λ_1 except for the case where the thickness of SiO_2 is 3 nm. Therefore, in this paper, we will analyze the subthreshold swing using only the potential distribution when n = 1.

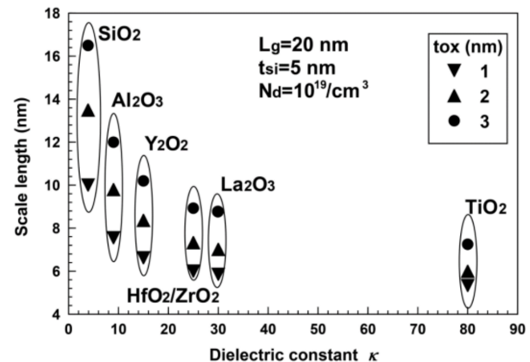

Fig. 3. Scale lengths for various dielectric constants with oxide thickness as a parameter under the given conditions.

In the first case, we rewrite (1) at n=1 as follows:

©2019 Int. J. Elec. & Elecn. Eng. & Telcomm.

$$\phi(x,y) = A + B\sinh\left[\frac{\pi(L_g - y)}{\lambda_1}\right] + C\sinh\left[\frac{\pi y}{\lambda_1}\right] \quad (3)$$

$$A = -\frac{qN_d x^2}{2\varepsilon_{si}} + V_{gs} - \Delta\phi + \frac{qN_d t_{si}^2}{8\varepsilon_{si}}\left(1 + \frac{4\varepsilon_{si}t_{ox}}{t_{si}\varepsilon_{ox}}\right)$$

$$B = b_1 \cos\left(\frac{\pi x}{\lambda_1}\right) \Big/ \sinh\left(\frac{\pi L_g}{\lambda_1}\right)$$

$$C = c_1 \cos\left(\frac{\pi x}{\lambda_1}\right) \Big/ \sinh\left(\frac{\pi L_g}{\lambda_1}\right)$$

The subthreshold swing is a measure of the gate voltage change with respect to the drain current change. If the electron density constituting the drain current can be approximated as $n=N_d e^{q\phi_{min}/kT}$ by a Boltzmann distribution using minimum potential $\phi_{\min}$, the subthreshold swing is expressed such as the following equation,

$$SS = \frac{\partial V_{gs}}{\partial \log I_{ds}} = \ln(10)\left(\frac{kT}{q}\right)\left(\frac{\partial \phi_{\min}}{\partial V_{gs}}\right)^{-1} \quad (4)$$

Here, k is the Boltzmann constant and T is absolute temperature. To obtain $\phi_{\min}$ in (4), we find $y=y_{\min}$ that satisfies $\partial\phi(x,y)/\partial y=0$ and substitute the $y_{\min}$ into (3). The $y_{\min}$ thus obtained is as follows:

$$y_{\min} = \left(\frac{\lambda_1}{\pi}\right)\cosh^{-1}\sqrt{U} \quad (5)$$

where

$$U = \frac{b_1^2}{b_1^2 - \left[b_1 \coth\left(\frac{\pi L_g}{\lambda_1}\right) - c_1 \operatorname{csch}\left(\frac{\pi L_g}{\lambda_1}\right)\right]^2} \; .$$

In the case of the JLDG MOSFET, most carriers flow through the center of the channel, so we can obtain the ϕ_{min} by substituting $y=y_{min}$ and $x=0$ in (3). Equation (A1) is obtained by differentiating ϕ_{min} with respect to V_{gs}. Substituting (A1) into (4) yields a subthreshold swing. The differential value for V_{gs} of the ϕ_{min} in (A1) will vary according to the b_1 and c_1, and those depend on the dielectric constant as shown in (1). Consequently, the subthreshold swing will vary with the dielectric constant. In this paper, we will observe the validity of (4) and use (A1) and (4) to find the change of the subthreshold swing for the change of the dielectric constant with the channel length, silicon thickness, and gate oxide thickness as parameters.

III. Subthreshold Swing According to Dielectric Constants for Gate Oxide of JLDG Mosfet

In order to observe the validity of (A1) and (4), we compare the two-dimensional numerical simulation TCAD results [12] with the subthreshold swings derived from the analytical subthreshold swing model of this paper in Fig. 4. As can be seen in Fig. 4, the analytical model of this paper is in good agreement with the TCAD simulation results within the error of 5%. However, it can be observed that the error increases for the channel length of 20 nm since λ_1 is 20 nm under the condition given in Fig. 4 and the channel length satisfying the condition of $L_g>1.5\lambda_1$ is more than 30 nm. As shown in Fig. 2, the scale length λ_1 decreases as the dielectric constant increases. Therefore, the channel length to which the analytical subthreshold swing model suggested in this paper is applied will be further reduced. Using the (A1) and (4), we can interpret the subthreshold swing of the JLDG MOSFET in the channel length range calculated in this paper, except for the case of SiO_2 with a very thick oxide thickness and a dielectric constant of 3.9.

Fig. 5 shows the subthreshold swing for various gate oxide materials with the gate oxide thickness as a parameter. As the dielectric constant increases, the subthreshold swing decreases as shown in Fig. 5. The changing rate of the subthreshold swing decreases with the changing rate of the gate oxide film thickness as the dielectric constant increases. Also, as the dielectric constant increases, the subthreshold swing sharply decreases. As the dielectric constant increases above 30, the subthreshold swing decreases to less than 65 mV/dec. The reason for this is that the parasitic current decreases as the dielectric constant increases. In particular, TiO_2 is close to the ideal threshold voltage of 60 mV/dec, regardless of the gate oxide thickness. As shown in Fig. 5, the subthreshold swing rapidly decreases when the dielectric constant is 30. When the dielectric constant is above 30, the subthreshold swing is maintained at a constant value as the dielectric constant increases.

Therefore, the on-off current ratio will increase with the increase of the dielectric constant and the transistor performance will be improved [16].

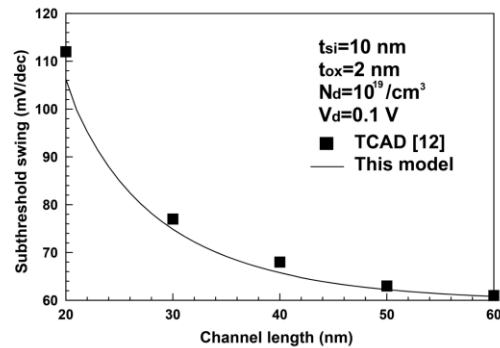

Fig. 4. Comparison of subthreshold swings for this analytical model and TCAD simulation [12] for κ=3.9

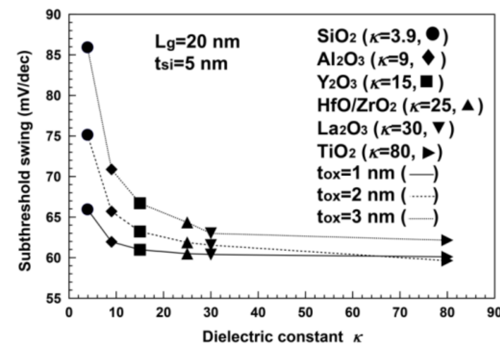

Fig. 5. Comparison of subthreshold swings of this analytical model for various dielectric constants with oxide thickness as a parameter

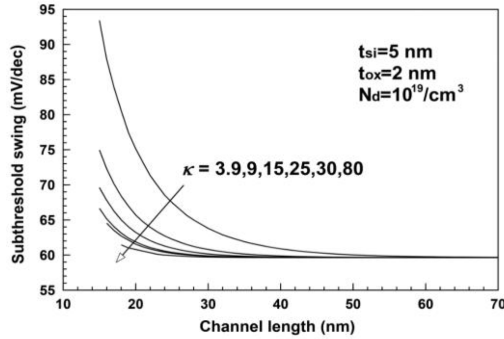

Fig. 6. Comparison of subthreshold swings of this analytical model for channel length with dielectric constant as a parameter

The change of the subthreshold swing along with the channel length is shown in Fig. 6 as a parameter of dielectric constant. As seen in Fig. 6, in the case of SiO_2 with a dielectric constant of 3.9, it can be seen that the subthreshold swing greatly changes along with the channel length. That is, the short channel effect becomes large and the subthreshold swing increases greatly as the channel length decreases. However, the short channel effect decreases as the dielectric constant increases. In particular, it is observed that the TiO_2 with a dielectric constant of 80 does not show the short channel effect even if the channel length decreases. The sharp increase of the subthreshold swing due to the short channel effect can be observed especially at a dielectric constant of 30 or less. That is, the subthreshold swing is maintained at 65 mV/dec or less with the dielectric constant of 30 or more even if the channel length is reduced to 15 nm. In fact, for TiO_2 with a dielectric constant of 80, excellent short channel effect can be observed as shown in Fig. 5 and Fig. 6. But, TiO_2 has a low energy band gap of about 3.2 eV and a low energy band offset value for silicon used as a channel. It is also pointed out that the limitation of mobility is due to the roughness of the Si/TiO_2 interface and the interface trap state [13]. A process for solving this problem has been developed, but a material with a dielectric constant near 30 may solve the above problems and reduce the short channel effect [9].

Fig. 7 shows the change of the subthreshold swing with respect to the dielectric constants with the silicon thickness as a parameter. When the dielectric constant is small, it is observed that the change of the subthreshold swing is large to the change in the silicon thickness. It is also observed that the subthreshold swing decreases from 80.4 mV/dec to 61.6 mV/dec when dielectric constant increases from 3.9 to 80 at the silicon thickness of 6 nm, but that only decreases from 70.5 mV/dec to 60.0 mV/dec at the silicon thickness of 4 nm. When the dielectric constant was increased to 15 or more, note that the subthreshold swing was 65 mV/dec or less regardless of the silicon thickness. It can be seen that the variation of the subthreshold swing with the change of the silicon thickness is almost constant if the dielectric constants increase to 30 or more. A dielectric material with a dielectric constant greater than 30, which forms a smooth and excellent interface with silicon, will be most suitable for reducing the short channel effect as the size of the JLDG MOSFET decreases.

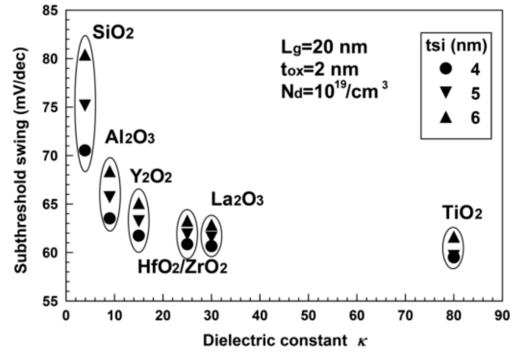

Fig. 7. Comparison of subthreshold swings of this analytical model for various dielectric constants with silicon thickness as a parameter.

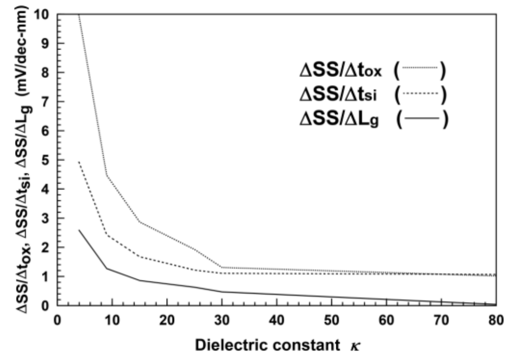

Fig. 8. The changing rate of subthreshold swing for channel length, silicon thickness, and oxide thickness.

The changes in the subthreshold swing for channel lengths from 15 nm to 25 nm, silicon thicknesses from 4 nm to 6 nm and oxide thickness variations from 1 nm to 3 nm are shown in Fig. 8. As can be seen in Fig. 8, the rate of change was greatly decreased with increasing dielectric constant. Particularly, when the dielectric constant is more than 30, the change of the subthreshold swing to the size change of 1 nm is less than 1 mV/dec. Also, the $\Delta SS/\Delta t_{ox}$, the variation of the subthreshold swing with the thickness of the oxide film was the largest. In particular, when the oxide material having a small dielectric constant such as SiO_2 is used, the rate of change is more than 10 mV/dec-nm for the change of oxide thickness.

The transconductance-to-drain current ratio g_m/I_d is a measure of the device's performance. This ratio describes how efficiently the current is used to achieve a certain value of transconductance. The high value of the g_m/I_d is very useful for the design of an analog IC. Moreover, the g_m/I_d is used for obtaining the threshold voltage [14] and the subthreshold swing [15] of the device. It can be expressed as a derivative of minimum potential $\phi_{\min}$ with respect to the gate voltage by using (4) as follows.

$$\frac{g_m}{I_d} = \frac{1}{I_d}\frac{\partial I_d}{\partial V_{gs}} = \frac{\partial(\ln I_d)}{\partial V_{gs}} = \frac{\ln(10)}{SS} = \frac{\partial \phi_{\min}}{\partial V_{gs}} \bigg/ \frac{kT}{q} \tag{6}$$

The transconductance-to-drain current ratio can be obtained using (A1), which is equal to the value obtained by dividing ln(10) by the subthreshold swing, as shown in (4) and (6). Therefore, for an ideal device with a subthreshold swing of 60 mV/dec, the maximum value of g_m/I_d is equal to nearly 38.5 V^{-1}, which is $(kT/q)^{-1}$. The

g_m/I_d value obtained by using (6) is shown in Fig. 9 with a dielectric constant as a parameter. As can be seen from Fig. 9, when the dielectric constant increases, the g_m/I_d value greatly increases, reaching the ideal g_m/I_d value when the channel length is 30 nm and the dielectric constant is 30. When the dielectric constant is large, the reduction of the g_m/I_d value due to the reduction of the channel length is very small. However, in the case of the SiO_2 having the dielectric constant of 3.9, the g_m/I_d is greatly decreased as the channel length is decreased.

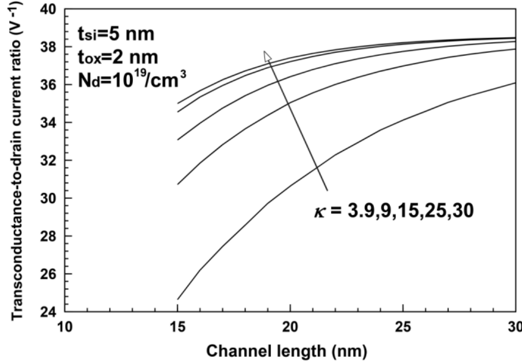

Fig. 9. Transconductance-to-drain current ratio by this analytical model for channel length with dielectric constant as a parameter.

IV. Conclusions

In this paper, the changes of the subthreshold swing have been analyzed for the change of the channel length, silicon thickness, and oxide thickness when a material with the high-κ dielectric constant used as a gate oxide film, in order to reduce the short channel effect caused by the scaling of JLDG MOSFET. We proposed the analytical subthreshold swing model using the potential distribution obtained by Poisson's equation. The results derived from the analytical model of the subthreshold swing proposed in this paper are in good agreement with the results of the two-dimensional numerical simulation. Using this analytical model, we observed the deviation of subthreshold swing for changes in the channel length, silicon thickness, and gate oxide thickness of the JLDG MOSFET with the dielectric constant as a parameter. As a result, the subthreshold swing decreases as the dielectric constant increases. The transconductance-to-drain current ratio shows high value for the dielectric material with a dielectric constant greater than 30. However, in the case of a material having a high dielectric constant, defects are generated at the interface with silicon. Therefore, a technique for forming a good interface should be developed.

Appendix A

$$\frac{d\phi_{\min}}{dV_{gs}} = 1 + \frac{1}{\sinh\left(\frac{\pi L_g}{\lambda_1}\right)}\left[\frac{db_1}{dV_{gs}}\sinh\left[\frac{\pi(L_g - y_{\min})}{\lambda_1}\right] + \frac{dc_1}{dV_{gs}}\sinh\left[\frac{\pi y_{\min}}{\lambda_1}\right] + b_1\frac{d\sinh\left[\frac{\pi(L_g - y_{\min})}{\lambda_1}\right]}{dV_{gs}} + c_1\frac{d\sinh\left[\frac{\pi(L_g - y_{\min})}{\lambda_1}\right]}{dV_{gs}}\right]$$

$$\frac{db_1}{dV_{gs}} = \frac{dc_1}{dV_{gs}} = \frac{(-1)\left[2\frac{\lambda_1^2}{t_{ox}\pi^2}\tan\left(\frac{\pi L_g}{\lambda_1}\right)\sin\left(\frac{\pi t_{si}}{2\lambda_1}\right)\right]}{\left[\frac{t_{si}}{2} + \left[t_{ox}\sin\left(\frac{\pi t_{si}}{\lambda_1}\right)\right]\Big/\sin\left(\frac{2\pi t_{ox}}{\lambda_1}\right)\right]}$$

$$\frac{d\sinh\left\{\left[\pi(L_g - y_{\min})\right]/\lambda_1\right\}}{dV_{gs}} = \cosh\left[\frac{\pi(L_g - y_{\min})}{\lambda_1}\right]\left[-\frac{\pi}{\lambda_1}\right]\frac{dy_{\min}}{dV_{gs}}$$

$$\frac{d\sinh\left[(\pi y_{\min})/\lambda_1\right]}{dV_{gs}} = \cosh\left[\frac{\pi y_{\min}}{\lambda_1}\right]\left[\frac{\pi}{\lambda_1}\right]\frac{dy_{\min}}{dV_{gs}}$$

$$\frac{dy_{\min}}{dV_{gs}} = \frac{\pi/\lambda_1}{\sqrt{U-1}}\frac{1}{2\sqrt{U}}\left[2b_1\frac{1}{b_1^2 - (a_1b_1 - a_2c_1)^2}\frac{db_1}{dV_{gs}} - b_1^2\left(\frac{1}{b_1^2 - (a_1b_1 - a_2c_1)^2}\right)^2\left(2b_1\frac{db_1}{dV_{gs}} - 2(a_1b_1 - a_2c_1)\left(a_1\frac{db_1}{dV_{gs}} - a_2\frac{dc_1}{dV_{gs}}\right)\right)\right]$$

$$a_1 = \cot\left[\frac{\pi L_g}{\lambda_1}\right],\quad a_2 = \cos\left[\frac{\pi L_g}{\lambda_1}\right]$$

References

[1] P. Hill. (June 22, 2017). Samsung begins mass production of the Exynos i T200 aimed at IoT. [Online]. Available: https://www.neowin.net/news/sam sung-begins-mass-production-of-exynos-i-t200-aimed-at-iot/

[2] D. Schor. (July 1, 2018). VLSI 2018: Samsung's 8 nm 8LPP, a 10 nm extension. [Online]. Available: https://fuse.wikichip.org/news/1443/vlsi-2018-Samsungs-8nm-8lpp-a-10nm-extension/

[3] Y. Wang, Y. Tang, L. Sun, and F. Cao, "High performance of junctionless MOSFET with asymmetric gate," *Superlattices and Microstructures*, vol. 97, pp. 8-14, Sep. 2016.

[4] L. Chen, M. Yeh, Y. Lin, K. Lin, M. Wu, V. Thirunavukkarasu,

and Y. Wu, "The Physical analysis on electrical junction of junctionless FET," *AIP ADVANCES*, vol. 7, no. 2, pp. 025301-1-5, 2017.

[5] Y. H. Shin, S. Weon, D. Hong, and I. Yun, "Analytical model for junctionless double-gate FET in subthreshold region," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1433-1440, April 2017.

[6] J. Ajayan, D. Nirmal, P. Prajoon, and J. C. Pravin, "Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-k dielectric for high speed applications," *Int. Journal of Electronics and Communications*, vol. 79, pp. 151-157, Sep. 2017.

[7] V. Kumar, R. Gupta, R. P. P. Singh, and R. Vaid, "Performance analysis of double gate n-FinFET using high-k dielectric materials," *Int. Journal of Innovative Research in Science, Engineering and Technology*, vol. 5, no. 7, pp. 13242-13249, 2016.

[8] G. L. Priya and N. B. Balamurugan, "New dual material double gate junctionless tunnel FET: Subthreshold modeling and simulation," *Int. Journal of Electronics and Communications*, vol. 99, pp. 130-138, Feb. 2019.

[9] Sakshi, S. Dhariwal, and A. Singh, "Analyzing the effect of gate dielectric on the leakage currents," in *Proc. MATEC Web of Conf.*, 2016, vol. 57, pp. 01028-1-5.

[10] Q. Xie, Z. Wang, and Y. Taur, "Analysis of short-channel effects in junctionless DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3511-3514, Aug. 2017.

[11] D. Nirmal, V. Kumar, P. C. Samuel, Shruthi, D. M. Thomas, and M. Kumar, "Analysis of dual gate MOSFETs using high k dielectrics," in *Proc. 3rd Int. Conf. on Electronics Computer Technology*, Kanyakumari, India, April 8-11, 2011.

[12] C. Jiang, R. Liang, J. Wang, and J. Xu, "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs," *AIP ADVANCES*, vol. 5, no. 5, pp. 057122-1-13, May 2015.

[13] A. Balhara and D. Punia, " Design and analysis of double gate MOSFET devices using high-k dielectric," *International Journal of Electrical Engineering*, vol. 7, no. 1, pp. 53-60, 2014.

[14] R. D. Trevisoli, R. T. Doria, M. de Souza, and M. A. Pavanello, "A physically-based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors," *Solid State Electron.*, vol. 90, pp. 12-17, Dec. 2013.

[15] K. Rajendran and G. S. Samudra, "Modelling of transconductance-to-drain current ratio(gm/Id) analysis on double-gate SOI MOSFETs," *Semicond. Sci. Technol.*, vol. 15, pp. 139-144, 2000.

[16] M. S. Islam, J. Afza, and S. Tarannum, "Modelling and performance analysis of asymmetric double gate stack-oxide junctionless FET in subthreshold region," presented at 2017 IEEE Region 10 Humanitarian Technology Conference, Dhaka, Dec. 21-23, 2017.

Hakkee Jung received the B.S. degree from Ajou University, Korea, in 1983, the M.S. and Ph.D. degrees from Yonsei University, Seoul, Korea, in 1985, 1990, respectively, all in electronic engineering. In 1990, he joined Kunsan National University, Chonbuk, Korea, where he is currently a Professor in the Department of Electronic Engineering. From 1994 to 1995, he held a research position with the Department Electronic Engineering, Osaka University, Osaka, Japan. From 2004 to 2005 and from 2015 to 2016, he was with the School of Microelectronic Engineering, Griffith University, Nathan, QLD, Australia. His research interests include semiconductor device physics and device modeling with a strong emphasis on quantum transport and Monte Carlo simulations. Prof. Jung received the best paper award from The Korean Federation of Science and Technology Societies 2010, and he was the president of the Korea Institute of Information and Communication Engineering from 2014 to 2015.