

A Small DC-AC Inverter by Using Cross-Connected Charge Pumps

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Abstract—This paper introduces a Switched-Capacitor (SC) DC-AC inverter with cross-connected topology. By cross connecting two charge pump DC-DC converters, the proposed SC DC-AC inverter can achieve small size with a grounded input. Moreover, the cross-connected structure provides the reduction of internal resistance. Therefore, not only small size but also efficient energy conversion can be realized by the proposed inverter. The characteristics of the proposed inverter were investigated by theoretical analysis as well as SPICE (simulation program with integrated circuit emphasis) simulations. The proposed inverter demonstrates higher performances, such as small size and high-power efficiency, than traditional SC DC-AC converters.

Index Terms—charge pump, DC-AC inverters, high voltage gain, clean energy technologies

I. INTRODUCTION

Currently, most of the household electric appliances are operated by AC voltages. Therefore, a DC-AC inverter is a key component to provide AC voltages for household electric appliances. Especially, the DC-AC inverter with small size and high-power efficiency is desirable for developing efficient electric appliances.

The DC-AC inverters have been studied in past studies. For example, a flexible multilevel boost DC-AC inverter was developed by Babaei [1]. By adding sharing switches and capacitors to the traditional boost converter, the multi-output boost converter provides a multilevel output, where the number of output levels is proportional to the number of capacitors. Following this study, Debre *et al.* proposed Z source based multilevel inverter [2]. However, due to the existence of magnetic components and many capacitors, these inverters suffer from large volume and heavy weight. For this reason, a switched capacitor (SC) DC-AC inverter that do not use magnetic component has been receiving much attention. Owing to the inductor-less topology, the SC inverter can realize not only small size but also small electro magnetic interference (EMI). The SC inverter can be divided into two types: the SC inverter

with grounded inputs and the SC inverter with non-grounded inputs.

In previous studies, Gautam and Pakala *et al.* proposed multilevel inverter with reduced number of devices [3], [4]. By utilizing non-grounded input sources such as PV panels, these SC inverters can provide small and simple structure. However, the application field is limited, because these SC inverters require non-grounded input sources.

On the other hand, several SC inverters with grounded input sources have been developed by assuming a battery input. Unlike the SC inverter with non-grounded input sources, the SC inverter with grounded input sources can be applied to many applications. In past studies, Ueno *et al.* and Oota *et al.* proposed the series-parallel type SC inverter [5], [6]. By modifying the series-parallel type SC inverter, Ishimatsu *et al.* and Ueno *et al.* developed the voltage equation type SC inverter [7], [8] for lighting electro-luminescence. Following this study, Eguchi *et al.* and Abe *et al.* proposed the Fibonacci-type SC inverter [9], [10] to achieve small size and high voltage gain. However, these SC inverters suffer from large number of circuit components and low power efficiency.

For small power applications, we propose an SC DC-AC inverter with a grounded input in this paper. Unlike existing SC inverters, the proposed inverter has a cross-connected topology [11], [12] utilizing two charge pump converters [13], [14]. The cross-connected topology provides the reduction of circuit components, output ripple, and internal resistance. Therefore, the proposed inverter can achieve small size and high power efficiency. To clarify the effectiveness of the proposed topology, the characteristics of the proposed inverter are investigated by not only SPICE (Simulation Program with Integrated Circuit Emphasis) simulations but also theoretical analysis.

The remainder of this paper is organized as follows. In Section 2, the circuit configuration of the proposed inverter is presented. In Section 3, we analyze the characteristics of the proposed inverter theoretically. In Section 4, the characteristic comparisons between the proposed inverter and traditional SC inverter are shown. The circuit simulation results of the proposed inverter are shown in Section 5. Finally, the conclusion and future work are drawn in Section 6.

Manuscript received October 4, 2018; revised April 6, 2019; accepted April 30, 2019.

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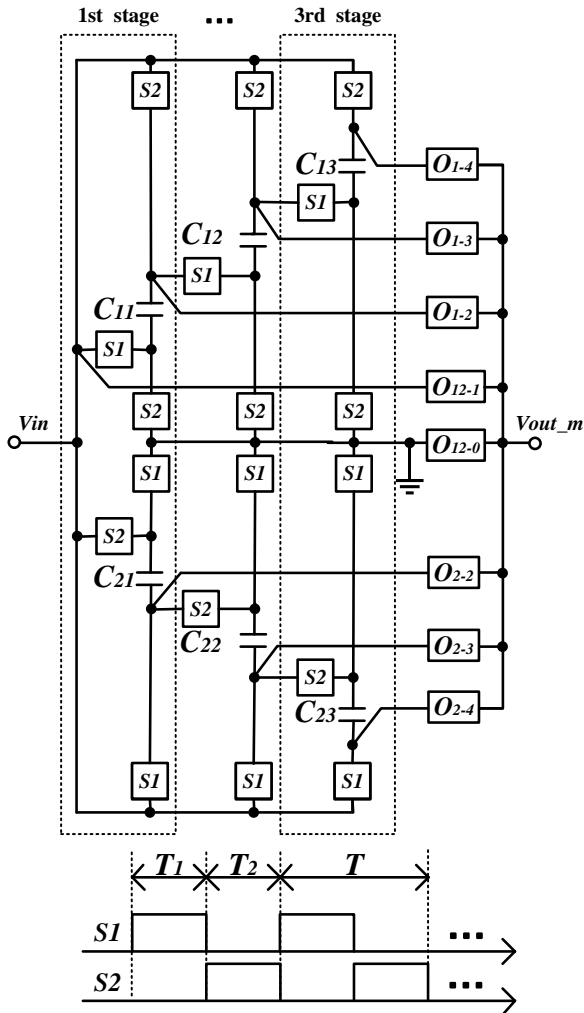


Fig. 1. Inverter topology of the traditional SC-type inverter [6] with 9 steps.

II. INVERTER TOPOLOGY

A. Traditional SC-Type Inverter [6]

Fig. 1 illustrates an example of the topology of the traditional series-parallel type SC inverter [6], where the number of steps is 9. By driving switches S_1 and S_2 cyclically by two-phase rectangular pulses, the capacitors of the traditional SC-type inverter, C_{kn} , is charged as

$$V_{C_{kn}} = V_{in}, \quad (n \geq 1) \quad (1)$$

where the parameters k and n are integers and $V_{C_{kn}}$ denotes the voltage the capacitor C_{kn} . In the series-parallel type SC inverter, the voltage of capacitor C_{kn} ($k=1, 2$ and $n=1, 2, 3$) becomes V_{in} . By extracting the capacitor voltage $V_{C_{kn}}$ through the switches O_{1m} and O_{2m} , an AC voltage is generated from the DC voltage shown as

$$V_{out,m} = mV_{in}, \quad (-n - 1 \leq m \leq n + 1) \quad (2)$$

where the parameter m is an integer from $-n - 1$ to $n + 1$. Therefore, by increasing the number of stages, the traditional SC inverter can realize multilevel output easily. However, in proportion to the number of stages, the number of circuit components increases linearly.

B. Traditional Fibonacci-Type Inverter [10]

Fig. 2 illustrates an example of the topology of the traditional Fibonacci-type inverter [10], where the number of steps is 9. By driving switches S_1 and S_2 cyclically by four-phase rectangular pulses, the capacitors of the traditional Fibonacci-type inverter, C_{kn} , is charged as

$$V_{C_{kn}} = nV_{in}, \quad (n \geq 1) \quad (3)$$

where the parameters k and n are integers and $V_{C_{kn}}$ denotes the voltage the capacitor C_{kn} . In the Fibonacci-type inverter, the voltage of capacitor C_{kn} ($k=1, 2$ and $n=1, 2$) becomes V_{in} and $2V_{in}$. By extracting the capacitor voltage $V_{C_{kn}}$ through the switches O_{1m} and O_{2m} , an AC voltage is generated from the DC voltage shown as

$$V_{out,m} = mV_{in}, \quad (-2n \leq m \leq 2n) \quad (4)$$

where the parameter m is an integer from $-2n$ to $2n$. Therefore, by increasing the number of stages, the traditional Fibonacci-type inverter can realize multilevel output easily. However, in proportion to the number of stages, the number of circuit components increases linearly.

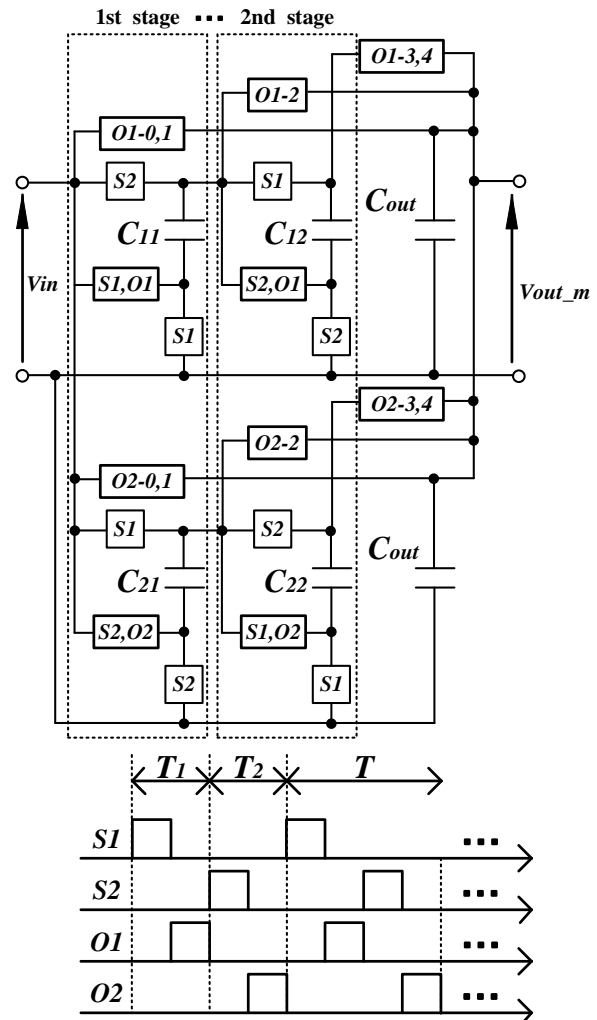


Fig. 2. Inverter topology of the traditional Fibonacci-type inverter [10] with 9 steps.

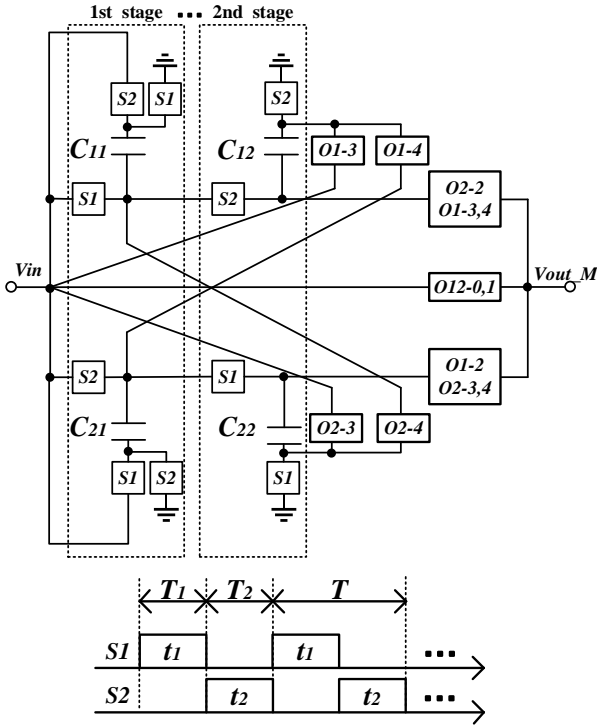


Fig. 3. Inverter topology of the proposed cross-connected inverter with 9 steps.

C. Proposed Inverter

The topology of the proposed inverter is shown in Fig. 3, where the number of steps is 9. By driving S_1 and S_2 by two-phase clock pulses, t_1 and t_2 , the capacitors of the proposed inverter, C_{kN} , is charged as

$$V_{C_{kN}} = NV_{in}, \quad (N \geq 1) \quad (5)$$

where the parameter N is an integer and $V_{C_{kN}}$ indicates the voltage the capacitor C_{kN} . In Fig. 3, the voltage of capacitor C_{kN} ($k=1, 2$ and $N=1, 2$) becomes V_{in} and $2V_{in}$. By extracting the capacitor voltage $V_{C_{kN}}$ through the switches O_{1m} and O_{2m} , an AC voltage is generated from the DC voltage shown as

$$V_{out_M} = MV_{in}, \quad (-2N \leq M \leq 2N) \quad (6)$$

where the parameter M is an integer from $-2N$ to $2N$. As you can see from (1), (3) and (5), the proposed inverter can charge higher voltage to the capacitor C_{kN} than the traditional SC inverter.

III. THEORETICAL EVALUATION

In this section, the proposed inverter shown in Fig. 3 will be evaluated theoretically. Concretely, power efficiency and output voltage are analyzed by using the equivalent model of Fig. 4. The conversion ratio of an ideal transformer m and the internal resistance R_{SC} are derived by employing the instantaneous models of the proposed cross-connected converter shown in Fig. 5 to Fig. 8. In these figures, we postulate the switches S_1 and S_2 as an ideal switch with on-resistance R_{on} . In State- T_j ($j=1, 2$) of Fig. 5 to Fig. 8, the electric charge $\Delta q_{T_j}^{kN}$ in C_{kN} ($k, N=1, 2$) satisfies

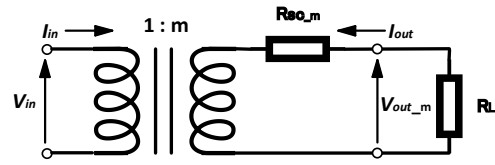


Fig. 4. Equivalent model of the inductor less DC-AC inverter.

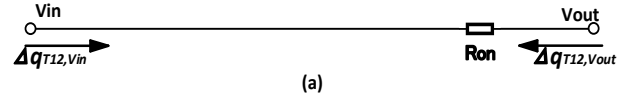


Fig. 5. Instantaneous models of the proposed cross-connected inverter: State- T_1 and T_2 of voltage gain 1.

$$\Delta q_{T_1}^{kN} + \Delta q_{T_2}^{kN} = 0 \quad (7)$$

because the electric charge in C_{kN} does not increase and decrease during one cycle.

In (7), the interval of T_1 , T_2 , and T is set to satisfy

$$T = T_1 + T_2 \quad \text{and} \quad T_1 = T_2 = T/2 \quad (8)$$

In this analysis, we estimate the output voltage and output efficiency corresponding to each the voltage gain. When the voltage gain is 1, in the input/output terminals of Fig. 5, the electric charges, $\Delta q_{T_1,Vin}$, $\Delta q_{T_1,Vout}$, $\Delta q_{T_2,Vin}$ and $\Delta q_{T_2,Vout}$, satisfy

$$\begin{aligned} \Delta q_{T_1,Vin} &= -\Delta q_{T_1,Vout}, \\ \Delta q_{T_1,Vout} &= -\Delta q_{T_1,Vin}, \\ \Delta q_{T_2,Vin} &= -\Delta q_{T_2,Vout}, \\ \Delta q_{T_2,Vout} &= -\Delta q_{T_2,Vin}. \end{aligned} \quad (9)$$

Equation (9) can be obtained by Kirchhoff's law. Using (9), we can express the average input/output currents, I_{in} and I_{out} , as

$$\begin{aligned} I_{in} &= \Delta q_{Vin}/T = (\Delta q_{T_1,Vin} + \Delta q_{T_2,Vin})/T, \\ I_{out} &= \Delta q_{Vout}/T = (\Delta q_{T_1,Vout} + \Delta q_{T_2,Vout})/T. \end{aligned} \quad (10)$$

In (10), Δq_{Vin} and Δq_{Vout} denote electric charges in V_{in} and V_{out} , respectively. Substitute (7)–(9) into (10) becomes

$$\begin{aligned} I_{in} &= -I_{out}, \\ \Delta q_{Vin} &= -\Delta q_{Vout}. \end{aligned} \quad (11)$$

From (11), the conversion ratio m is derived as 1.

Next, in order to derive R_{SC} of Fig. 4, we discuss the total consumed energy $W_{T,1}$ of Fig. 4. In Fig. 5, only the on-resistance R_{on} consumes energy. Accordingly, we can express $W_{T,1}$ as

$$W_{T,m} = 2W_{T,1,m}, \quad (12)$$

where

$$W_{T,1,1} = R_{on}(\Delta q_{T_1,Vout})^2/T_1. \quad (13)$$

In (12) and (13), $W_{T,1,1}$ is the consumed energy of Fig. 5 during T_1 . Substitute (7)–(9) and (12) into (13) becomes

$$W_{T,1} = R_{on}(\Delta q_{Vout})^2/T \quad (14)$$

Since $W_{T,1}$ of Fig. 4 is expressed by

$$W_{T,1} = R_{SC,1}(\Delta q_{Vout})^2/T \quad (15)$$

we get $R_{SC,1} = R_{on}$. Here, it is known that Fig. 4 can be expressed by the K-matrix. Therefore, we obtain the power efficiency η_1 and the output voltage $V_{out,1}$ as

$$\eta_1 = R_L/(R_L + R_{on}),$$

$$V_{out,1} = \{R_L/(R_L + R_{on})\}V_{in}. \quad (16)$$

Similarly, the above calculations are performed for the case of each voltage gain (2, 3 and 4).

When the voltage gain is 2, in the input/output terminals of Fig. 6 (a), the electric charges, $\Delta q_{T1,vin}$ and $\Delta q_{T1,vout}$, satisfy

$$\begin{aligned} \Delta q_{T1,vin} &= \Delta q_{T1}^{11} - \Delta q_{T1}^{21}, \\ \Delta q_{T1,vout} &= \Delta q_{T1}^{21} + \Delta q_{T1}^{22}, \\ \Delta q_{T1}^{11} &= -\Delta q_{T1}^{21}, \\ \Delta q_{T1}^{22} &= 0. \end{aligned} \quad (17)$$

On the other hand, in the input/output terminals of Fig. 6 (b), $\Delta q_{T2,vin}$ and $\Delta q_{T2,vout}$, satisfy

$$\begin{aligned} \Delta q_{T2,vin} &= \Delta q_{T2}^{21} - \Delta q_{T2}^{11}, \\ \Delta q_{T2,vout} &= \Delta q_{T2}^{11} + \Delta q_{T2}^{12}. \end{aligned} \quad (18)$$

Substitute (17) and (18) into (10) becomes

$$\begin{aligned} I_{in} &= -2I_{out}, \\ \Delta q_{vin} &= -2\Delta q_{vout}. \end{aligned} \quad (19)$$

From (19), the conversion ratio m is derived as 2.

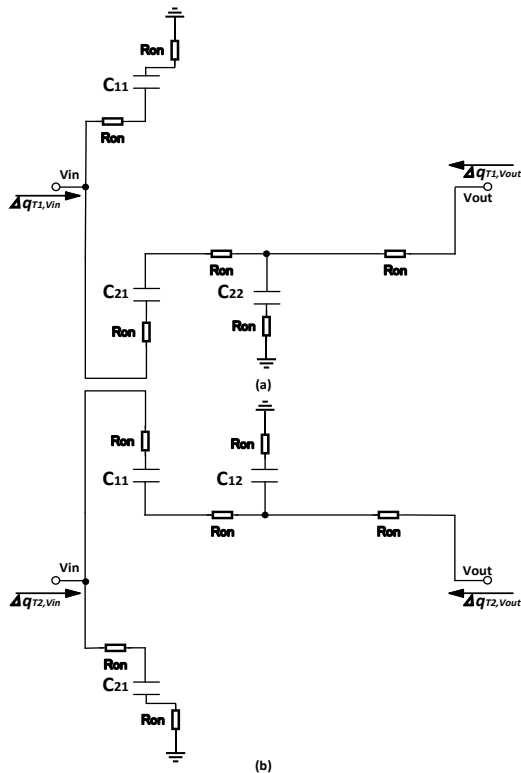


Fig. 6. Instantaneous models of the proposed cross-connected inverter: (a) State- T_1 of voltage gain 2, (b) State- T_2 of voltage gain 2.

Next, we discuss the total consumed energy $W_{T,2}$ of Fig. 4 of voltage gain 2. Accordingly, we can express $W_{T1,2}$ as

$$W_{T1,2} = \{ 2R_{on}(\Delta q_{T1}^{11})^2 + 2R_{on}(\Delta q_{T1}^{21})^2 + R_{on}(\Delta q_{T1}^{22})^2 + R_{on}(\Delta q_{T1}^{21} + \Delta q_{T1}^{22})^2 \} / T_1. \quad (20)$$

Substitute (7), (8), (12), (17) and (18) into (20) becomes

$$W_{T,2} = 5R_{on}(\Delta q_{Vout})^2/T \quad (21)$$

From (21), we can get $R_{SC,2} = 5R_{on}$. Therefore, the power efficiency η_2 and the output voltage $V_{out,2}$ are expressed as

$$\eta_2 = R_L/(R_L + 5R_{on}),$$

$$V_{out,2} = \{R_L/(R_L + 5R_{on})\}2V_{in}. \quad (22)$$

When the voltage gain is 3, in the input/output terminals of Fig. 7 (a), the electric charges, $\Delta q_{T1,vin}$ and $\Delta q_{T1,vout}$, satisfy

$$\begin{aligned} \Delta q_{T1,vin} &= \Delta q_{T1}^{11} - \Delta q_{T1}^{12} - \Delta q_{T1}^{21}, \\ \Delta q_{T1,vout} &= \Delta q_{T1}^{12}, \\ \Delta q_{T1}^{11} &= -\Delta q_{T1}^{21}, \\ \Delta q_{T1}^{12} &= \Delta q_{T1}^{21}. \end{aligned} \quad (23)$$

On the other hand, in the input/output terminals of Fig. 7 (b), $\Delta q_{T2,vin}$ and $\Delta q_{T2,vout}$, satisfy

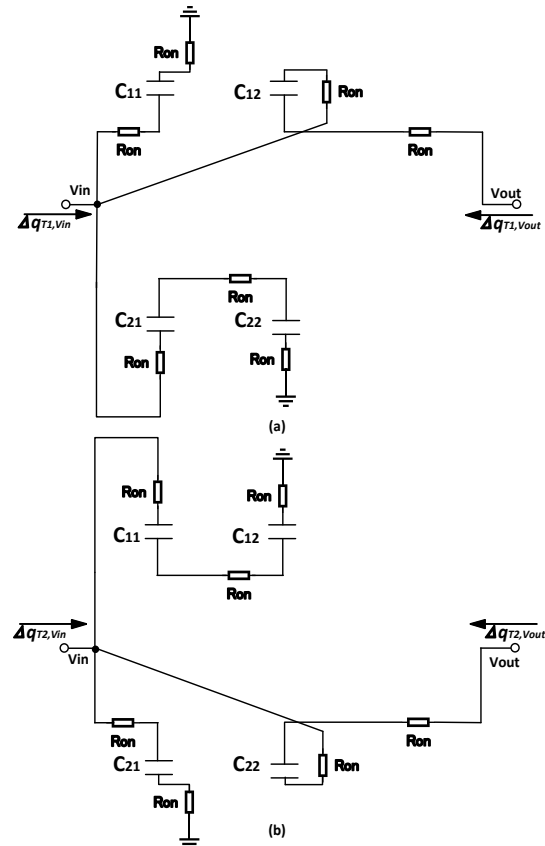


Fig. 7. Instantaneous models of the proposed cross-connected inverter: (a) State- T_1 of voltage gain 3, (b) State- T_2 of voltage gain 3.

$$\begin{aligned}\Delta q_{T2,Vin} &= \Delta q_{T2}^{21} - \Delta q_{T2}^{22} - \Delta q_{T2}^{11}, \\ \Delta q_{T2,Vout} &= \Delta q_{T2}^{22}.\end{aligned}\quad (24)$$

Substitute (23) and (24) into (10) becomes

$$\begin{aligned}I_{in} &= -3I_{out}, \\ \Delta q_{Vin} &= -3\Delta q_{Vout}.\end{aligned}\quad (25)$$

From (25), the conversion ratio m is derived as 3.

Next, we discuss the total consumed energy W_{T_3} of Fig. 4 of voltage gain 3. Accordingly, we can express $W_{T_{1_3}}$ as

$$\begin{aligned}W_{T_{1_3}} &= \{2R_{on}(\Delta q_{T1}^{11})^2 + \\ &2R_{on}(\Delta q_{T1}^{12})^2 + 3R_{on}(\Delta q_{T1}^{21})^2\}/T_1\end{aligned}\quad (26)$$

Substitute (7), (8), (12), (23) and (24) into (26) becomes

$$W_{T_3} = 7R_{on}(\Delta q_{Vout})^2/T\quad (27)$$

From (27), we get $R_{SC_3} = 7R_{on}$. Therefore, the power efficiency η_3 and the output voltage V_{out_3} are expressed as

$$\begin{aligned}\eta_3 &= R_L/(R_L + 7R_{on}), \\ V_{out_3} &= \{R_L/(R_L + 7R_{on})\}3V_{in}.\end{aligned}\quad (28)$$

When the voltage gain is 4, in the input/output terminals of Fig. 8 (a), the electric charges, $\Delta q_{T1,Vin}$ and $\Delta q_{T1,Vout}$, satisfy

$$\begin{aligned}\Delta q_{T1,Vin} &= \Delta q_{T1}^{11} - \Delta q_{T1}^{21}, \\ \Delta q_{T1,Vout} &= \Delta q_{T1}^{12},\end{aligned}$$

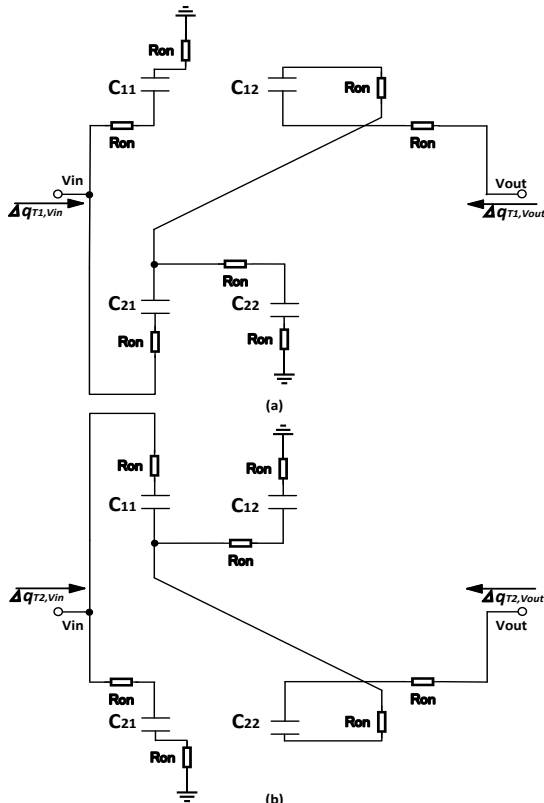


Fig. 8. Instantaneous models of the proposed cross-connected inverter: (a) State- T_1 of voltage gain 4, (b) State- T_2 of voltage gain 4.

$$\Delta q_{T1}^{11} = -\Delta q_{T1}^{21},$$

$$\Delta q_{T1}^{22} = \Delta q_{T1}^{12} - \Delta q_{T1}^{21},$$

$$\Delta q_{T1}^{12} = \Delta q_{T1}^{21}/2.\quad (29)$$

On the other hand, in the input/output terminals of Fig. 8 (b), $\Delta q_{T2,Vin}$ and $\Delta q_{T2,Vout}$, satisfy

$$\Delta q_{T2,Vin} = \Delta q_{T2}^{21} - \Delta q_{T2}^{11},$$

$$\Delta q_{T2,Vout} = \Delta q_{T2}^{22}.\quad (30)$$

Substitute (29) and (30) into (10) becomes

$$I_{in} = -4I_{out},$$

$$\Delta q_{Vin} = -4\Delta q_{Vout}.\quad (31)$$

From (31), the conversion ratio m is derived as 4.

Next, we discuss the total consumed energy W_{T_4} of Fig. 4 of the voltage gain 4. Accordingly, we can express $W_{T_{1_4}}$ as

$$\begin{aligned}W_{T_{1_4}} &= \{2R_{on}(\Delta q_{T1}^{11})^2 + R_{on}(\Delta q_{T1}^{21})^2 + \\ &2R_{on}(\Delta q_{T1}^{22})^2 + 2(\Delta q_{T1}^{21})^2\}/T_1.\end{aligned}\quad (32)$$

Substitute (7), (8), (12), (29) and (30) into (32) becomes

$$W_{T_4} = 16R_{on}(\Delta q_{Vout})^2/T\quad (33)$$

From (33), we can get $R_{SC_4} = 16R_{on}$. Therefore, the power efficiency η_4 and the output voltage V_{out_4} are expressed as

$$\begin{aligned}\eta_4 &= R_L/(R_L + 16R_{on}), \\ V_{out_4} &= \{R_L/(R_L + 16R_{on})\}4V_{in}.\end{aligned}\quad (34)$$

As you can see from (16), (22), (28) and (34), R_{SC_m} is the important factor for η_m and V_{out_m} .

IV. CHARACTERISTIC COMPARISON

Table I summarizes the number of circuit components in the case of 9 steps. As you can see from Table I, the proposed inverter is the smallest of the traditional inverter. Unlike conventional inverters, the proposed inverter does not require large number of components, because this circuit has small components by cross-connected topology.

TABLE I. COMPARISON OF THE NUMBER OF COMPONENTS

Inverter topology	Circuit components	
	Switch	Capacitor
Proposed inverter	17	4
SC-type inverter [6]	26	6
Fibonacci-type inverter [10]	22	4

V. SIMULATION RESULT

The validity of the discussion in Sections III is confirmed by comparing theoretical results with simulation results. Using the SPICE simulator, the comparison was performed under the conditions shown in Table II. The simulated power efficiency and output voltage are shown in Fig. 9. As you can see from Fig. 9,

the theoretical results agree well with the SPICE simulation results.

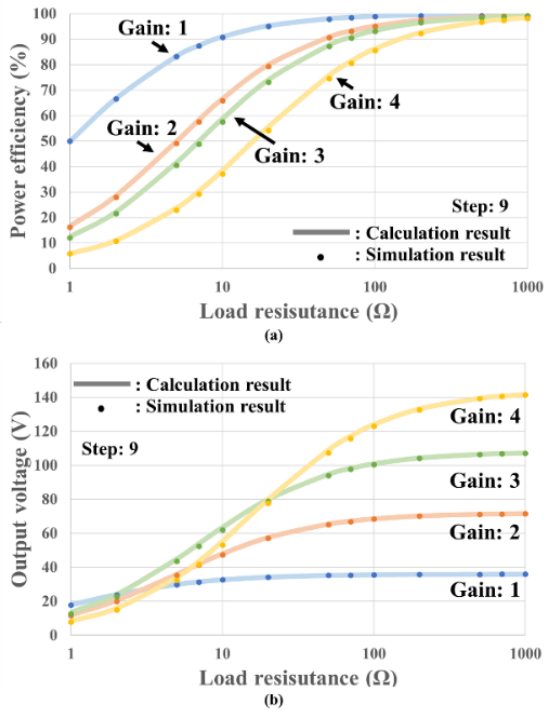


Fig. 9. Comparison of theoretical calculation and simulation of each voltage gain: (a) power efficiency according to the load resistance (b) output voltage according to the load resistance.

TABLE II. SIMULATION CONDITIONS OF THEORETICAL ANALYSIS

Parameters	Value
Input voltage V_{in}	36 V
On-resistance R_{on}	1 Ω
Operating frequency	10 kHz
Main capacitor $C_{1,1} = \dots = C_{2,3}$	33 μ F

Next, the comparison of traditional inverters and the proposed inverter was performed under the conditions shown in Table III. The simulated output voltage waveforms are shown in Fig. 10. As Fig. 10 shows, the multilevel output with 9 steps was generated by the proposed inverter. The simulated power efficiency and output voltage are shown in Fig. 11. In Fig. 11 (a), the proposed inverter has the highest efficiency of the traditional inverter when output power is between 1W to 60W. It has higher efficiency 2~ 75% than the traditional inverter [6] when output power is between 1W to 60W. At same time, the proposed inverter was achieved as high output voltage about 105V as the traditional inverter [6] when output power is between 1W to 60W in Fig. 11 (b).

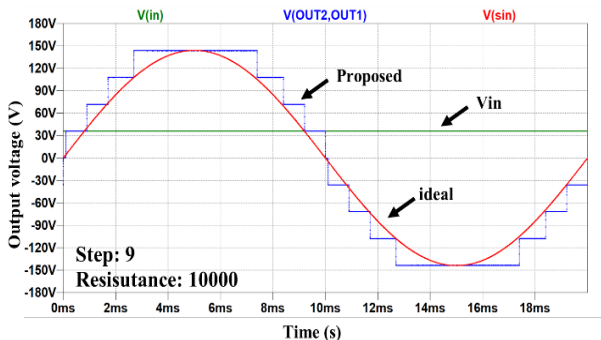


Fig. 10. Simulated output voltage waveforms.

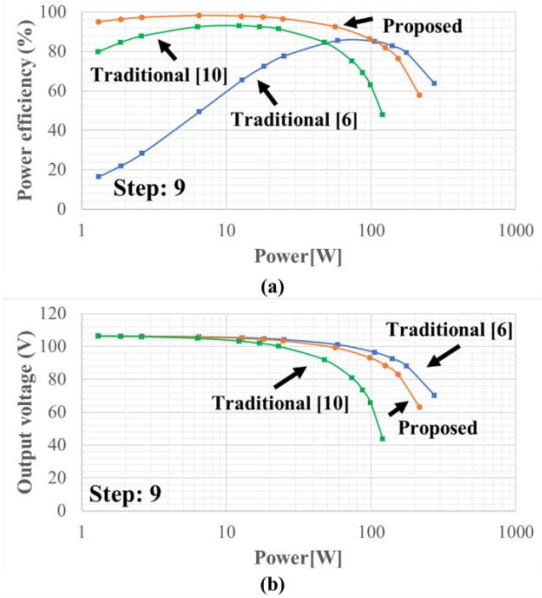


Fig. 11. Comparison of simulation result: (a) power efficiency according to the output power and (b) output voltage according to the output power.

TABLE III. SIMULATION CONDITIONS FOR COMPARISON

Parameters	Value
Input voltage V_{in}	36 V
On-resistance R_{on}	1 Ω
Operating frequency	10 kHz
Main capacitor $C_{1,1} = \dots = C_{2,3}$	33 μ F

VI. SUMMARY

In this paper, we have proposed a small DC-AC inverter with cross-connected charge pumps. The theoretical analysis and SPICE simulations revealed the following. 1) The proposed inverter realizes the same multilevel output as the traditional SC inverter by a small number of circuit components. 2) The proposed inverter improves 2% ~ 75% power efficiency from the traditional inverter when output power is between 1 to 60W.

The future enhancement of this work is to integrate the proposed cross-connected inverter into an IC chip and investigate the characteristics experimentally. The integrated inverter will be used for digital cameras, AV equipment, etc.

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