# FPGA Based Design and Implementation of DUC/DDC Based OFDM for Data/Image Transmission

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***Abstract*—The tremendous growth in the wireless communication system demands a very high-speed data transmission with better quality of service. The Orthogonal Frequency Division Multiplexing (OFDM) provides high-speed data communications by utilizing the spectrum more significantly than other approaches including Frequency Division Multiple Access (FDMA). Most of the OFDM transceiver architectures with different algorithms for wireless communication are conventionally used along with software-based approaches which are not suitable for real-time scenarios in Radio Frequency (RF) systems. There is no complete standard benchmark or prototyped hardware architecture for OFDM based RF systems. Very few existing designs are available with hardware overhead issues. In this paper, the proposed OFDM system offers low cost hardware architecture which includes Quadrature Amplitude Modulation (QAM) modulation-demodulation, highly pipelined Inverse Fast Fourier Transform (IFFT)- Fast Fourier Transform (FFT) modeling along with digital conversion systems like Direct Up-Conversion (DUC) and Direct-Down-Conversion (DDC), which supports the RF systems for real-time requirements. The proposed OFDM systems support both data and image for transmission. The design is synthesized in Xilinx platform and simulated using Model-sim and prototyped on Artix 7 FPGA board. The proposed OFDM system is compared with existing similar architecture on the same FPGA device with hardware constraints improvements.**

***Index Terms*—DUC, DDC, FFT Model, FPGA, modulation, OFDM, RF system**

## I. Introduction

The enormous growth in the wireless multimedia communication demands the necessary data transmission at higher speed [1]. The current telecommunication industries are providing different services from voice to multimedia data transmission, where the communication speed ranges from Kbps to Mbps [2]. To fulfill the demand of high-speed communication many of the techniques were introduced, among which Multicarrier Modulation (MM) is widely used for data transmission [3]. The multicarrier modulation technique divides the high rated data bit streams into different parallel Low Data Bit Streams (LDBS) and these data helps in the modulation of many carriers [4]. The multicarrier transmission holds the important properties like delay spread tolerance and spectral efficiency. The OFDM (orthogonal frequency division multiplexing) is a kind of MM which can be used as an emerging technology for both wired and wireless communication. The recent research trend has addressed that OFDM has gained popularity among the broadband community [5]. OFDM is widely considered for many communication protocols because of significant properties of OFDM over the conventional Frequency Division Multiplexing (FDM). During transmission, OFDM transforms a frequency selective wideband channel to a cluster of nonselective narrowband channels by maintaining the orthogonality in the frequency domain [6]. The OFDM system engages with two key points Fast Fourier Transform (FFT) and inverse FFT (IFFT). The FFT algorithm is used to evaluate the Discrete Fourier Transform (DFT) that transforms the data from the time domain to the frequency domain. The inverse FFT performs the reverse transformation of data, i.e., from the frequency domain to the time domain [7].

The hardware implementation of FFT or IFFT mechanisms is the biggest concern. The Digital Signal Processing (DSP) and field-programmable gate array (FPGA) chips are considered as the design environments for implementation of different FFT schemes [8]. The fast processing nature of Very-Large-Scale Integration (VLSI) technology suggested the use of FPGA which offers the complete environment of Programmable System-on-Chip (PSoC) [9]. The FPGA includes thousands of logic gates and configurable logic blocks that make a meaningful solution for prototyping the Application-Specific Integrated Circuit (ASIC) with dedicated architectures for specified DSP applications [10].

The OFDM is a modulation scheme which exhibits a multicarrier transmission mechanism. The OFDM performs the division of spectrum into abundant carriers, and each carrier will be modulated at lower data rates. The OFDM is analogous to FDM, but it is spectrally efficient by positioning the sub-channels much nearer

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together. The positioning of sub-channels is done by selecting the frequencies which are orthogonal and by letting each spectrum sub-channel to overlay another without interfering with it. The OFDM performs the splitting of the bandwidth as narrowband channels with its sub-carrier which are made orthogonal to each other. This helps to overcome overhead carrier spacing issues of Frequency Division Multiple Access (FDMA). The OFDM is a multi-carrier transmission mechanism that divides various spectrums into a various number of the carrier, and each of these carriers will be modulated with the low rate data stream. The OFDM exhibits the same properties like FDMA where the access to multiple users can be attained by subdividing the available bandwidth to multiple channels which are then allocated to desired users. The OFDM uses the spectrum efficiently by spacing channels more closely together. This can be attained by keeping all the carriers orthogonal to each other, preventing interference among the closely spaced carriers [11]-[14].

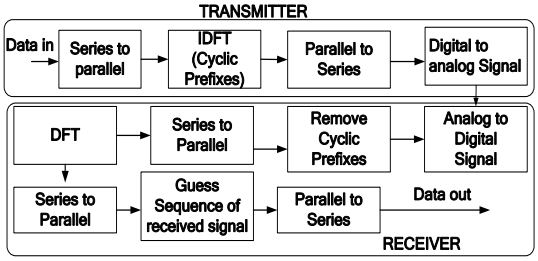


Fig. 1. Transmitter and receiver of OFDM.

Fig. 1 indicates the model of the OFDM transmitter and receiver. The transmitter changes from serial to parallel and then applies the Inverse Discrete FOURIER Transform (IDFT) adds a cyclic prefix and then convert it back to parallel to serial. Later on, the signal is converted to analog from digital [15].

The receiver does the reverse operation of the transmitter, in which it converts the analog signal into digital (represented in Fig. 4). Later it performs the elimination of cyclic prefixes and conversion of received signals as a parallel from serial. Then it applies the DFT and guesses the sequence of the received signal. Finally performs the conversion of the signal as serial one.

**Significance:** The OFDM has much significance [16], [17] than other modulation mechanisms and are discussed below:

- The *bandwidth efficiency* is the main aspect of high-speed communication. In wireless communication, the bandwidth can be shared by all the devices expected to share the full range of carrier channels. Due to the orthogonality nature of OFDM, it reduces the 50% of the total bandwidth.
- The inter symbol interference causes a problem in *high data rate transmission*. The OFDM helps to transmit with at high speed.

The OFDM helps to spreads a frequency selective fade over the symbol. The OFDM effectively randomizes the burst errors caused by deep fade or impulse interferences.

The major challenge for the research community is to deal with the optimization of VLSI circuit in terms of area and time. The existing conventional techniques involve pipelining, re-timing, parallel processing, etc., while non-conventional techniques involve evolutionary and genetic algorithms Cartesian genetic programming and genetic programming. This paper introduces an FPGA based optimized OFDM transceiver design. The performance of the proposed system is compared with the existing system to declare the effectiveness of the proposed system.

The paper is organized with following sections like a review of most relevant existing research survey in Section II and problem statement in Section III. Section IV discusses the design and implementation of the proposed system. The next Section V presents the obtained results analysis. Finally, Section VI concludes paper contribution with the conclusion.

## II. Related Work

This section discusses the recent tries in the design and implementation of the OFDM transmission system by using the FPGA concept. The work of Ganesh *et al*. [18] introduced the concept of designing of OFDM transmission and implementation of FPGA using Simulink on FPGA. This system has got an efficient and simple hardware interface. The outcomes were verified using Spartan3E FPGA and found effective for the transmitter and receiver design. The work of Mohamed *et al*. [19] discussed the design and the implementations of OFDMA were illustrated by using MATLAB. The design considered various parameters for system performance. Author implemented the OFDM transceiver over FPGA Spartan 3A kit and found effective results. Similar work was performed by Mev *et al*. [20] for OFDM transmitter and receiver design using FPGA. Author has used Altera modelsim for simulation and implemented Verilog with radix2 point decimation under frequency FFT and IFFT. The extensive research toward the implementation of IFFT for transmitter and receiver design of OFDM in Bhavani *et al*. [21]. The author used 8-point IFFT with radix-2 and implemented FPGA based HDL. The simulation and synthesis were performed using Xilinx ISE tools. The implementation of the FFT algorithm for OFDM transceiver was presented in Kaur *et al*. [22]. The system design was optimized one for the area and speed was concerned. The outcomes suggest that the system achieves higher speed and low area. The work introduced by Sawant *et al*. [23] discussed the study on the transmitter and receiver of OFDM. The design was implemented over Spartan 3A kit and used VHDL language system. The outcomes gave the optimized and efficient results. The work introduced by Pechetty *et al*. [24] presented a reconfigurable platform for OFDM transmitter and receiver. This has given the transceiver implementation and validation of OFDM transceiver over FPGA which is purely digital and found low cost and simple in programming. The work introduced by Gautham *et al*. [25] worked on DUC/DDC/DWT based OFDM and implemented through FPGA Verilog code and Hardware utilization. Based on the analysis of current research trend following problem is found.

The implementation of software for baseband communication in OFDM transceiver system was failed to have better performance and low latency. Thus, a work of Pham *et al*. [26] has presented an OFDM transceiver model by using partial reconfiguration of FPGA and achieved latency in the reconfiguration of OFDM. Similarly, Korrai *et al*. [27] have considered FPGA for channel estimation along with orthogonality matching pursuit mechanism for OFDM and improved system performance. A recent work of Bruno *et al*. [28] have presented a variable length FFT for OFDM system and considered FPGA implementation through which [28] have achieved higher throughput.

## III. Problem Statement

The design of OFDM always demands a comprehensive and complete understanding and selection of critical parameters as the design is of no exception which deals with significant features. The significant feature of OFDM is that it decreases the data rate at the subcarrier level by which the symbol duration increases and hence the multipath are effectively eliminated. This leads to higher Cyclic Prefix (CP) providing important outcomes but causes higher energy losses. Thus, there a need for proper OFDM concept [29]. For the same concern, various researchers are introduced to different OFDM transceiver systems by implementing the different algorithms to have significant digital communication in a conventional manner [30]. From the survey analysis of current research trend in OFDM, it is found that most of the mechanisms follow the software-based designs which are not meant for real-time application areas in Radio Frequency (RF) systems, wireless communications, etc. It is also found that there are few standard architectures are presented for hardware prototyping. These hardware architectures are designed for OFDM systems and are lags with designs constraints like area overhead, power consumption and hardware complexity up to the standards in real-time applications.

## IV. Proposed System

In order to bring effectiveness in the conventional RF communication system, an optimized OFDM transceiver system is designed by using Verilog-HDL over FPGA. The block diagram of the OFDM transceiver system is represented in Fig. 2, which consists of both the transmitter and receiver units. The transmitter unit composed of main blocks like QAM modulation, a symbol generation module, zero padding, IFFT module, and cyclic prefix module, Primary Input and Secondary Output (PISO) register, Digital Up Conversion (DUC). The receiver unit follows the reverse process of the transmitter unit, i.e., it exhibits the inverse cyclic prefix module, FFT module, inverse zero padding, inverse symbol generation, and QAM demodulation. The transmitter unit considers the input of 4bit binary data for QAM modulation which helps to modulate the carrier frequency signal and generates the In-phase Quadrature (IQ) signals using consolation mapping. The QAM modulation provides the output signal of 16bits and is subjected to Symbol Generation Module (SGM). The SGM increases the symbol for IFFT operation with the help of shift registers. The SGM gives the output of 64bits signal and is subjected to Zero Padding (ZP). The ZP adds the zero symbols to enhance the number of samples. The ZP leads the output of 128-bits data and is given to IFFT. The proposed study implements the pipelined 8point 16bit architecture. Then it is forwarded to Cyclic Prefixes (CP) that prefixes the carriers and removes the ISI. The output of CP generates the output of 304bits and is subjected to PISO which converts the parallel stream input of 304 bits into the serial output of 16bits. This output is subjected to DUC to forward it to the channel. This channel is transmitted to the receiver unit which does the reverse operation illustrated above and gives the output data.

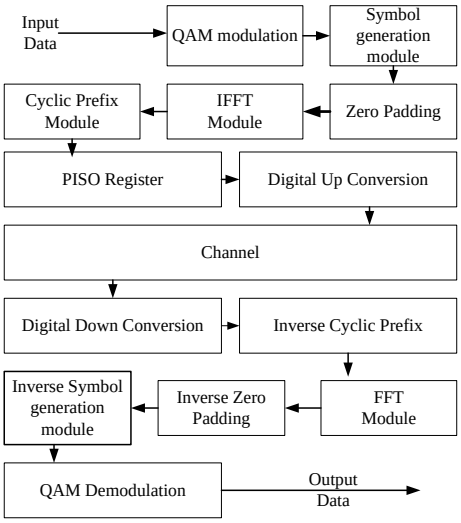


Fig. 2. The architecture of proposed DUC/DDC based OFDM system.

***Transmitter:*** For this design, the clock frequency is adjusted to 100 MHz to perform the division of global clock frequency and gives the moderate clock as transceiver module. In QAM modulation, two carriers wave exist of same frequency which changes the phase of 90 degrees. In this system, 16 QAM modulation approach is used which exhibits 4 inputs and provides 16-bit quadrature phase signal data. The signal generation module receives the 16-bit data and generates 64-bit symbol data. The zero padding provides the output of 128-bit real and imaginary sample data. The IFFT modules decomposed the zero padded output data into 16-bit data from LSB to MSB format 8 times and stored in 8-bit, so total 128-bit symbol data as a real and imaginary data. For cyclic prefix, 48-bit symbols are used for guard band design. The PISO register processes the shifting operation parallel with the counter operation. The main operation of DUC is to the conversion of one or more channels baseband data to pass band data at specified radio frequencies. The DUC module is usually appearing in transmitter side and its counterpart Digital Down Converter (DDC) module in the receiver side. The DUC input signal is sampled at a low sampling rate which comes from PISO register output.

***Receiver:*** This does the reverse operation of the transmitter where DDC generate the cosine (Ac) output. The 16-bit sine and cosine data are generated in the DDC module. In that anyone which is fed to inverse cyclic prefix module which shifts the counter until clock cycle reset to zero. Then the FFT module receives the 128-bit data from inverse cyclic prefix module and decomposes 128-data into eight 16-bit registers. Then inverse zero padding, inverse symbol generation, QAM demodulation.

The proposed RF OFDM transceiver includes the DUC and DDC provides the RF frequency signals to channel and vice versa and which strengthen the overall system in real time scenarios and improves the system performances. The DUC/DDC mainly contains Digital Frequency Synthesizer (DFS) and multiplier modules. The DFS module is used to generate the sine and cosine data based on the input angle. The sine and cosine outputs are multiplied with two separate multipliers to generate the DUC/DDC outputs.

The DFS hardware architecture mainly consists of two multipliers, two adders, two multiplexers, and two data registers is represented in Fig. 3. The inputs Ai, Bi, angle, output sine, and cosine are 16-bits wide. If we increase the size the data elements like inputs and output, hardware resource utilization will also increase. Initially, all the hardware elements reset to zero. Ai and Bi are fed to multiplexers when select is high, so the current values of Bc and Ac are sine and cosine values respectively. When clock is activated on the rising edge of a clock, registers stores the current value of Bc, Ac in next clock cycle, by that time select becomes low. When select is low in next clock cycles multiplexers acts as wires throughout the design process. Registers release the Bp, Ap values which are acts previous values of sine and cosine respectively. The previous value (Bp) of sine is multiplied by angle input $\theta$ and added with previous value (Ap) of cosine. After multiplexing it generates the current value of cosine (Ac). Similarly, the previous value (Ap) of cosine is multiplied by angle input $\theta$ and added with previous value (Bp) of sine. After multiplexing it generates the current value of sine (Bc).

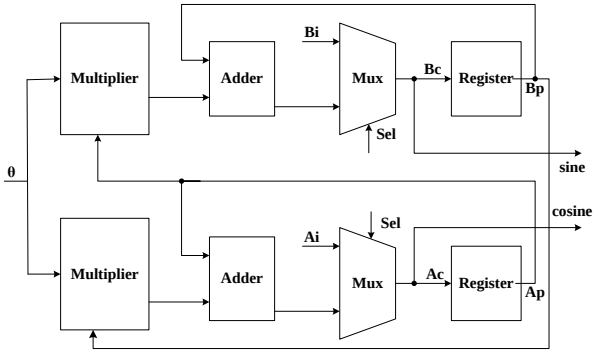


Fig. 3. The hardware architecture of DFS.

The proposed RF OFDM transceiver block diagram is presented as shown in Fig. 4. At the transmitter side, the digital input data is passed serially into the QAM modulator from which QAM symbols are generated. The IFFT block takes *N* input symbols and modulates it into *N* orthogonal subcarriers and generates an OFDM signal which is the sum of *N* subcarriers. A cyclic prefix code is added to the OFDM signal to overcome the intra-symbol and inter-symbol interference effects. The DUC block performed the up-conversion to RF frequencies and passed through a channel.

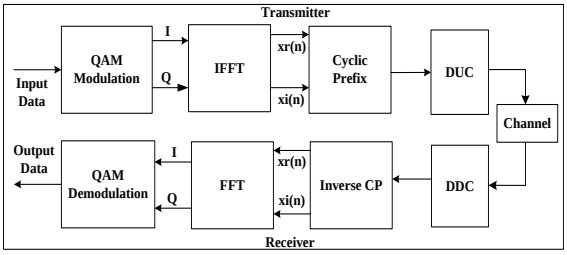


Fig. 4. Proposed RF OFDM block diagram.

At the receiver side, the DDC block performs the down-conversion of the RF signals to get the OFDM signal. The FFT block transforms the OFDM signal into *N* QAM symbols which will be demodulated to get the original input data. The methodology starts with an initial design of an OFDM based RF transceiver system which is then simulated. The simulation results are then used for comparison with the existing system. Two comparisons are made here 1) The simulation results of the FFT system designed are compared with the MATLAB FFT computation and 2) The proposed OFDM RF transceiver system is compared with the existing OFDM RF transceiver system.

## V. Result Analysis

The OFDM transceiver module is mainly contained transmitter, receiver, DUC and DDC modules. The clock frequency is set to 100 MHz to perform the division of global clock frequency and gives the moderate clock as transceiver module. The design is synthesized in Xilinx 14.7 ISE using Verilog and simulated using Modelsim6.3f and implemented over Artix7 FPGA board. A device is 7A100T-3 CSG324. The clock is toggling at every 10 ns; the asynchronous reset is initially high to reset the process. Then make it low. The valid_i is always high in all the stages. The input data is data_in =1011, and output data is data_out is generated same as input after all the process done. The following Fig. 5 represents the simulation outcomes obtained from the modelsim-6s simulator.

The proposed design uses IFFT-FFT based transmitter and receiver modules. The proposed design is compared with a similar model [30] which uses lifting based DWT on OFDM systems. The intention is that FFT based OFDM is better in terms of Area and power utilization. The number of occupied slices and number of slices LUT's are improved with 33.88 % and 28.84 % with respect to [30] in terms of area utilization as shown in Table I and Fig. 6.

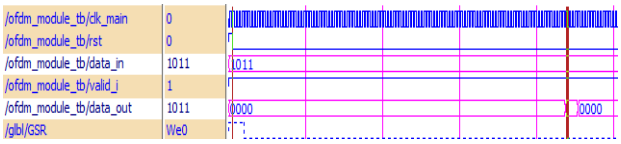


Fig. 5. OFDM transceiver simulation results.

TABLE I. AREA UTILIZATION COMPARISON OF WHOLE OFDM SYSTEMS WITH [30]

| Area utilization | Previous [30] | Proposed | Improvements |
|---|---|---|---|
| Number Slices | 3491 | 2308 | 33.88% |
| Slice LUT's | 9620 | 6845 | 28.84% |

Table II shows the total power utilization with an improvement of 41.24%. Hence it reduces the hardware complexity in the chip.

The proposed system is also compared with the system presented by a similar system [31] which is a lifting-based DWT for OFDM. Here, the area is considered as the main parameter for comparison with resource utilization of the proposed system and similar to [31]. The outcomes of the proposed system and previous [31] are tabulated in Table III. From the Table III, found that the LUT Flip-flop pairs, Slice Flip-flops and DSP48E's are improved with 16.50%, 62.93%, and 89.16% respectively. Fig. 7 gives the graphical representation of whole OFDM area utilization which indicates the improvement of the proposed system.

The proposed work is compared with similar architecture [32] using Spartan 6 FPGA is tabulated in Table IV. The logic utilization is improved than the previous work with respect to Slice registers, Buffers, and DSP elements.

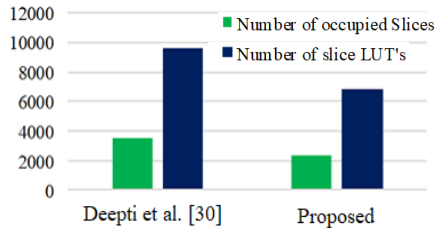


Fig. 6. Comparative analysis of area utilization.

TABLE II. ANALYSIS OF POWER CONSUMPTION

| Power Utilization | Previous [30] | Proposed | Improvements |
|---|---|---|---|
| Total Power | 1.879W | 1.104W | 41.24% |

TABLE III. AREA UTILIZATION COMPARISON OF WHOLE OFDM SYSTEMS WITH [31]

| Area utilization | Previous [31] | Proposed | Improvements |
|---|---|---|---|
| LUT FF pairs | 9173 | 7659 | 16.50% |
| Slice FF | 6006 | 2226 | 62.93% |
| DSP48E's | 240 | 26 | 89.16% |

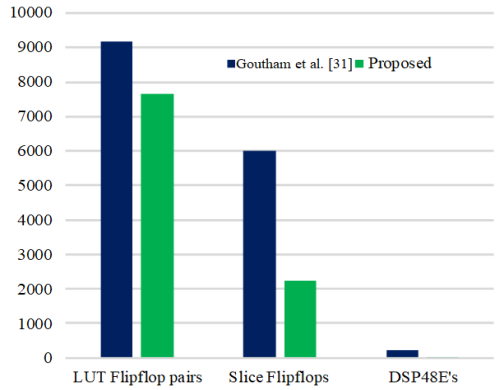


Fig. 7. Comparative analysis plot of proposed and previous [31].

TABLE IV. COMPARISON OF AREA UTILIZATION FOR FFT MODEL

| Logic Utilization | Previous [32] | Proposed |
|---|---|---|
| Slice registers | 25650 | 2497 |
| BUFG/BUFGCTRs | 9 | 5 |
| DSP48A1s | 52 | 34 |

TABLE V. COMPARISON OF AREA UTILIZATION FOR FFT MODEL

| Area Utilization | Previous FFT [33] | Proposed-FFT | Overhead |
|---|---|---|---|
| Slices | 3155 | 871 | 72.39% |
| 4 input LUTs | 5916 | 1688 | 71.46% |
| Mult18x18s | 16 | 8 | 50% |

The area utilization proposed FFT system is done with the existing work towards FFT design of previous [33] by considering the device utilization components like No. of slice, No. of four input LUTs, No. of Multi18x18s and No. of clocks (GCLKs) and is given in Table V. The proposed design uses Pipelined 8-point 16-bit FFT architecture. The slices and 4-input LUT's are improved with 72.39 % and 71.46 % respectively with respect to previous FFT system [33].

Thus, from the above outcomes found that the proposed system, achieved with less area overhead, total power reduction and less hardware complexity of the OFDM systems on FPGA Chip.

## VI. CONCLUSION

The recent vast developments in communication have allowed multimedia communication to demand the necessary data transmission at higher speed. The challenge with optimization of VLSI circuit in terms of area and time. The existing conventional techniques involve pipelining, re-timing, parallel processing, etc., while non-conventional techniques involve evolutionary and genetic algorithms Cartesian genetic programming and genetic programming. Thus to provide high-speed data communication in real time RF system, this paper presents the OFDM Transceiver module is mainly contains transmitter, receiver, DUC and DDC modules. The outcomes suggest that the number of occupied slices and number of slice LUT's are improved with 33.88 % and 28.84 % with respect to [30]. The proposed design uses pipelined 8-point 16-bit FFT Architecture, and the slices and 4-input LUT's are improved with 72.39 % and 71.46 % respectively with respect to [33]. The proposed outcomes proposed a system, achieved with less area overhead, total power reduction and less hardware complexity of the OFDM systems on FPGA chip.

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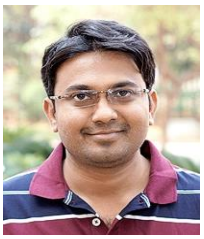

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