13.56 MHz Highly-Efficient Power Conditioning Unit Using an Active Rectifier and LDO for Implantable Medical Devices (IMD)

Rovil S. Berido and Allenn C. Lowaton
Mindanao State University-Iligan Institute of Technology, Microelectronics Laboratory, Iligan City, Philippines
Email: berido.rovilsaga@gmail.com; allenn.lowaton@g.msuint.edu.ph

Abstract—This paper presents a highly-efficient power conditioning unit using 65 nm CMOS technology for inductively-powered Implantable Medical Device (IMD). The unit is comprised of an active rectifier and a low dropout regulator (LDO) which together, provides a stable 3 V (30 mW power) to the IMD (load). The active rectifier is equipped with an integrated offset compensation control in the rectifier comparator. Other published works require off chip signals that are necessary for the comparator to work. This paper has all the comparator components integrated on chip. Operating at 13.56 MHz frequency and with peak input voltage of 3.6V, the rectifier has high power conversion efficiency (PCE) of 90%. The LDO has also a high PCE of 89%. Together, the rectifier and the LDO form a high PCE power conditioning unit for a 30 mW IMD.

Index Terms—active rectifier, LDO, IMD, inductive power transmission, 13.56MHz ISM band

I. INTRODUCTION

An implantable medical device (IMD) which is implanted into the human body depends on an outside power source to operate [1], [2]. Approved IMDs have already adopted wireless power transmission where power is provided from an outside power source to an implanted device without any direct electrical contact in between. Among the few forms of wireless power transmission, inductive power transmission is the most commonly used because of its high-power transfer efficiency (PTE) [3]-[6].

Fig. 1 shows the general structure of an IMD which uses inductive power transmission. It is composed of three components: 1) transmitter (Tx); 2) inductive link and 3) receiver (Rx). The power amplifier (PA) in the Tx unit drives the primary coil, $L_1$, into the carrier frequency $f_c$. This signal is coupled into the secondary coil, $L_2$, of the Rx unit via the inductive link. This then generates the alternating current (AC) voltage, $V_{coil}$, across the resonance circuit $L_2$ and $C_2$. An alternating current to direct current (AC-DC) converter then follows to supply the load of the receiver with the DC output voltage $V_{out}$. A low-dropout regulator (LDO) is used after AC-DC converter to provide a constant DC output voltage. The AC-DC converter can either be a passive rectifier, passive voltage doubler, active rectifier or an active voltage doubler. The AC-DC converter together with the LDO forms the power conditioning unit of the power receiver which are required to have high individual Power Conversion Efficiency (PCE) for the total PTE of the system to be high.

II. DESIGN AND IMPLEMENTATION

Fig. 2 shows the flowchart of the design procedure. Before the actual circuit design, a review of available architectures of rectifier and LDO is done so as provide basis for the schematic design.

Fig. 1. IMD using inductive power transmission

Fig. 2. Flowchart of the design and implementation
A. Active Rectifier

The active rectifier is a full-wave rectifier which composed of two active diodes D1 and D2 as well as a cross-coupled nMOS pair N1 and N2. All the diodes are implemented as active diodes as shown in Fig. 3. In the active diode implementation, pass transistors driven by a high-speed comparator are used to place the operation at the deep triode region in order to achieve low dropout voltages [7]-[9].

During the positive cycle, when \( V_{\text{rec}} > V_{\text{ac}} > V_{\text{in}}(Mn2) \) where \( V_{\text{ac}} = V_{\text{ac}(+) - V_{\text{ac}(-)}} \) the positive feedback operation of M\(_n1\) and M\(_n2\) connects \( V_{\text{ac}(+)} \) to \( V_{\text{ss}} \) through M\(_n2\). In this case M\(_n1\) is turned off. The output of CMP\(_2\) is high since \( V_{\text{rec}} > V_{\text{g}}\text{2} \) and \( V_{\text{g}}\text{2} \) is turned off. As long as \( V_{\text{rec}} < V_{\text{ac}}, M_{p1} \) is off. Now, when \( V_{\text{rec}} < V_{\text{ac}}, \) the output of CMP\(_1\) is low thereby causing M\(_p1\) to turn on. There is now a flow of current from \( V_{\text{ac}(+)} \) to \( V_{\text{rec}} \) thus supplying the load. Meanwhile, during the negative cycle of the input \( V_{\text{ac}}, \) when \( |V_{\text{ac}}| > V_{\text{th}}(Mn2) \), M\(_{sl1}\) connects \( V_{\text{ac}(+)} \) to \( V_{\text{ss}} \) and M\(_{sl2}\) is turned off. As long as \( |V_{\text{ac}}| < V_{\text{rec}}, \) both M\(_{p1}\) and M\(_{p2}\) are turned off. When \( |V_{\text{ac}}| > V_{\text{rec}}, \) CMP\(_2\) turns M\(_{p2}\) on. In this case current flows from \( V_{\text{ac}(-)} \) to \( V_{\text{rec}} \) to supply the load again.

The purpose of auxiliary transistors M\(_b1\) to M\(_b4\), M\(_s2a\) and M\(_s2b\) is to ensure that the body terminals of M\(_p1\) and M\(_p2\) are always connected to the highest potential in the entire circuit. This is to prevent latch up and leakage currents by M\(_p1\) and M\(_p2\) because of the sharp transitions experienced by \( V_{\text{ac}(+)} \) and \( V_{\text{ac}(-)} \)[10], [11].

1) Comparator: Comparators play an important role in increasing the PCE of an active AC-DC converter especially when the operating frequency is as high as 13.56 MHz. Note that the rectifying transistors M\(_{p1}\) and M\(_{p2}\) in Fig. 4 are large devices. As such, when driven by comparators, turn-on and turn-off delay are unavoidable. When these transistors experience turn-on delay, some of the forward conduction time is wasted. On the other hand, when they experience turn-off delay, a reverse current will flow from the load back to the LC tank. In both cases, the PCE of the AC-DC converter is degraded. Hence, there must be some way to compensate for this delay in the comparator so that a high PCE is maintained.

Fig. 4 shows the schematic diagram of the comparator. Transistors M\(_1\) to M\(_4\) form a common-gate amplifier. M\(_1\) and M\(_2\) are set to have non-uniform W/L ratio for turn-on delay compensation. The output of the common-gate amplifier is feed to the tapered buffer composed of M\(_{10}\) to M\(_{15}\) in order to drive M\(_{p1}\) and M\(_{p2}\) of Fig. 4. Turn-off delay compensation is controlled by transistors M\(_{16}\) to M\(_{24}\). Unlike the work in [12], where off chip signals are necessary for the comparator to work, in this paper all comparator components are integrated on chip.

2) Constant gm Current Reference for the Comparator: To supply the bias current of the comparator, a constant gm-current reference is used. Shown in Fig. 5, the main advantage of using this type of current reference circuit is being insensitive to supply variation. This is necessary in order to ensure proper operation of the comparator at the instant where the regulated output voltage is just starting to raise to its peak.

This circuit provides a nearly ideal current to the comparator. The circuit is divided into three parts: the main current reference circuit, the cascade bias circuit and the start-up circuit. The cascade bias circuit generate the proper bias voltage of the main current reference circuit while the start-up circuit will ensure that the main current reference circuit will operate at the desired point. The current reference is provided by M\(_{20}\) for the transistor M\(_{40}\) in order to generate the bias voltages for transistors
M_{32}, M_{33}, and M_{39}. On the other hand, current reference is provided by M_{41} for the transistor M_{37} in order to generate the bias voltages for transistors M_{30}, M_{31}, and M_{38}.

The two power transistors M_{p1} and M_{p2} are simultaneously turned on and off depending on the polarity of the input. For the positive cycle of the input with |V_{in}| > V_{rec}, M_{p1} is conducting. On the other hand, for the negative cycle of the input with |V_{in}| > V_{rec}, M_{p2} is conducting.

Note that the two (2) power transistors of the rectifier are pMOS. Therefore, the output of comparator CMP_{1} must be logic 0 at the positive clock cycle of the input when |V_{in}| > V_{rec}. Likewise, the output of comparator CMP_{2} must be logic 0 at the negative clock cycle of the input when |V_{in}| > V_{rec}. Fig. 8 and Fig. 9 show the output of CMP_{1} and CMP_{2} respectively.

III. RESULTS AND DISCUSSION

A. Rectifier

The actual design of the rectifier starts with the design of the comparator. The primary goal is to turn on and turn off the power transistors at the exact time in order to ensure maximum PCE. To do this the comparator is equipped with turn-on and turn-off compensation circuits in order to compensate for the delay cause by the large gate capacitance of the power transistor. The current reference of the comparator must provide a stable and constant current irrespective of the variation of the supply voltage. Fig. 7 shows the DC analysis of the I_{ref} as supply voltage is swept from 0 to 3.3 V. The I_{ref} value is within 5% of its maximum at supply voltage equal to 1.44 V, 1.49 V and 1.39 V for typical-typical (tt), slow-slow (ss) and fast-fast (ff) corner, respectively. At 3.3 V, the I_{ref} value is 5.10 μA, 5.23 μA and 4.90 μA for tt, ss and ff corner, respectively.
For CMP1, the pulse width of the output is 8.11ns, 7.40 ns and 8.56ns for tt, ss and ff corner, respectively. Similarly, for CMP2, the pulse width of the output is 8.11 ns, 7.40ns and 8.56ns for tt, ss and ff corner, respectively. For both cases, duty cycle is 10.99%, 10.00%, and 11.60% for tt, ss and ff corner, respectively.

Fig. 10 shows the output of the rectifier for peak input voltage $V_{in}$ of 3.6V different corners. The rectifier output voltage $V_{rec}$ is 3.34V, 3.33V and 3.36V for tt, ss, and ff corner respectively. Dropout voltage is 260mV, 270mV and 240mV for tt, ss, and ff corner, respectively. Fig. 11 shows that even with varying load current (from 7.5 mA to 15 mA), PCE is still greater than 89.5%.

Power conversion efficiency is also measured for different values of load current at 3.6V peak input voltage. From Fig. 11, PCE is at maximum at 10mA load current and equal to 90.06%, 89.99% and 90.16% for tt, ss and ff corner, respectively. Even with varying load current (from 7.5 mA to 15 mA), PCE is still greater than 89.5%.

Power conversion efficiency is also measured for different values of $V_{in}$ for at 10 mA load. From Fig. 12, PCE is at maximum at 3.6V input voltage (90.06%, 89.99% and 90.16% for tt, ss and ff corner, respectively). Even with varying input voltage (from 3.3V to 3.9V), PCE is still greater than 89.2%.

### Table I: Rectifier Specification Summary

<table>
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<tr>
<th>Corner</th>
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<td>$V_{in,peak}$ (V)</td>
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<td>$R_i$ (Ohms)</td>
<td>300</td>
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<td>300</td>
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<tr>
<td>$f_c$ (MHz)</td>
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<td>13.56</td>
<td>13.56</td>
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<tr>
<td>$V_{rec}$ (V)</td>
<td>3.34</td>
<td>3.33</td>
<td>3.36</td>
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<tr>
<td>Dropout voltage (mV)</td>
<td>260</td>
<td>270</td>
<td>240</td>
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<tr>
<td>Settling time (us)</td>
<td>48</td>
<td>44</td>
<td>44</td>
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<tr>
<td>PCE</td>
<td>90</td>
<td>89.99</td>
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### Table II: LDO Specification Summary

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<tr>
<td>Input voltage (V)</td>
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<tr>
<td>$V_{reg}$ (V)</td>
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<td>3.00</td>
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<tr>
<td>Output current (mA)</td>
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<td>Ripple (%)</td>
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<td>0.00557</td>
<td>0.00643</td>
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<td>Overshoot voltage (mV)</td>
<td>49</td>
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<tr>
<td>PCE (at 10mA load)</td>
<td>88.87</td>
<td>89.14</td>
<td>88.64</td>
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<tr>
<td>Line regulation (mV/V)</td>
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<tr>
<td>Dropout regulation (mV/mA)</td>
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<tr>
<td>Load regulation (mV/mA)</td>
<td>0.00653</td>
<td>0.00840</td>
<td>0.00547</td>
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The simulation results for the rectifier is summarized in Table I.

### B. LDO

The output of the rectifier is feed to the LDO in order to provide a stable supply to the IMD. An LDO is designed for 3.35V input voltage and 7.5 mA to 15 mA load range. The input voltage of 3.35 V is chosen since it is the average output voltage (for three corners) from the rectifier circuit. Table II summarizes the simulation results for the LDO.

The strongest point of this paper, in addition providing a relatively higher PCE as compared to previous architectures [12]-[15] is that all comparator components are fully integrated on chip. This is possible by using a constant gm current reference and a common gate amplifier in the comparator with fully integrated turn on and turn off compensation.

![Image](image.png)
Table III summarizes the PCE comparison results. PCE of the rectifier is constant and does not vary for different corners as previously shown in Table I. Most importantly, PCE is still greater than 89.2% even with varying the load from 7.5mA to 15mA and still greater than 89.5% for $V_{in}$ peak range of 3.3V to 3.9V.

IV. CONCLUSION

This paper completes the design of a highly efficient power conditioning unit for an IMD. A high-efficiency rectifier (90% PCE) has been designed for 13.56 MHz, 30 mW, inductively-powered IMD. A stable output voltage of 3.0 V is available at the output of the LDO (89% PCE) to power the IMD electronics. In this work, the comparator components are fully integrated on chip unlike in the case for the comparator in [12].

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REFERENCES