13.56 MHz Highly-Efficient Power Conditioning Unit Using an Active Rectifier and LDO for Implantable Medical Devices (IMD)

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***Abstract*—This paper presents a highly-efficient power conditioning unit using 65 nm CMOS technology for inductively-powered Implantable Medical Device (IMD). The unit is comprised of an active rectifier and a low drop-out regulator (LDO) which together, provides a stable 3 V (30 mW power) to the IMD (load). The active rectifier is equipped with an integrated offset compensation control in the rectifier comparator. Other published works require off chip signals that are necessary for the comparator to work. This paper has all the comparator components integrated on chip. Operating at 13.56 MHz frequency and with peak input voltage of 3.6V, the rectifier has high power conversion efficiency (PCE) of 90%. The LDO has also a high PCE of 89%. Together, the rectifier and the LDO form a high PCE power conditioning unit for a 30 mW IMD.**

***Index Terms*—active rectifier, LDO, IMD, inductive power transmission, 13.56MHz ISM band**

I. Introduction

An implantable medical device (IMD) which is implanted into the human body depends on an outside power source to operate [1], [2]. Approved IMDs have already adopted wireless power transmission where power is provided from an outside power source to an implanted device without any direct electrical contact in between. Among the few forms of wireless power transmission, inductive power transmission is the most commonly used because of its high-power transfer efficiency (PTE) [3]-[6].

Fig. 1 shows the general structure of an IMD which uses inductive power transmission. It is composed of three components: 1) transmitter (Tx); 2) inductive link and 3) receiver (Rx). The power amplifier (PA) in the Tx unit drives the primary coil, L_1 into the carrier frequency f_c. This signal is coupled into the secondary coil, L_2 of the Rx unit via the inductive link. This then generates the alternating current (AC) voltage, V_{coil} across the resonance circuit L_2 and C_2. An alternating current to direct current (AC-DC) converter then follows to supply the load of the receiver with the DC output voltage V_{out}. A low-dropout regulator (LDO) is used after AC-DC converter to provide a constant DC output voltage. The AC-DC converter can either be a passive rectifier, passive voltage doubler, active rectifier or an active voltage doubler. The AC-DC converter together with the LDO forms the power conditioning unit of the power receiver which are required to have high individual Power Conversion Efficiency (PCE) for the total PTE of the system to be high.

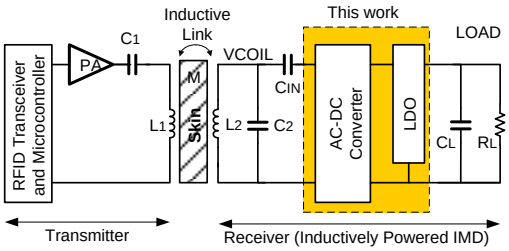

Fig. 1. IMD using inductive power transmission

II. Design and Implementation

Fig. 2 shows the flowchart of the design procedure. Before the actual circuit design, a review of available architectures of rectifier and LDO is done so as provide basis for the schematic design.

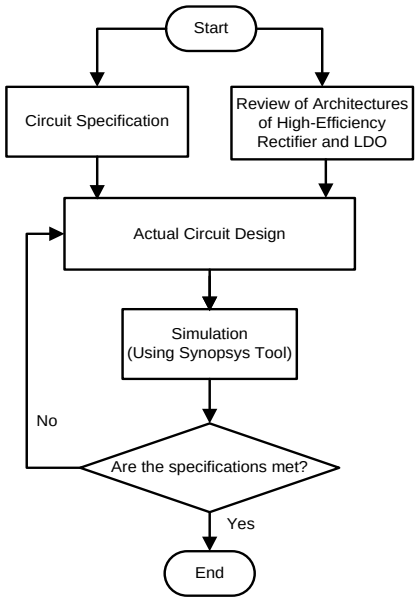

Fig. 2. Flowchart of the design and implementation

Manuscript received February 5, 2018; revised October 25, 2018; accepted November 5, 2018.
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doi: 10.18178/ijeetc.8.2.84-88

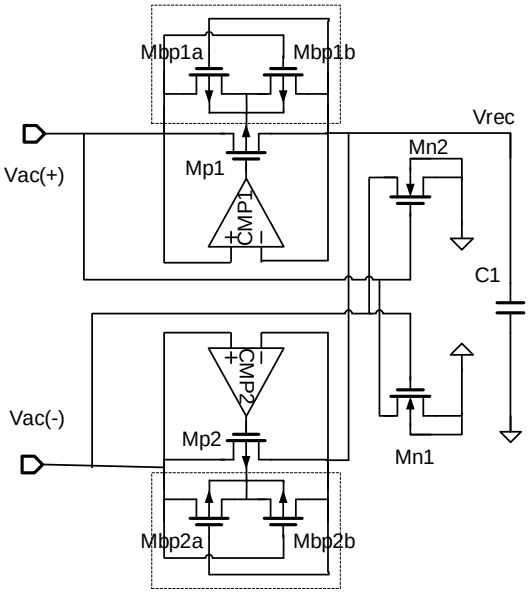

Fig. 3. Active *rectifier*

The idea is to design a high PCE rectifier and high PCE LDO to come up with a power conditioning unit with high PTE. To serve this purpose, an active rectifier is used to function as an AC-DC converter. This active rectifier operates at 13.56 MHz and outputs a rectified voltage which will then be regulated by using an LDO. The output is a constant DC voltage which powers the electronics of an IMD.

A. Active Rectifier

The active rectifier is a full-wave rectifier which composed of two active diodes D_1 and D_2 as well as a cross-coupled nMOS pair N_1 and N_2. All the diodes are implemented as active diodes as shown in Fig. 3. In the active diode implementation, pass transistors driven by a high-speed comparator are used to place the operation at the deep triode region in order to achieve low dropout voltages [7]-[9].

During the positive cycle, when $V_{rec} > V_{ac} > V_{th\,(Mn2)}$ where $V_{ac} = V_{ac(+)} - V_{ac(-)}$ the positive feedback operation of M_{n1} and M_{n2} connects $V_{ac(-)}$ to V_{ss} through M_{n2}. In this case M_{n1} is turned off. The output of CMP_2 is high since $V_{rec} > V_{ss}$ and M_{p2} is turned off. As long as $V_{rec} > V_{ac}$, M_{P1} is off. Now, when $V_{rec} < V_{ac}$, the output of CMP_1 is low thereby causing M_{P1} to turn on. There is now a flow of current from $V_{ac(+)}$ to V_{rec} thus supplying the load. Meanwhile, during the negative cycle of the input V_{ac}, when $|V_{ac}| > V_{th(Mn2)}$, M_{n1} connects $V_{ac(+)}$ to V_{ss} and M_{n2} is turned off. As long as $|V_{ac}| < V_{rec)}$, both M_{P1} and M_{P2} are turned off. When $|V_{ac}| > V_{rec)}$, CMP_2 turns M_{P2} on. In this case current flows from $V_{ac(-)}$ to V_{rec} to supply the load again.

The purpose of auxiliary transistors M_{p1a}, M_{p1b}, M_{p2a} and M_{p2b} is to ensure that the body terminals of M_{P1} and M_{P2} are always connected to the highest potential in the entire circuit. This is to prevent latch up and leakage currents by M_{P1} and M_{P2} because of the sharp transitions experienced by $V_{ac(+)}$ and $V_{ac(-)}$[10], [11].

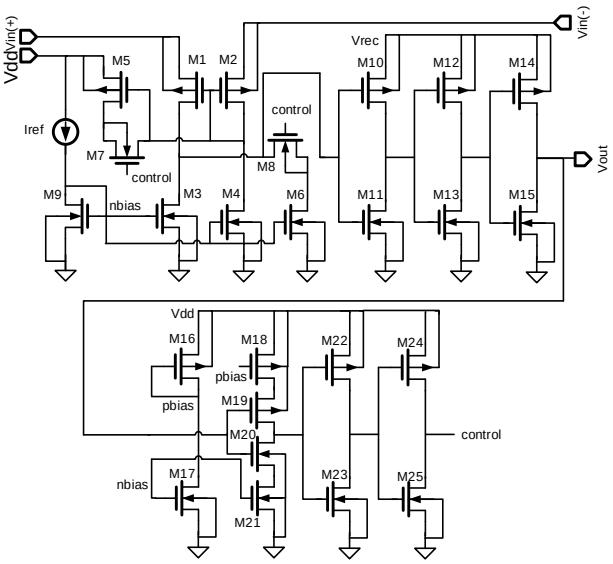

Fig. 4. Comparator

1) Comparator: Comparators play an important role in increasing the PCE of an active AC-DC converter especially when the operating frequency is as high as 13.56 MHz. Note that the rectifying transistors M_{P1} and M_{P2} in Fig. 4 are large devices. As such, when driven by comparators, turn-on and turn-off delay are unavoidable. When these transistors experience turn-on delay, some of the forward conduction time is wasted. On the other hand, when they experience turn-off delay, a reverse current will flow from the load back to the LC tank. In both cases, the PCE of the AC-DC converter is degraded. Hence, there must be some way to compensate for this delay in the comparator so that a high PCE is maintained.

Fig. 4 shows the schematic diagram of the comparator. Transistors M_1 to M_8 form a common-gate amplifier. M_1 and M_2 are set to have non-uniform *W/L* ratio for turn-on delay compensation. The output of the common-gate amplifier is feed to the tapered buffer composed of M_{10} to M_{15} in order to drive M_{P1} and M_{P2} of Fig. 4. Turn-off delay compensation is controlled by transistors M_{16} to M_{25}. Unlike the work in [12], where off chip signals are necessary for the comparator to work, in this paper all comparator components are integrated on chip.

2) Constant Gm Current Reference for the Comparator: To supply the bias current of the comparator, a constant gm-current reference is used. Shown in Fig. 5, the main advantage of using this type of current reference circuit is being insensitive to supply variation. This is necessary in order to ensure proper operation of the comparator at the instant where the regulated output voltage is just starting to raise to its peak.

This circuit provides a nearly ideal current to the comparator. The circuit is divided into three parts: the main current reference circuit, the cascade bias circuit and the start-up circuit. The cascade bias circuit generate the proper bias voltage of the main current reference circuit while the start-up circuit will ensure that the main current reference circuit will operate at the desired point. The current reference is provided by M_{36} for the transistor M_{40} in order to generate the bias voltages for transistors

M_{32}, M_{33}, and M_{39}.On the other hand, current reference is provided by M_{41} for the transistor M_{37} in order to generate the bias voltages for transistors M_{30}, M_{31}, and M_{38}.

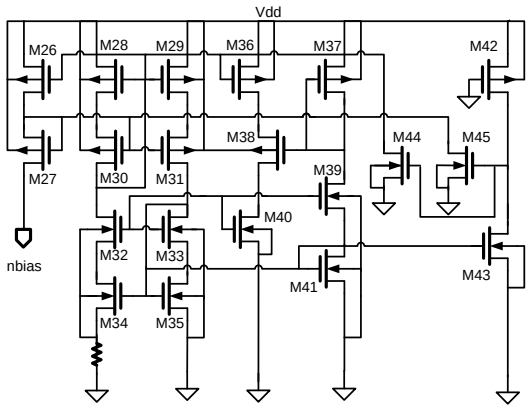

Fig. 5. Constant Gm current reference.

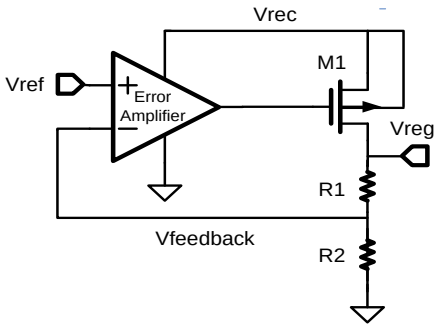

Fig. 6. LDO.

B. LDO

The LDO as shown in Fig. 6 is composed of an error amplifier, feedback network, pass device and voltage reference. The pass device is implemented as a pMOS pass transistor M_1. The feedback network uses a resistor voltage divider which is composed of R_1 and R_2. The voltage reference is temperature independent bandgap voltage reference while error amplifier uses a miller compensated two-stage op-amp.

III. Results and Discussion

A. Rectifier

The actual design of the rectifier starts with the design of the comparator. The primary goal is to turn on and turn off the power transistors at the exact time in order to ensure maximum PCE. To do this the comparator is equipped with turn-on and turn-off compensation circuits in order to compensate for the delay cause by the large gate capacitance of the power transistor. The current reference of the comparator must provide a stable and constant current irrespective of the variation of the supply voltage. Fig. 7 shows the DC analysis of the I_{ref} as supply voltage is swept from 0 to 3.3 V. The I_{ref} value is within 5% of its maximum at supply voltage equal to 1.44 V, 1.49 V and 1.39 V for typical-typical (tt), slow-slow (ss) and fast-fast (ff) corner, respectively. At 3.3 V, the I_{ref} value is 5.10 µA, 5.23 µA and 4.90 µA for tt, ss and ff corner, respectively.

The two power transistors M_{P1} and M_{P2} are simultaneously turned on and off depending on the polarity of the input. For the positive cycle of the input with $|V_{in}| > V_{rec}$, M_{p1} is conducting. On the other hand, for the negative cycle of the input with $|V_{in}| > V_{rec}$, M_{p2} is conducting.

Note that the two (2) power transistors of the rectifier are pMOS. Therefore, the output of comparator CMP_1 must be logic 0 at the positive clock cycle of the input when $|V_{in}| > V_{rec}$. Likewise, the output of comparator CMP_2 must be logic 0 at the negative clock cycle of the input when $|V_{in}| > V_{rec}$. Fig. 8 and Fig. 9 show the output of CMP_1 and CMP_2 respectively.

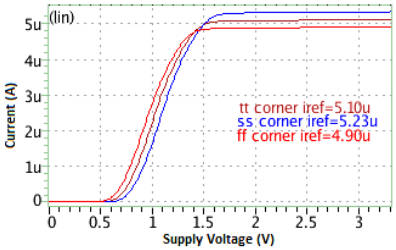

Fig. 7. I_{ref} vs supply voltage.

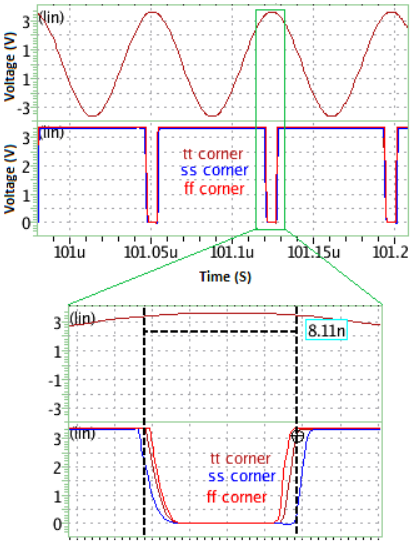

Fig. 8. Output of CMP_1 vs time.

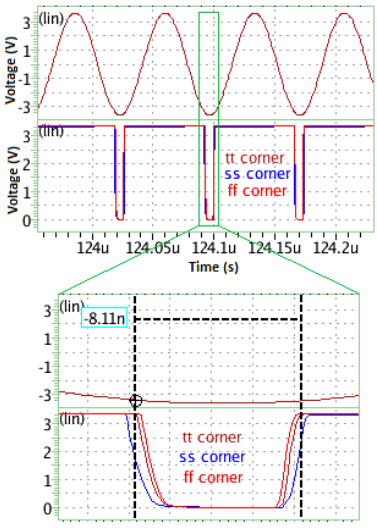

Fig. 9. Output of CMP_2 vs time.

For CMP_1, the pulse width of the output is 8.11ns, 7.40 ns and 8.56ns for tt, ss and ff corner, respectively. Similarly, for CMP_1, the pulse width of the output is 8.11 ns, 7.40ns and 8.56ns for tt, ss and ff corner, respectively. For both cases, duty cycle is 10.99%, 10.00%, and 11.60% for tt, ss and ff corner, respectively.

Fig. 10 shows the output of the rectifier for peak input voltage V_{in} of 3.6V different corners. The rectifier output voltage V_{rec} is 3.34V, 3.33V and 3.36V for tt, ss, and ff corner respectively. Dropout voltage is 260mV, 270mV and 240mV for tt, ss, and ff corner, respectively. V_{rec} settling time is at 48µs, 44µs and 44µs for tt, ss, and ff corner, respectively.

Power conversion efficiency is measured for different values of load current at 3.6V peak input voltage. From Fig. 11, PCE is at maximum at 10mA load current and equal to 90.06%, 89.99% and 90.16% for tt, ss and ff corner, respectively. Fig. 11 shows that even with varying load current (from 7.5 mA to 15 mA), PCE is still greater than 89.5%.

Power conversion efficiency is also measured for different values of V_{in} for at 10 mA load. From Fig. 12, PCE is at maximum at 3.6V input voltage (90.06%, 89.99% and 90.16% for tt, ss and ff corner, respectively). Even with varying input voltage (from 3.3V to 3.9V), PCE is still greater than 89.2%.

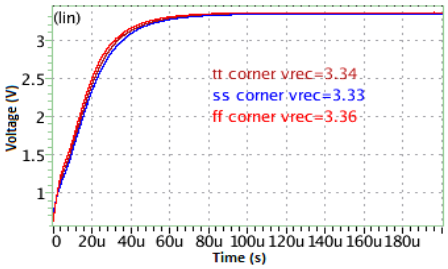

Fig. 10. Output of the rectifier (Vrec) vs time.

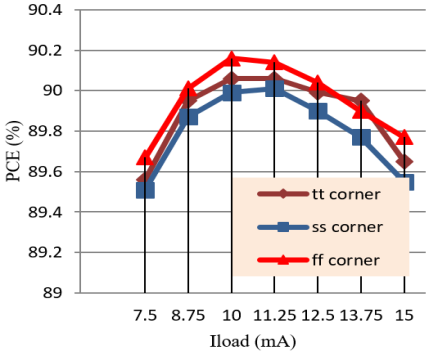

Fig. 11. Rectifier PCE vs load.

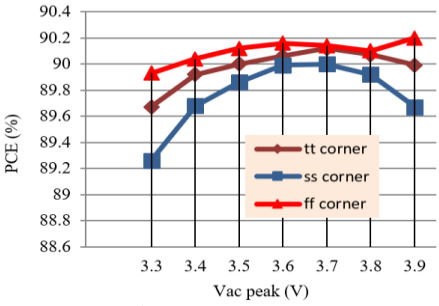

Fig. 12. Rectifier PCE vs input voltage (V_{in}) peak.

TABLE I: RECTIFIER SPECIFICATION SUMMARY

Corner	tt	ss	ff
$V_{in,peak}$ (V)	3.6	3.6	3.6
R_l (Ohms)	300	300	300
f_c (MHz)	13.56	13.56	13.56
V_{rec} (V)	3.34	3.33	3.36
Dropout voltage (mV)	260	270	240
Settling time (us)	48	44	44
PCE	90	89.99	90.16

TABLE II: LDO SPECIFICATION SUMMARY

Corner	tt	ss	ff
Input voltage (V)	3.35	3.35	3.35
V_{reg} (V)	3.00	3.00	3.00
Output current (mA)	7.5-15	7.5-15	7.5-15
Ripple (%)	0.00587	0.00557	0.00643
Overshoot voltage (mV)	49	44	53
PCE (at 10mA load)	88.87	89.14	88.64
Line regulation (mV/V) Input rises from 3.35V to 3.45V	0.00439	0.00438	0.00439
Line regulation (mV/V) Input falls from 3.35V to 3.25V	0.00726	0.00726	0.00729
Load regulation (mV/mA) Load switching current bet. 7.5mA and 15mA	0.00653	0.00840	0.00547

TABLE III: TABLE OF COMPARISON

Publication	2011 [12]	2012 [13]	2013 [14]	2014 [15]	This Work
Technology	0.5 µm CMOS	0.5 µm CMOS	0.5 µm CMOS	0.18 µm CMOS	65nm CMOS
Structure	Active rectifier	Active doubler	Active doubler	Active doubler	Active rectifier
$V_{in,peak}$ (V)	3.8	2.2	1.46	1.192	3.6
V_{out} (V)	3.12	3.1	2.4	2	3.35
R_l (Ohms)	500	500	1000	100	300
I (mA)	6.24	6.2	2.4	20	10
P (mW)	~20	~20	~5.8	40	34
f_c (MHz)	13.56	13.56	13.56	13.56	13.56
Dropout voltage (mV)	700	~1.3	~520	384	260
PCE (%)	80.2	70	79	85	90

The simulation results for the rectifier is summarized in Table I.

B. LDO

The output of the rectifier is feed to the LDO in order to provide a stable supply to the IMD. An LDO is designed for 3.35V input voltage and 7.5 mA to 15 mA load range. The input voltage of 3.35 V is chosen since it is the average output voltage (for three corners) from the rectifier circuit. Table II summarizes the simulation results for the LDO.

The strongest point of this paper, in addition providing a relatively higher PCE as compared to previous architectures [12]-[15] is that all comparator components are fully integrated on chip. This is possible by using a constant gm current reference and a common gate amplifier in the comparator with fully integrated turn on and turn off compensation.

Table III summarizes the PCE comparison results. PCE of the rectifier is constant and does not vary for different corners as previously shown in Table I. Most importantly, PCE is still greater than 89.2% even with varying the load from 7.5mA to 15mA and still greater than 89.5% for V_{in} peak range of 3.3V to 3.9V.

IV. Conclusion

This paper completes the design of a highly efficient power conditioning unit for an IMD. A high-efficiency rectifier (90% PCE) has been designed for 13.56 MHz, 30 mW, inductively-powered IMD. A stable output voltage of 3.0 V is available at the output of the LDO (89% PCE) to power the IMD electronics. In this work, the comparator components are fully integrated on chip unlike in the case for the comparator in [12].

Acknowledgment

This research is funded by DOST-ERDT (Department of Science and Technology-Engineering Research and Development for Technology) and DOST-PCIEERD (Department of Science-Philippine Council for Industry, Energy, and Emerging Technology Research and Development).

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