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Research Paper

DESIGN OF A LOW-VOLTAGE LOW-DROPOUT REGULATOR

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A low-voltage Low-Dropout (LDO) regulator that converts an input of 1 V to an output of 0.85-0.5 V, with 90-nm CMOS technology is proposed. A simple symmetric operational transconductance amplifier is used as the Error Amplifier (EA), with a current splitting technique adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO regulator. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, minimizing the size of the power MOS transistor. Furthermore, a fast responding transient accelerator is designed through the reuse of parts of the EA. These advantages allow the proposed LDO regulator to operate over a wide range of operating conditions while achieving 99.94% current efficiency, a 28-mV output variation for a 0-100 mA load transient, and a power supply rejection of roughly 50 dB over 0-100 kHz. The area of the proposed LDO regulator is only 0.0041 mm^2, because of the compact architecture.

Keywords: Fast transient response, High power supply rejection, Low-Dropout (LDO) regulator, Low-voltage, Small area

INTRODUCTION

POWER management unit with several integrated regulators is widely used in modern battery powered portable devices. These power management schemes often use a primary switching regulator and several postregulators (Lee *et al.*, 2010; and El-Nozahi *et al.*, 2010). The primary switching regulator converts the high dc voltage level of the battery (e.g., 4.2-2.7 V) into a low dc voltage level (e.g., 1 V) with a high conversion efficiency (>90%). The postregulators also generate several independent power sources for multiple voltage domains. The switching regulator inevitably generates voltage ripples over the range of the switching frequency. The switching frequency of the regulator often lies within a low-frequency band of a few 10-100 kHz to reduce switching power loss. The post-regulators should, therefore, be able to provide a good Power Supply Rejection (PSR) ability to suppress these unwanted low-frequency

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noises. To further maintain high power efûciency, minimize the impact on target load circuits, and reduce cost, these post regulators must operate at low voltage and low quiescent current (I_Q), achieve a fast transient response with a small out-put variation, and minimize their area. The low-dropout (LDO) regulator has a simple architecture and a fast-responding loop, which makes it the best candidate to implement these post regulators.

A number of previous papers focused on enhancing the transient response (Hazucha *et al.*, 2005; Al-Shyoukh *et al.*, 2007; Lam and Ki, 2008; Lin *et al.*, 2008; Garimella *et al.*, 2010; Chen *et al.*, 2011; Hu *et al.*, 2011; and Zhan and Ki, 2011) or the PSR (Al-Shyoukh *et al.*, 2007; Lam and Ki, 2008; El-Nozahi *et al.*, 2010; Patel and Rincon-Mora, 2010; and Zhan and Ki, 2010) or both of LDO regulators. The designs in (Hazucha *et al.*, 2005; Al-Shyoukh *et al.*, 2007; Lam and Ki, 2008; and Chen *et al.*, 2011) use either a large driving current or additional circuits, which consume a significant I_Q. The design in (Lin *et al.*, 2008) consumes a small I_Q, yet has a large output variation during the load transient. Further, a complex compensation circuit (Lin *et al.*, 2008) or a high-gain cascode Error Amplifier (EA) (Garimella *et al.*, 2010) complicates the LDO regulator design and is not feasible for low-voltage systems (≤1 V) that are using advanced technology. All the previous regulators are unable to achieve sub 1-V operation.

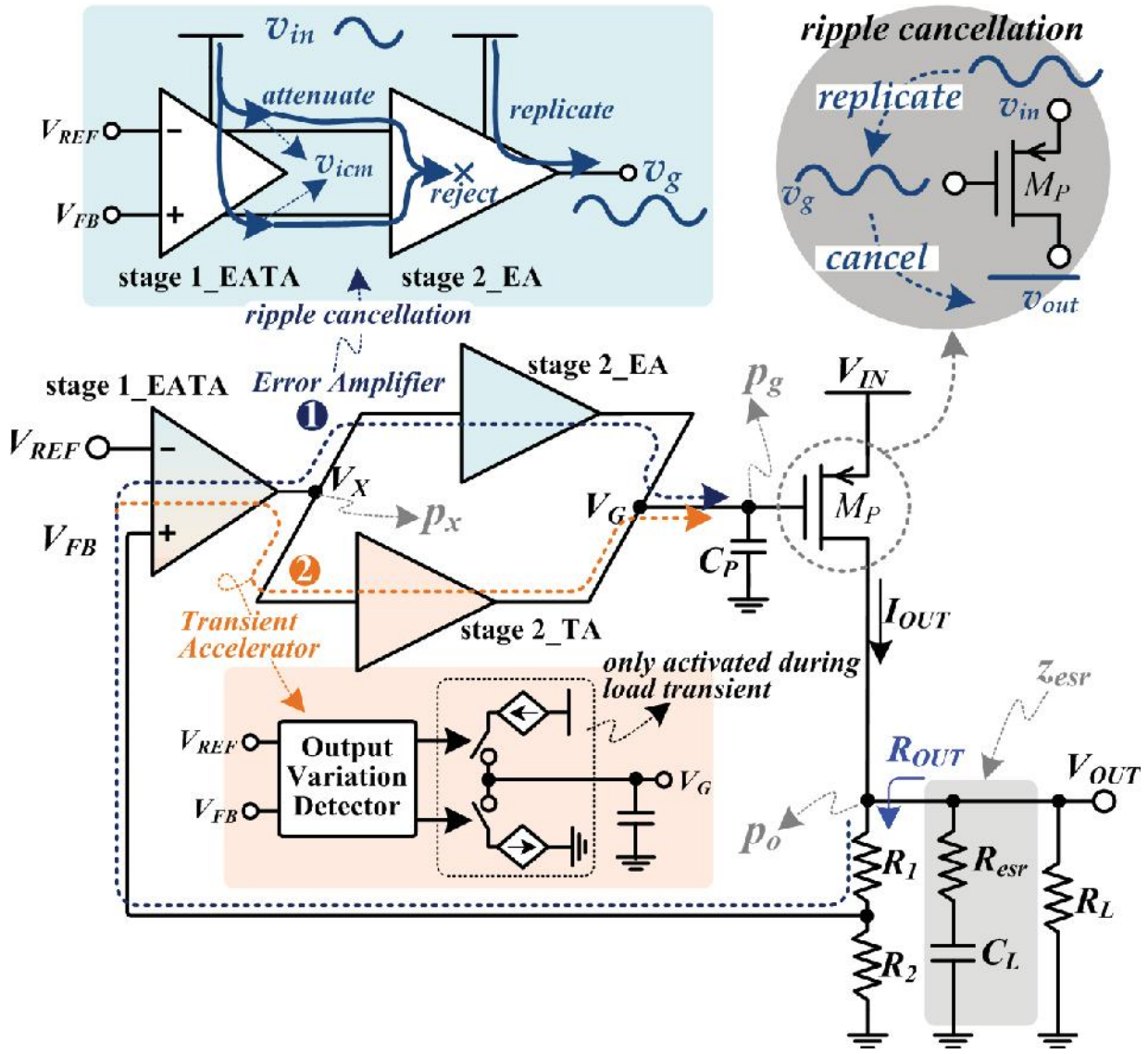
DESIGN CHALLENGES AND CONCEPTS OF THE PROPOSED LOW-VOLTAGE LDO REGULATOR

A basic LDO regulator is mainly composed of a biasing circuit, an EA, a power MOS transistor (M_P), and a feedback network, as shown in Figure 1. Now, the Transient Accelerator (TA) is removed. An off-chip output capacitor (C_L) is used to mitigate the output variations during the load transient. The design challenges and concepts in designing a low-voltage LDO regulator are summarized brieûy in the following sections.

Low Supply (Input) Voltage and Low I_Q

A high loop gain is mandatory in LDO regulator design to achieve optimum performance values such as accurate output (line/load regulation) and PSR. A low supply voltage and output-resistance reduction induced by a shrinking technology limit the achievable gain of the EA. Thus, there are many auxiliary circuits that consume considerable I_Q that are pro-posed to enhance performance. A M_P with a significant size is required for a specific load current when an LDO regulator sinks current from a low voltage power source. Thus, the EA requires a higher current slew rate to drive the M_P. To achieve low-voltage operation, an EA with not more than three stacked transistors between the supply voltage and ground is preferred. each of the transistors, therefore, has more voltage space to stay in the saturation region. A possible candidate can be as simple as an Operational Transconductance Amplifier (OTA) with a low-cost gain-boosting technique like current splitting (Sansen, 2008). The EA also requires a wide output swing to minimize the size of the M_P, and hence relieve the requirement on output current slew rate of the EA.

Figure 1: Conceptual Block Diagram of the Proposed LDO Regulator



Fast Transient Response

The transient response, includes the voltage variation (spike) and recovery (settling) time during the load current transient. The voltage variation is more important than the recovery time, as even a small output-voltage variation (e.g., 50 mV) can cause severe performance degradation to the load circuit oper-ating at an ultralow supply voltage (e.g., 0.5 V). To reduce the output-voltage variation, both a large closed-loop bandwidth of the LDO regulator and a large output current slew rate of the EA are required (Rincon-Mora, 2009). Increasing the closed-loop bandwidth may, however, affect the pole/zero locations and the circuitry may become too complex, consuming more I_Q (Al-Shyoukh *et al.*, 2007; and Chen *et al.*, 2011). The concept of the TA, shown in Figure 1, is, therefore, adopted to conditionally provide extra charging/discharging current

paths (slew current), depending on the status of the output variation detector.

Power Supply Rejection

To provide a clean and accurate output voltage with a low voltage level (≤1 V), noise suppression is paramount. An *n*-type power MOS transistor or a cascoded power MOS transistor structure can achieve a high PSR; however, they are unfeasible for sub 1-V operations. As an LDO regulator adopts a *p*-type power MOS transistor, either a high loop gain or good noise cancellation at node V_G can achieve a high PSR. It is, however, difficult to achieve a high loop gain with a low supply voltage. In addition, the circuit for the power noise cancellation mechanism increases the design complexity and consumes extra I_Q. The concept of resources sharing power noise cancellation mechanism as shown in Figure 1 is thus proposed. The first stage (stage 1_EATA) of the EA attenuates the power noise, whereas the second stage (stage 2_EA) of the EA rejects the common mode noise (v_{icm}) at its inputs, and creates a replica of the supply noise at the output. The stage 1_EATA is shared by the EA and TA, saving the cost and I_Q.

Small Area

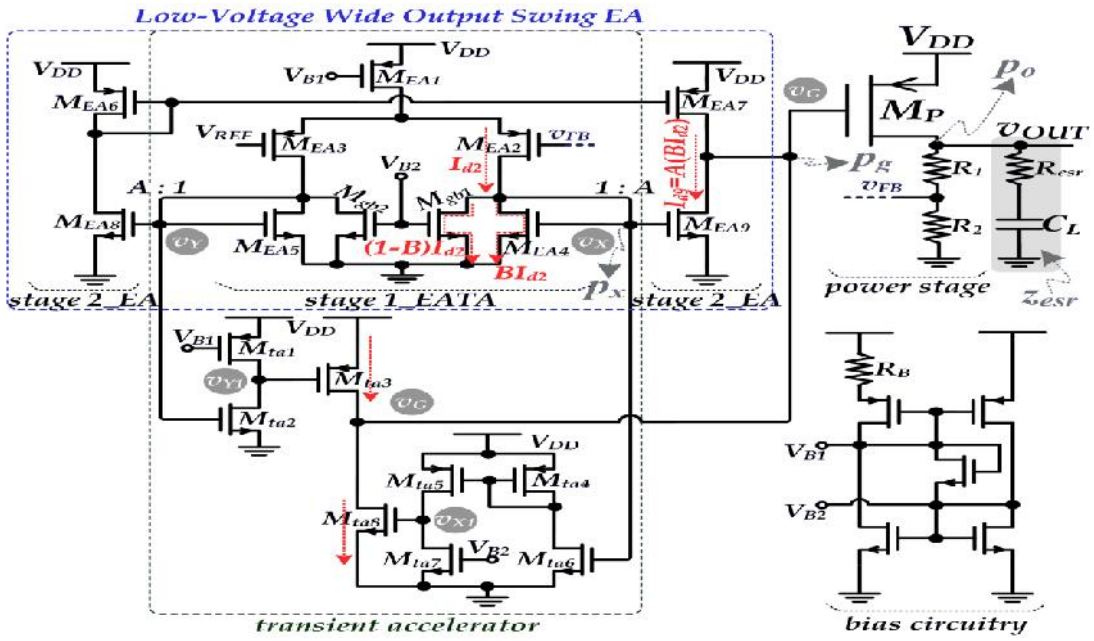
In a low-voltage LDO regulator design, several performance enhancing auxiliary circuits and a large M_P occupy consider-able space. A wide output swing EA can reduce the size of the M_P. To support a wide load current range (e.g., 0-100 mA) and a wide output-voltage range (e.g., 0.5-0.85 V), the M_P may enter the triode region when under a heavy load condition (large V_{SG}) with a low-dropout voltage (small V_{SD}). The M_P should, therefore, be large enough to make the intrinsic gain of the M_P close to one at the triode region and maintain a high loop gain in the LDO regulator. Similarly, the LDO regulator can respond to the load current transient in time for such a wide range of operating conditions.

CIRCUIT REALIZATION AND SIMULATION RESULTS

To achieve the required goals of compact and low-voltage operation while achieving a fast transient response, low I_Q and high PSR, four aspects of the proposed LDO regulator are optimized. The circuit schematic is shown in Figure 2. We first apply the simple symmetric OTA as the EA, composed of M_{EA1}-M_{EA9}, where $gm_{i|i}$ = 1-9, $rO_{i|i}$ = 1-9, and $^{a}{}_{i|i}$ = 1-9 represent the corresponding transconductance, output resistance, and the channel length modulation coefûcients, respectively. The OTA-type EA requires no compensation capacitor, and operates at a minimum supply voltage (V_{DD},min) equal to one threshold voltage plus twice the overdrive voltage (V_{DD},min = V_T + 2 × V_{OV}). Thus, the EA can operate with a low supply voltage (≤1 V). The symmetric structure of the EA also has a low input offset voltage for the regulator to achieve an accurate output. Furthermore, the impedances at node v_x and v_y are low enough to push the nondominant pole (p_x) to a sufficient high frequency so as not to affect the system stability.

The EA achieves a rail-to-rail output swing at node V_G by the output stage (M_{EA7} and M_{EA9}); therefore, the size of the M_P can be minimized for a specific load current requirement. Reducing the size of the M_P significantly reduces the circuit area and contributes to a smaller gate capacitance. This allows the EA

Figure 2: Circuit Schematic of the Proposed LDO Regulator



to drive the M_P by a large enough slew rate with a relatively low biasing current. The gain of the EA (A_{EAO}) is as follows:

$$A_{EAO} = gm \times A \times (rO7 || rO9)$$

$$\approx gm2 \times A \times rO9$$

$$= \frac{2I_{d2}}{V_{oV2}} xAx \frac{1}{^{a}9xAxI_{d2}}$$

$$= \frac{2}{Vo2x^{a}9} \quad ...(1)$$

where we assume ($rO7$ _ $rO9$) and let {I_{d2}, V_{OV2}, A} represent the bias current, overdrive voltage of M_{EA2}, and current ratio between the first and second stages of the EA, respectively. The A_{EAO} in (1) is too low to achieve a fast transient response and high PSR. Therefore, we apply the current splitting technique to boost the gain by maintaining $gm2$ and increasing $rO9$. The transistors M_{gb1} and M_{gb2} can reduce the bias current being mirrored to the second stage of the EA. Thus, the gain of the modified EA (A_{EAM}) is boosted by a factor of 1/B as follows:

$$A_{EAM} \approx gm2 \times A \times rO9$$

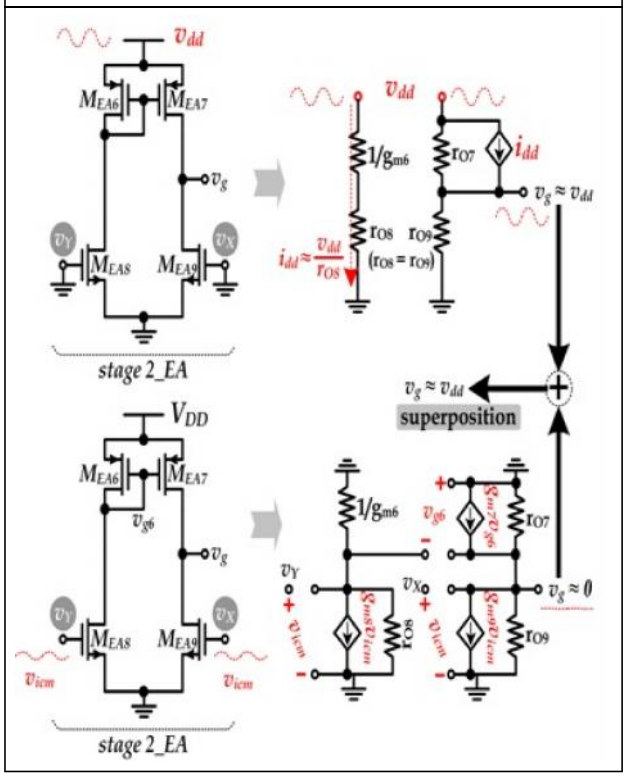
$$= \frac{2I_{d2}}{Vo2} xAx \frac{1}{^{a}9xAxBxI_{d2}}$$

$$= \frac{A_{EAO}}{B} \quad ...(2)$$

where B is the current splitting ratio and is <1.

A p-type device is chosen to construct the power MOS transistor MP, because of the low supply voltage and low-dropout voltage requirements. The gain-boosted OTA-based EA improves the loop gain of the LDO regulator, which in turn enhances the PSR performance. In addition, we create a replica of the power noise at the gate terminal of the M_P to cancel out the power noise at the source terminal of M_P. This further improves the PSR performance. To reduce the area and I_Q, we use the existing EA to replicate the power

Figure 3: Low-Frequency, Small-Signal Model of the EA Output Stage (Stage 2_EA) for Ripple Cancellation Analysis



noise instead of using an auxiliary circuit. The two equivalent resistors between the output nodes (v_x and v_y) of the ûrst stage of the EA (stage 1_EATA) and the ground have a low resistance value ($1/gm4$ and $1/gm5$); therefore, the power supply noise of stage 1_EATA can be attenuated at nodes v_x and v_y. Only a small level of power supply noise can be coupled to nodes v_x and v_y, as they appear in the form of a common mode input (v_{icm} in Figure 3) to the output stage of the EA (stage 2_EA). We first assume that the power noise is propagated by stage 1_EATA through the common mode signal v_{icm} and causes a fiuctuation on v_{g6}. The output v_g induced by v_{icm} is, therefore, given by

$$v_g = (gm7v_{g6} - gm9v_{icm}) \cdot (rO7||rO9) \approx 0 \quad ...(3)$$

where we assume that M_{EA8} and M_{EA9} are matched devices ($gm8 = gm9$), ($rO8\_1/gm6$), and ($gm6 \approx gm7$). To cause gm6 to be close to $gm7$, the channel length of M_{EA6} and M_{EA7} are selected to be five times the minimum length to reduce the effect of channel-length modulation. Then, we ground both the nodes v_x and v_y and input the power noise from the power supply (V_{DD}). The small-signal model shown at the top of Figure 3 is used to show how the power noise is replicated to v_g.

Application of the superposition theorem by summing (3) and (4), we see that almost the entire power supply noise is replicated to the gate terminal of M_P(v_g). As the frequency of the power noise increases, the small-signal model shown in Figure 3 is no longer valid as the equivalent impedance of the parasitic capacitance of M_P(C_{gs}/C_{gd}) becomes finite and can no longer be ignored. As C_{gs}/C_{gd} equals 1.4/0.5 pF in our design, the PSR is expected to fall when the frequency of the power noise goes >100 kHz.The first stage of the EA and M_{ta1}-M_{ta8} constitutes the TA that reduces the slew time of the gate terminal of M_P by increasing the dynamic discharging/ chargingcurrent during the load transient. The ûrst stage of the EA is reused as a part of the output variation detector of the TA to reduce the circuit complexity. Furthermore, to avoid a signiûcant increase in I_Q and to avoid the breaking of perfect replication of the power noise at the gate terminal of M_P, M_{ta3}, and M_{ta8} are biased at the cutoff region in the steady state. A large load change causes a variation in both the output voltage (v_{OUT}) and feedback voltage (v_{FB}).

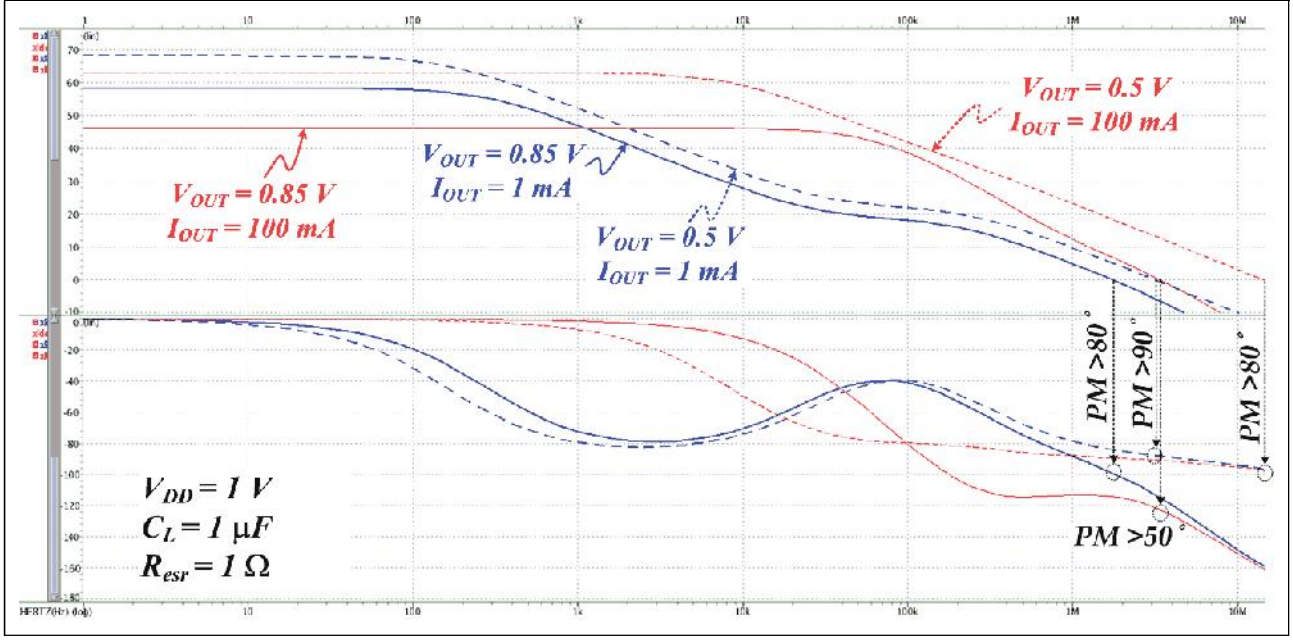
The proposed LDO regulator shown in Figure 2 has three poles (p_o, p_x, and p_g) and

one zero (z_{esr}), and the simulated frequency response of the loop gain for different load currents (I_{OUT} = 1 and 100 mA), output voltage (V_{OUT} = 0.5 and 0.85 V) are shown in Figure 4. The dominant pole is p_o(100-10 kHz) due to the large off-chip compensation capacitor C_L(1«*F*). The second dominant pole (p_g) is located at a relatively high frequency (~100 kHz) as the wide output swing of the EA reduces the size of the M_P. Thus, p_g can be easily cancelled by the zero (z_{esr}). The third pole (p_x) is far beyond the UGF because of the simple architecture of the OTA-based EA, and therefore does not affect the stability. Figure 4 guarantees the stability of the proposed LDO regulator for a wide range of operating conditions.

EXPERIMENTAL RESULTS AND THE PERFORMANCE EVALUATIONS

The proposed LDO regulator is fabricated using a 90-nm CMOS process. The core area is only 0.0041 mm^2 and the maximum load current is 100 mA. The input voltage is 1 V and the values of R_1 and R_2 can be adjusted to generate any regulated output level between 0.85 and 0.5 V. The maximum I_Q is 60 «*A*, achieving a 99.94% current efficiency. The C_L used for measurement is 1 «*F* with a R_{esr}. The input/output voltage V_{DD} and V_{OUT} is set to {1 V, 0.85 V} and {1 V, 0.5 V}, respectively. The output variations during load transient (_V_{OUT}) are measured to be only 28 and 24 mV for V_{OUT} equal to 0.85 and 0.5 V, respectively. The rise/fall time (10 «*s*) of the load current transient is restricted by the limitation of our measurement instrument (Chroma Electronic Load System 6300 Series). The ac capability of the proposed LDO regulator is, therefore, not tested to its best condition and the resulting small output variations are from enough dc loop gain. As the output variation of 28 mV is far less than the value of (100 mA × R_{esr}), we can, however,

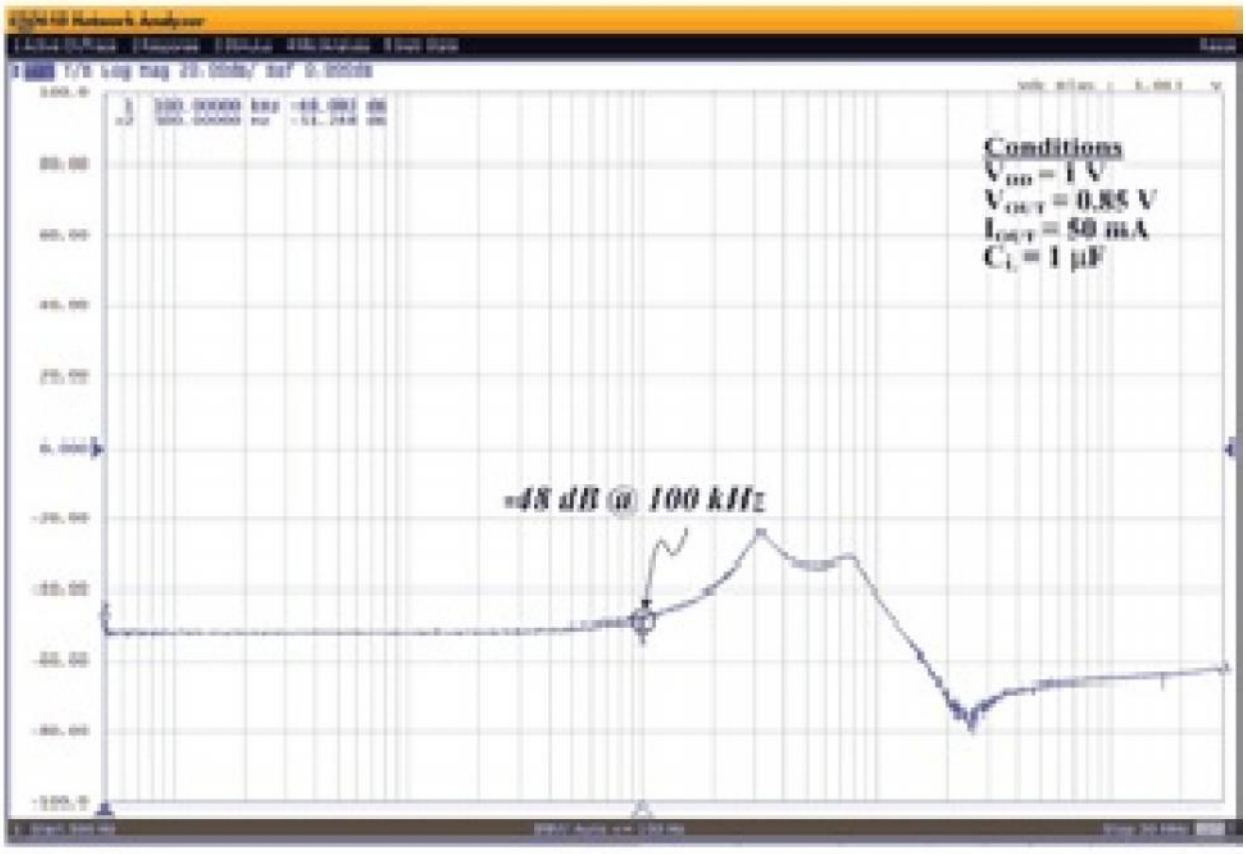
Figure 4: Simulated Frequency Response of the Proposed LDO Regulator for Load Currents of (1 mA, 100 mA) and Output Voltages (0.5 V, 0.85 V)



speculate that the response time of the LDO regulator test chip is far <10 «*s*. The PSR performance is also measured when the test conditions are V_{DD} = 1 V, V_{OUT} = 0.85 V, and I_{OUT} = 50 mA; the measured result is shown in Figure 5. The proposed LDO regulator achieves a PSR ~ 50 dB at low frequencies whereas the rolloff frequency is ~100 kHz. Although the consumed I_Q is larger than the design in [6], the proposed LDO regulator benefits from superior performance in output variations. In contrast, Lam and Ki (2008) produced the smallest output variation (0-50 mA), yet consumed a significant I_Q. To fairly evaluate the performance of the load transient response, the frequently used figure of merit (FOM1) proposed in Hazucha *et al.* (2005) was adopted to include the dependence of the output capacitance. The design in Garimella *et al.* (2010) had a better FOM1 than the proposed design; however, it did not show the dominant ESR effects of output variation during the load transient. Further, Garimella *et al.* (2010) was unable to operate below 1-V input voltage, and does not report the PSR performance. We also use FOM2 that is (FOM1 × area) to show the area efûciency further.

In summary, the proposed LDO regulator is compact in size, and achieves a high PSR, fast transient response, and high current efficiency for low-voltage operation.

Figure 5: Measured PSR Performance (V_{DD} / V_{OUT} / I_{OUT} = 1 V / 0.85 V / 50 mA)



CONCLUSION

This paper presented an LDO regulator using a simple OTA-type EA plus an adaptive transient accelerator, which can achieve operation below 1 V, fast transient response, low I_Q, and high PSR under a wide range of operating conditions. The proposed LDO regulator was designed and fabricated using a 90-nm CMOS process to convert an input of 1 V to an output of 0.85-0.5 V, while achieving a PSR of ~50 dB with a 0-100-kHz frequency range. In addition, a 28-mV maximum output variation for a 0-100-mA load transient, and a 99.94% current efûciency was achieved. The experimental results veriûed the feasibility of the proposed LDO regulator.

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