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Research Paper

SPWM GENERATOR BASED ON FPGA FOR HIGH SWITCHING FREQUENCY DC/AC INVERTERS

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The digital implementation of Sinusoidal Pulse Width Modulation (SPWM) generators have dominated over their counterparts based on analog circuits. Here an FPGA based SPWM generator is implemented, which is capable to support the high switching frequencies more than 1 MHZ, thus it is capable to support the high switching frequency requirements of modern single-phase dc/ac power converters. This design occupies a small fraction of a medium sized FPGA and, thus can be integrate in larger designs. In addition to that, it has a flexible architecture that can be implemented to a variety of single-phase dc/ac inverter applications. This experimental results confirm that compared to the past-proposed microcontrollers and DSPs generation unit designs, the SPWM generator exhibits much faster frequency, lower power consumption, and higher accuracy of generating the desired SPWM waveform.

Keywords: SPWM, DC, AC, FPGA, DSP

INTRODUCTION

The dc/ac converters (inverters) are the major power electronic conversion units in renewable energy production, motor drive, and uninterruptible power supply applications. The Sinusoidal Pulse Width Modulation (SPWM) technique is widely employed in order to adjust the dc/ac inverter output voltage amplitude and frequency to the desired value. In this inquest, the power converter switch MOSFET is set to the ON or OFF state according to the result of the comparison between a high-frequency, constant-amplitude triangular wave (carrier) with two low-frequency (e.g., 50 Hz) reference sine waves of adjustable amplitude and/or frequency. A dc/ac inverter comprised of four cascaded Z-source inverter modules, which have been built using Gallium Nitride devices operating at high switching Frequency. Compared to the microcontroller and DSP-integrated circuits, FPGAs have the advantage of flexibility in case of changes and they enable the reduction of the execution time of the dc/ac inverter control algorithm due to their capability to integrate digital

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hardware with high speed and parallel processing features. The triangular wave is implemented in the form of an up-down counter. The SPWM control signals are produced by comparing the corresponding values of the sinusoidal and carrier digital signals. The SPWM pulse train is produced by comparing the sinusoidal and triangular signals generated according to the Direct Digital Synthesis (DDS) technique. The comparison is performed using a high-speed analog comparator. The regular-sampled PWM technique presented in targets to reduce the amount of computation time required in order to facilitate the generation of higher switching frequencies online and in real time.

In this technique, the pulse width is calculated once and used over N consecutive switching edges of the SPWM wave pulses. Then, a new sample of the reference sine wave is acquired. Consequently, the number of calculations required to produce the complete SPWM waveform is N times less than in the conventional SPWM generation methods. In this architecture the values of both the reference sine and triangular waves are stored in the FPGA device Block RAMs (BRAMs) in order to exploit their one-clock cycle access time, thus providing a much higher switching frequency capability.

RELATED WORK

There are different types of methodologies found in architecture to obtain high switching frequency. However it is important to reach the high switching frequency. SPWM generator is used to adjust the dc/ac inverter output voltage and frequency. It can be adapted in various single phase inverter mainly to increase switching frequency mostly recently developed reduced common voltage PWM methods under one umbrella, is established. They program the pulse patterns of various high performance applications. However, this will not modulate the several pulses per half cycle. So if we make use of Sinusoidal Pulse Width Modulation (SPWM) the width of each pulse is varied proportional to the amplitude of a sine wave evaluated at the center of the same pulse. DPWM architecture Reduce the exceedance of clock frequency requirements but the disadvantage in this paper is that the Clock frequency may exceeds the operating frequency (Hava and Cetin, 2011).

The possibility of Adjustable switching frequency can be done by Full bridge HF LCL resonant inverters switching is achieved for all switches for the whole power range. With the phase shift modulated as sinusoidal, a full-wave rectified output current synchronized with the utility line is obtained. So here we make use of the dc/ac inverter as major power conversion production units which can be implemented in renewable energy sources, motor drives and uninterruptable power supply applications but it has only fixed switching frequency (Patel and Madawala, 2009).

Multi bit binary signals (for generation of sinusoidal pulses) has the possibility of reduced Inverter output filter size (due to reduction in harmonics distortion) and so cost is low in case of improved size filter it failed to retain its capacity (Li and Bhat, 2012).

The bit stream representation has the advantage of having the characteristics of a classical pulse width modulation signal and hence can be used to drive high power switching devices with minimal conditioning. The practical implementation lead to total harmonic distortion measures ranging between 0.75% and 4.92%.But this leads to high cost and the filter size is large in size. Increasing switching frequency of the triangular wave results in a reduction of the dc/ac inverter output filter size and cost (Navarro *et al.*, 2012).

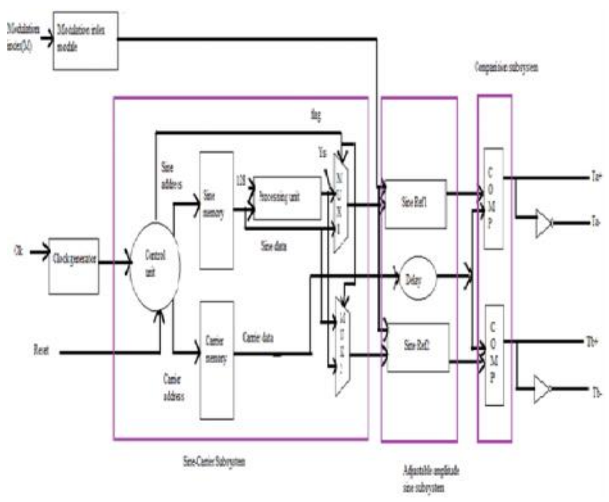
Advantages of digital control in power electronics have led to an increasing use of Digital Pulse Width Modulators (DPWM). But if we make use of DPWM architecture then the clock frequency requirements may exceed the operational limits when the power converter switching frequency is increased. In order to reduce the exceedance of clock frequency requirements here we implementing the FPGA based SPWM generator unit (Lei and Tina-Yu, 2011).

A phase modulated high frequency isolated DC/AC converter is used for a PMSG-based grid-connected wind generation application. With the single phase shift modulated as sinusoidal, a 120 Hz rectified output current is obtained. A Control strategy for a single phase series connected inverter with a micro grid is used to connect the ac load not only to regulate the load voltage under load disturbances but also to control the load power drawn from the micro grid. Use of control strategy also facilitates a specific power of active power flow to the irrespective of the micro grid voltage condition. The rest of the load power is supplied to the micro grid (Hayashi *et al.*, 2007).

DESIGN METHODOLOGY

Architecture of SPWM Generator

Figure 1: Block Diagram of SPWM Generator



Clock Generator Subsystem

The "Clock generator" subsystem takes as input the FPGA input clock and produces a new clock signal used by the digital circuits of the SPWM generator, such that the desired SPWM switching frequency *fc* specified by the designer/user is generated. A two-state Finite State Machine (FSM) is initially used to set the input clock frequency f_{clk} to $f_{clk/2}$ and then a Digital Clock Manager module adapts this frequency to the desired value.

Modulation Index Subsystem

The "Modulation index" subsystem is used to convert the floating-point modulation index *M*, which is input in the SPWM generation system to the corresponding value in fixed-point arithmetic. The floating point value produced is then converted into a fixed-point value ranging from 0 to 255, via a float-to-fixed point conversion unit, thus producing the "Index" output of the "Modulation index" subsystem.

Sine-Carrier Subsystem

The "Sine-Carrier" subsystem consists of the control unit, two BRAMs, which contain samples of the sinusoidal and triangular (i.e., carrier) waves and two multiplexers that produce the two constant-amplitude reference sine waves used for the production of the SPWM output signals. The BRAMs of the sine wave and carrier operate as LUTs. Both the sinusoidal and triangular waves are sampled and quantized with the same sampling frequency *fs* using MATLAB. In order to minimize the utilization of the FPGA resources, only the values are stored in the corresponding BRAM, while the values of the sine wave during the time interval ®/2 – 2® are calculated by mirroring and inverting the values of the first quarter. The BRAM of the carrier contains the values of a complete period of the reference triangular wave. Consecutive addresses of both memories are generated in every clock cycle by the control unit. The control unit also produces a "flag" signal, which is responsible for the retrieval of the sine-wave values during the time interval ® – 2® of the reference sine-wave period. The BRAM of the constant-amplitude sinusoidal wave is scanned up and down four times, since this memory contains only the values during the first quarter of the sinusoidal-wave period. The value of the "flag" signal determines the up or down direction of consecutive accesses performed for retrieving the data stored in the BRAM memory of the reference sine wave. While "flag" is set to 0, the multiplexer "MUX1" outputs the data read from the constant-amplitude sinusoidal memory. Otherwise, "MUX1" outputs the values corresponding to the second half-cycle (i.e., during ® – 2®) of the constant-amplitude sinusoidal wave. The multiplexer "MUX2" is used for the production of the second constant-amplitude reference sine wave, which operates with a 180° phase difference compared with the one analyzed above.

Adjustable Amplitude Sine Subsystem

The "Adjustable amplitude sine" subsystem takes as input the constant-amplitude reference sinusoidal values produced by the "Sine-Carrier" subsystem and generates sinusoidal digital signal Yawith amplitude adjustable according to the value of the modulation index M which is an input in the SPWM generation system. The value of Y_a is in the range 0-255 Index is the output of the "Modulation Index" subsystem.

Comparison Subsystem

The "Comparison" subsystem implements the comparison between the high frequency constant-amplitude triangular wave (carrier) with the two low-frequency reference sine waves, using two comparators. The control signals, *Ta*– *Tb*+, and *Tb*– of the single-phase dc/ac inverter power switches are generated from the outputs of the corresponding comparators of this subsystem, thus forming the SPWM wave at the dc/ac inverter output terminals. *Ta*+ and *Tb*+ are the outputs of the comparators in the "Comparison subsystem".

IMPLEMENTATION OF SPWM GENERATOR UNIT

MATLAB System

The MATLAB system consists of these main parts:

Desktop Tools and Development Environment: This part of MATLAB is the set of tools and facilities that help you use and become more productive with MATLAB files and functions. Many of these usages are graphical user interfaces. It includes: browsers for viewing help, the workspace, and folders. Mathematical Function Library: This library is a vast collection of computational algorithms ranging from elementary functions, like addition, sine, cosine, and complex arithmetic, to more advanced functions like matrix inverse, matrix Eigen values, and fast Fourier transforms.

The Language: The MATLAB language is a high-level matrix/array language with control flow, data structures, functions, input/output, and many other programming features. It allows both “programming in the small” to rapidly create quick programs you do not intend to reuse. You can also do “programming in the large” to create complex application programs intended for reuse.

Graphics: MATLAB has extensive facilities for displaying vectors and matrices as graphs. It contains high-level functions for bi-dimensional and three-dimensional data visualization, image processing and graphics. It also includes low-level functions that allows to fully customize the appearance of graphics and to build complete graphical user interfaces on MATLAB applications.

External Interfaces: The interfaces library allows you to write C/C++ and FORTRAN programs that interacts with MATLAB which includes facilities for calling routines (dynamic linking), for calling MATLAB as a computational engine, and for retrieving and writing MAT-files.

Modelsim

The Modelsim advanced code coverage capabilities provide valuable metrics for systematic verification. Information is stored in the Unified Coverage Database, which is used to manage and collect all coverage information in a highly efficient database. Coverage materials that analyze code coverage data, such as test ranking and merging, are available. Coverage results can be viewed by post-simulation else after a merge of multiple simulation runs. Code coverage metrics can be depicted by instance or by design unit, giving flexibility in managing coverage data.

RESULTS AND DISCUSSION

Figure 2: SPWM Generation Unit

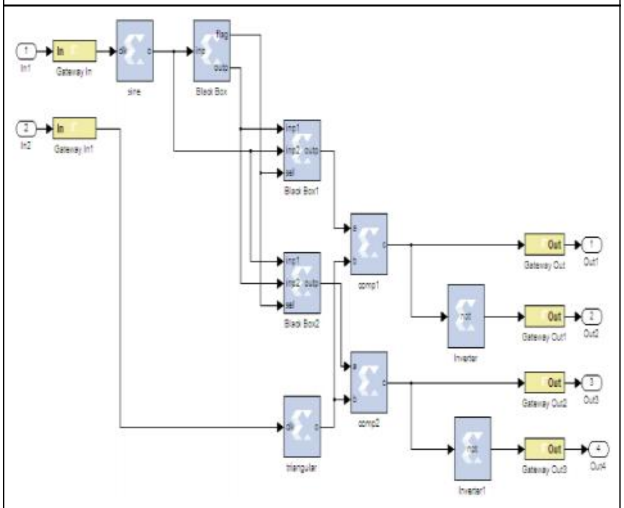


Figure 3: Output of SPWM Generator Unit

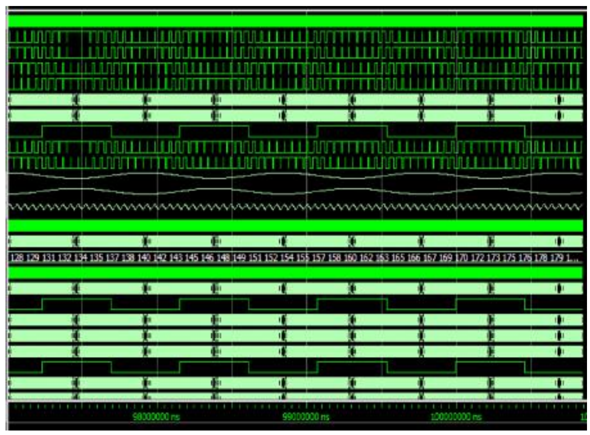
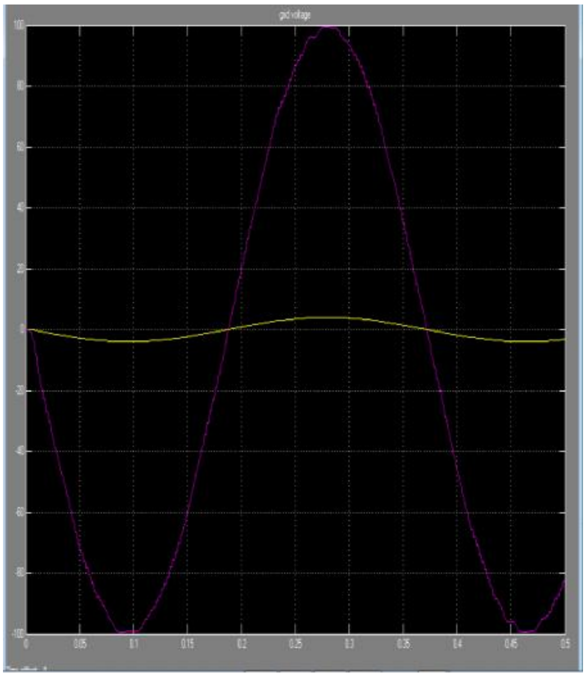


Figure 4: Output of dc/ac Inverter



CONCLUSION

The SPWM principle is widely used in dc/ac inverters in energy conversion and motor drive applications. The past proposed SPWM generators have been designed to operate at low switching frequencies, while this have a higher switching frequencies.

Here an FPGA-based SPWM generator has been presented, which is capable to operate at switching frequencies more than 1 MHz, thus it is able to support the high switching frequency requirements of modern single-phase dc/ac inverters.

SPWM generator exhibits much rapid switching frequency, lower power consumption, and higher accuracy of generating the desire SPWM waveform.

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