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Research Paper

AREA POWER AND DELAY EFFICIENT EVALUATION OF TRUNCATED AND MODIFIED WALLACE FIR FILTER

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The most area and power consuming arithmetic operation in high-performance circuits like Finite Impulse Response (FIR), multiplication is one. There are different types of multipliers to reducing the cost and effective parameters in FIR filter design. Among those this paper use truncated multiplier and modified Wallace multiplier in the fir design. The structural adders and delay elements occupies more area and consumes power in this form so it was a reason to forward the proposed method. In prior FIR filters design with low cost effective results will done by the faithfully rounded truncated multipliers with the carry save additions. In MCMAT design the low cost FIR filters within the best area and power results are implement in this paper by using the improved truncated methods. Along with that the proposed method modified Wallace multiplier based fir filter is also designed in this paper to make the fir filter design is suitable for low power applications.

Keywords: Finite Impulse Response (FIR) Filter, Multiple constant multipliers/Accumulators with faithfully rounded truncation (MCMAT), Truncated multiplier, MODIFIED WALLACE tree multiplier

INTRODUCTION

In the field of electronic industry digital filters are used extensively. The noise ranges gradually increases by using analog filters for better noise performance can be obtained by using digital filters compared to analog filters. At every intermediate step in digital filter transformation able to perform noiseless mathematical operations. Our design includes the optimization of bit width and hardware resources without any impact on the frequency response and output signal precision [1]. Addition (or subtraction), Multiplication (normally of a signal by a constant) Time Delay, i.e., delaying a digital signal by one or more sample periods are three basic mathematical

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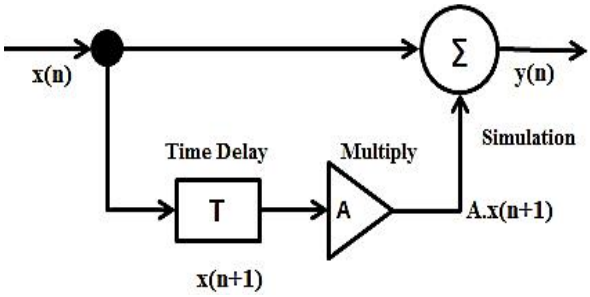
operations used in digital filter is shows in Figure 1. By using the mathematical operations mentioned above we can describe the behavior of the filter. The coefficients are multiplied by fixed-point constants using additions, subtractions and shifts in a multiplier block [5].

Figure 1: Block Diagram of a Simple Digital Filter



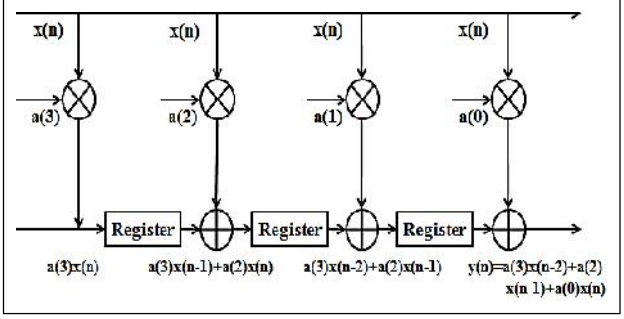
The unit sample of the signal defined by $\delta(n)$ is response one for generating the digital filter impulse response h(n). Input sequence x(n) can whose response can be calculated easily if the impulse response is known at every sample index at n = 0 a unit impulse is applied so that to attain non zero response for whose value of n is greater than or equal to 0 (i.e., $n \geq 0$). The impulse response made to be idle so that to avoid uneven responses before applying input. It follows a time invariant property, in which the response delayed by a sample of $\delta(n - k)$.

The input x(n) whose response is shown as below

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k)$$

In VLSI Signal Processing two types of digital filters are most widely used one is FIR (finite impulse response) and the other is IIR (infinite impulse response). FIR as indicates that the impulses are finite in this filter and phase is kept linear in order to noise distortions and no feedback is used for such a filters. As compared to IIR, FIR is very simple to design. Such type of FIR filters are used in DSP processors for high speed. In Digital Signal Processing Multiplication and addition is of times required. A high speed addition is done by parallel prefix adder and the better version of truncated multiplier with fewer components makes the reduction in delay [4]. For multi-rate applications FIR filters are suitable for decrease in sampling rate called decimation or for increase in sampling rate called interpolation, or for both. Either decimating or interpolating, the calculations are omitted by using FIR, which indeed used for maintaining. For limited calculations IIR is used because all output is found separately, even though there is a need of providing feedback. In Digital Signal Processing, FIR filters define less number of bits which are designed by using finite-precision. In IIR filter by using feedback problems will raise but in FIR filters limited bits are efficient in which there is no feedback. Using fractional arithmetic we can implement FIR filters. But in IIR filters, coefficients with magnitude of less than 1.0 are always possible to implement a FIR filter. Using FIR

Figure 2: FIR Filter Architecture



filters is that they require more co-efficient than an IIR filter in order to implement the same frequency response, therefore needing more memory and more hardware resources to carry out mathematical operations.

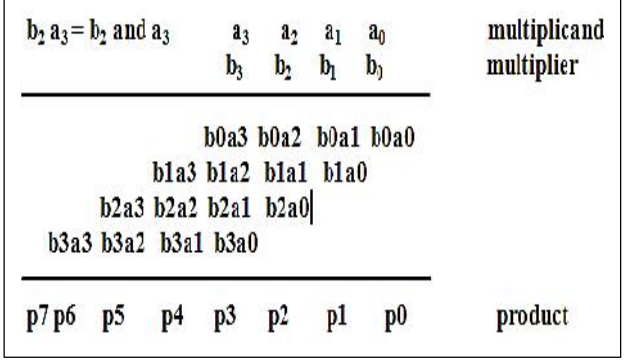
MULTIPLIERS

Now a day's fast co-processors, digital signal processing chips and graphics processors has created to satisfy customer needs for high speed and area efficient multipliers. Current design range from small, low-performance shift and add multipliers, to large high-performance array and tree multipliers. High performance is achieved in Conventional linear array multipliers, and require huge amount of silicon. Higher performance has gained for Tree structures than linear arrays but the tree interconnection is more complex and less regular. In paper various multiplier architectures have designed, during the past few years. In digital signal processors and microprocessors multiplier is one of the key hardware blocks in most of the digital and high performance systems. With the recent advances in technology, more efficient multipliers have routed by many researchers. The main motivation behind this paper is to offer lower power consumption without increase in silicon area.

Binary Multiplications

Figure 3 represents the process of multiplying two binary numbers, the multiplicand and the multiplier rules; if the inputs are n bit then the output should be 2n. The green box indicates the partial product matrix and the red box indicates a single partial product. The first step in this method is to form the partial product matrix are obtained by Adding the multiplicand and multiplier bits. Another way to look at this is if the multiplier bit is 0, the partial product is also 0. If the multiplier bit is 1, the partial product is equal to the multiplicand repeat for every multiplier bit Notice that this gives a number of partial products equal to the width of the multiplier. To obtain the final product the elements in the columns (from right to left) are added using binary logic 7. Any carries are carried on to the next column. The result of this operation is stored in one bit of the product and the operation is repeated for each remaining column.

Figure 3: 4 x 4 Bit Binary Multiplication



Wallace Tree Multiplier

To reduces the number of partial products to be added into 2 final intermediate results we use Wallace tree. The basic operation of Wallace tree is multiplication of two unsigned integer, an efficient hardware to implement a digital circuit that multiplies two integers is Wallace tree multiplier, designed by an Australian Computer Scientist Chris in 1964.

There are three steps in Wallace Tree:

1. Partial Product Generation Stage
2. Partial Product Reduction Stage
3. Partial Product Addition Stage

Partial Product Generation Stage

The first step in binary multiplier is Partial product generation. These are the intermediate terms which are generated based on the multiplier value. If the multiplier bit is '0' (zero), then partial product row is also '0' (zero), and if it is '1' (one), then we can copy the multiplicand as it is. Each partial product row is shifted one unit to the left from the 2nd bit multiplication onwards is shown in the above mentioned example. The sign bit in signed multiplication also extended to the left. In the process of multiplication of two numbers, the main operation is addition of the partial products. Thus, the performance and speed of the multiplier depends on the performance of the adder that forms the core of the multiplier. The multiplier must be pipelined, to achieve higher performance.

Partial Product Reduction Stage

The design analyses begin with the analysis of the elementary algorithm for multiplication by Wallace Tree multiplier. The algorithm for 8-bits x 8-bits multiplication performs by Wallace Tree multiplier. To complete the multiplication process we have 5 stages. In each stage we used half adders and full adders that are denoted by the red circle for the 1 bit half adder and the blue circle for the 1-bit full adder. Reduce the partial products by using half adders and full adders that are combined to build a Carry-Save Adder (CSA) until there were just two rows of partial products left.

In next step we add the remaining two rows by using a fast carry-propagate adder. For this project to get the final product of the two operands multiplication, Ripple-Carry Adder (RCA) is used, Secondly, the schematic of the conventional 8-bits x 8-bits high speed Wallace Tree multiplier is designed by referring to the algorithm. The block diagram for the conventional high speed 8-bits x 8-bits Wallace Tree multiplier. By the layers of full and half adders we can reduce the number of partial products to 2.The main aim of the proposed architecture is to reduce the overall latency. Thus we increases speed and reduce power consumption. In this design in place of full adders we used compressors. WALLACE tree and DADDA tree are two reduction techniques used which are discussed in paper [6].

Partial Product Addition Stage

We use multiple half adders and full adder's in these addition stages to sum the products of the multiple bits. In this stage the Wallace multiplier method is using Ripple Carry Adders (RCA) to perform these addition operations.

Three steps used in Wallace method to process the multiplication operation. They are

1. Construction of bit product(s).

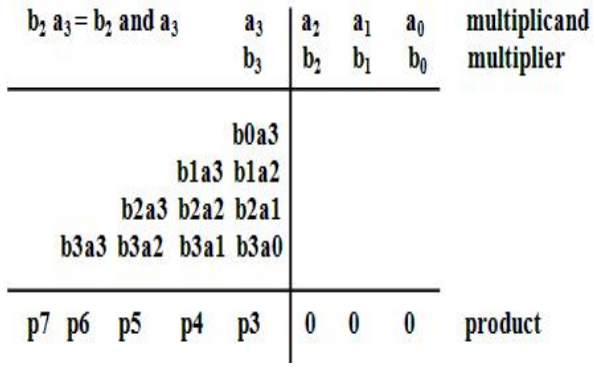
Figure 4: Method of Reduction on 8 x 8 Multiplier

2. Exhausting conventional adder, combine all product matrixes to form 2 vectors (carry and sum) outputs in first row.
3. Fast carry-propagate adder, remaining two rows are summed to produce the product.

TRUNCATED MULTIPLIER

Truncated multiplication is a technique where only the most significant columns of the multiplication matrix are used and therefore area requirements can be reduced. Truncation is a method where the least significant columns in the partial product matrix are not formed. The amount of columns not formed in this way 'T' defines the degree of truncation and the T least significant bits of the product always result in '0'. The algorithm behind truncated multiplication is the same as when dealing with non-truncated multiplication regardless of the truncation degree. The effect is illustrated in Figure 2, where a truncation degree of T = 3, is applied. Notice that the columns to the right of the maroon vertical line are missing [2].

Figure 5: 4 x 4 Bit Binary Multiplication with Truncation Degree T = 3



In the truncated multiplier the removal of unnecessary PPBs is composed of three processes:

A. Deletion

B. Truncation

C. Rounding

Deletion

In truncated multiplier we start the multiplication process with deletion only. In the partial product bits we remove the more than half of the bits, and then remaining bits become the partial products in the process. This is the main criteria of deletion.

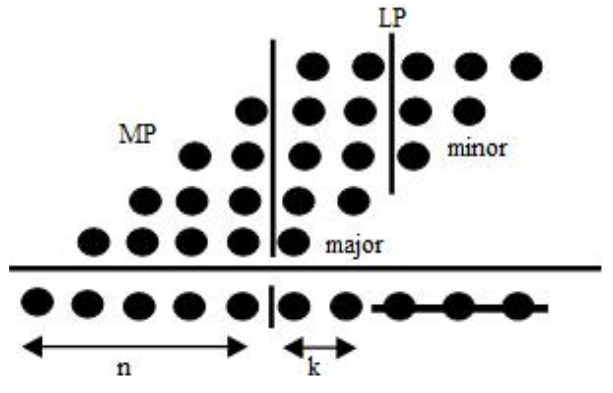
Truncation

Truncation is a method where the least significant columns in the partial product matrix are not formed. The amount of columns not formed in this way 'T' defines the degree of truncation and the T Least Significant Bits (LSB) of the product always results in 0. The algorithm behind fixed width multiplication is the same as when dealing with non-fixed width multiplication regardless of the truncation degree. In filter the 0der of non-uniform coefficient quantization is used to minimize the cost of area [3].

Rounding

Conventionally an n-bit multiplicand and an n-

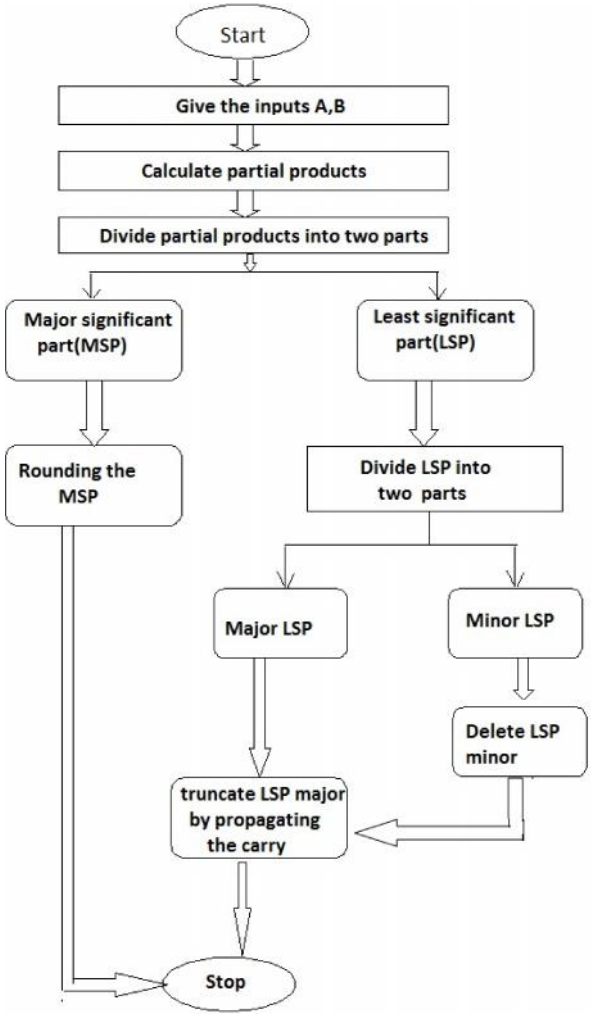
Figure 6: Partial-Products Matrix of a 5 x 5 Bit Multiplier



bit multiplier would render a 2n-bit product. Sometimes an n-bit output is desired to reduce the number of stored bits. Let us consider an instance of 5 x 5 bit multiplier. Truncated multiplication provides an efficient method for reducing the power dissipation and area of rounded parallel multiplier.

Truncated Flow Chart

Figure 7: Truncated Flow Chart



MODIFIED WALLACE MULTIPLIER

In the paper a MAC (Multiplication and accumulation) is implemented using modified Wallace multiplier and for performing the addition the Ripple Carry Adder (RCA) is used. Modified Wallace multiplier is also known as DADDA multiplier. For improving the performance the addition is implemented using reversible 3:2 compressor through which the number of adders required for performing the operation is reduced. A modified Wallace multiplier is an efficient hardware implementation of digital circuit which multiplies two integers. Generally in the reduction phase of conventional Wallace multipliers, many full adders and half adders are used when compared to modified Wallace multipliers. As we know that half adders do not reduce the number of partial product bits. Therefore, it is necessary to minimize the number of half adders used in a multiplier which reduces the hardware complexity. Hence, a modification to the Wallace reduction is done in which the delay is the same as for the conventional Wallace reduction. The modified reduction method greatly reduces the number of half adders with a very slight increase in the number of full adders. Reduced complexity Wallace multiplier reduction consists of three stages. First stage the N x N product matrix is formed and before passing on to the second phase the product matrix is rearranged to take the shape of inverted pyramid. During the second phase the rearranged product matrix is grouped into non-overlapping group of three as shown below, single bit and two bits in the group will be passed on to the next stage and three bits are given to a full adder. The number of rows in each stage of the reduction phase is calculated by the formula

$$r_{i+1} = 2[r_i/3] + r_i \bmod 3$$

If $r_i \bmod 3 = 0$, then $r_{i+1} = 2r_i/3$

Figure 8: Modified Wallace Reduction Block Diagram

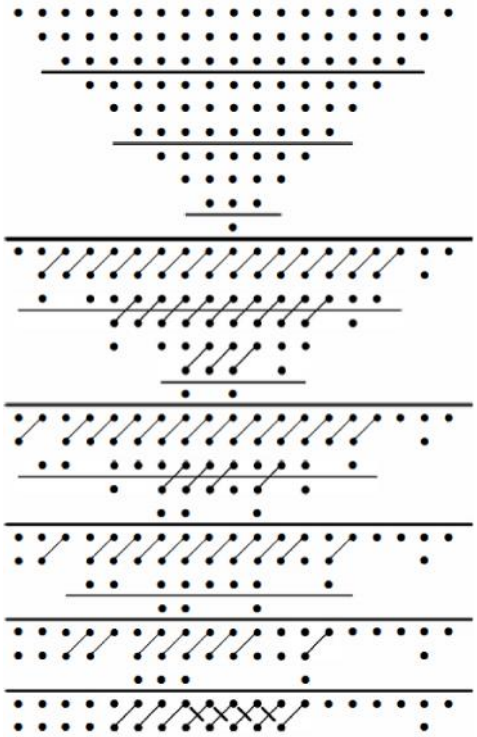
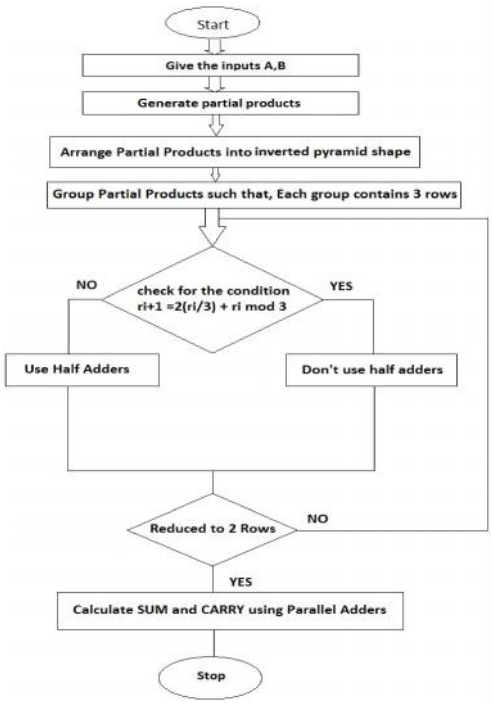


Figure 9: Modified Wallace Flow Chart



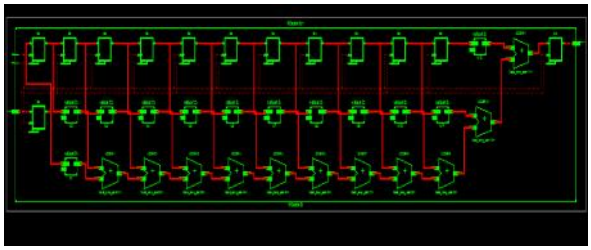
If the value calculated from the above equation for number of rows in each stage in the second phase and the number of rows that are formed in each stage of the second phase does not match, only then the half adder will be used. The final product of the second stage will be in the height of two bits and passed on to the third stage. During the third stage the output of the second stage is given to the carry propagation adder to generate the final output.

RESULTS

FIR Modified Wallace RTL Schematic

The RTL SCHEMATIC gives the information about the user view of the design. The internal blocks contains the basic gate representaion of the logic. These basic gate realization is purely depend upon the corresponding FPGA selection and the internal database information.

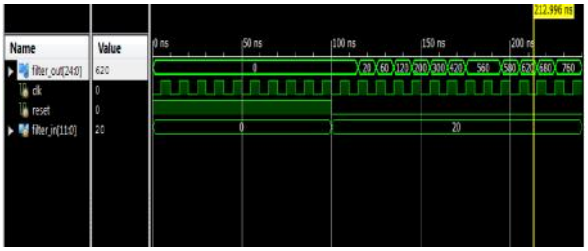
Figure 10: FIR Modified Wallace RTL Schematic



FIR Modified Wallace Waveform

In the waveform which is shown above, clk signal represents clock, reset signal is for providing initialization which we are applying to the design. Similarly filter_out is the output signal for the design. Here clock signal is generated for the positive edge. Initially the reset signal should be force to logic 1 and after one clock cycle made it to logic 0 for performing the corresponding functional operation. To

Figure 11: FIR Modified Wallace Waveform

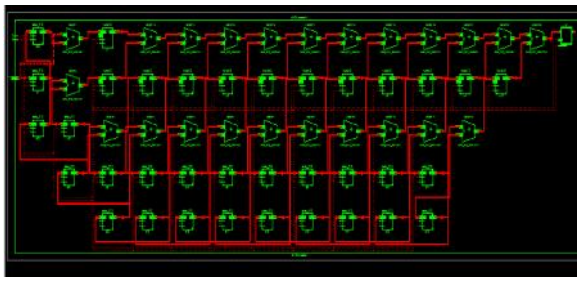


obtain the required outputs force the inputs logic with the required values. Here we provide the filter in as 20. Based on that the fir operation is performed and the resultant values are appeared in the filter_out.

FIR Truncated RTL Schematic

The RTL SCHEMATIC gives the information about the user view of the design.The internal blocks contains the basic gate representaion of the logic.These basic gate realization is purely depend upon the corresponding FPGA selection and the internal database information.

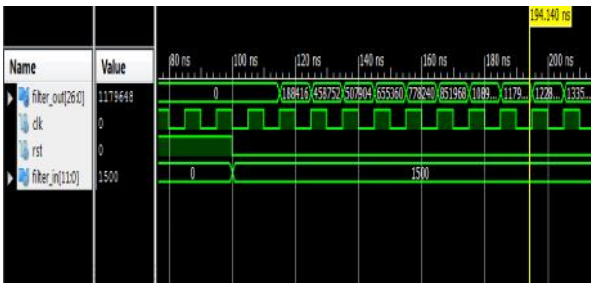
Figure 12: FIR Truncated RTL Schematic



FIR Truncated Waveform

In the waveform which is shown above, clk signal represents clock, reset signal is for providing initialization which we are applying to the design. Similarly filter_out is the output signal for the design. Here clock signal is generated for the positive edge. Initially the

Figure 13: FIR Truncated Waveform



reset signal should be force to logic 1 and after one clock cycle made it to logic 0 for performing the corresponding functional operation. To obtain the required outputs force the inputs logic with the required values. Here we provide the filter in as 1500. Based on that the fir operation is performed and the resultant values are appeared in the filter_out.

Table 1: Modified Wallace FIR Filter Comparision

Bit Width	Memory(kb)	Delay(ns)	No. of LUT'S	Power(mw)
4 bit	244908	10.772	107	0.87236
8 bit	269676	16.854	263	2.14422
12 bit	303532	20.879	688	5.60921

Table 2: Truncated FIR Filter Comparision

Bit Width	Memory(kb)	Delay(ns)	No. of LUT'S	Power(mw)
4 bit	243628	1.320	14	0.11414
8 bit	267884	12.094	691	5.63367
12 bit	357356	16.142	1358	11.0716

CONCLUSION

In this paper the designed fir filter with both modified Wallace and truncated multipliers for 4 bit, 8 bit and 12 bit are compared. From the comparison table it should be concluded that the 12 bit modified Wallace fir filter consumes

less power with the device XC3S100E-5FG320. So for higher order filters the modified Wallace multiplier is well suited especially for low power applications. At the same time the no of adders and multipliers are not that much required along with less delay for this truncated multiplier to design the fir filter when compare with other multiplier like modified Wallace tree multiplier and with literature report especially at low bit rate which here is 4 bit. In the VLSI designing the tradeoff plays a key role. From the table it should concluded, that the design modified Wallace is well suited for higher order and truncated based filter for lower order by maintaining a tradeoff in the accuracy. The functionality is verified through ISE Simulator using VERILOG HDL and the synthesis is carried out with XILINX ISE 12.3i.

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