International Journal of Electrical and Electronic Engineering & Telecommunications

ISSN 2319 – 2518 www.ijeetc.com
Vol. 4, No. 4, October 2015

Research Paper

IMPLEMENTATION OF POWER OPTIMIZED I2CON FOR EFFICIENT DATA TRANSMISSION

Samuel Challapalli[1]* and N Suresh Babu[2]

*Corresponding Author: Samuel Challapalli, ✉ samuel447@gmail.com

As modern computing systems become increasingly complex, communication efficiency among and inside chips has become as important as the computation speeds of individual processor cores. Traditionally, inter-chip and intra-chip communication architectures are separately designed to maximize design flexibility under different constraints. However, jointly designing communication architectures for both inter-chip and intra-chip communication could potentially yield better solutions. In this project, we present an inter/intra-chip optical network, called I2CON, for chip multiprocessors (CMP). I2CON is based on recent progress in nano-photonic technologies. It connects not only processors on a single CMP but also multiple CMPs in a system. I2CON employs a hierarchical optical network to separate inter-chip communication traffic from intra-chip communication traffic. It fully utilizes a single optical network to transmit both payload packets and control packets. The network controller on each CMP not only manages intra-chip communications but also collaborate with each other to facilitate inter-chip communications. By using the proper FSM we prove the communication is happen in the entire chip with reduced power consumption.

Keywords: I2CON, chip multiprocessors (CMP), NOC, Power consumption

INTRODUCTION

Modern computing systems have become increasingly complex to satisfy the growing performance demanded by applications. As the number of transistors available on a single chip increases to billions, chip multiprocessor (CMP) has become an attractive platform delivering high performance with limited power budget. For inter chip communications, bus-based and ad-hoc architectures are still popular, and signals are mostly transmitted by electrical interconnects on Printed Circuit Boards (PCB).The limitations of electrical interconnects such as high-delay and high-power consumption, are already shown in high performance systems. For intra chip

[1] M.Tech Student, Department of ECE, Chirala Engineering College, Chirala, Andhra Pradesh 523157, India.

[2] Associate Professor, Department of ECE, Chirala Engineering College, Chirala, Andhra Pradesh 523157, India.

communication, architectures gradually move from ad-hoc and bus-based architectures to Network-on-Chip (NoC) to alleviate issues including poor scalability and limited bandwidth [1], [2]. Optical interconnects, with advantages including ultra high throughput, low-delay and low-power consumption, are proposed to replace both inter and intrachip electrical wires. Traditionally, interchip/intrachip communication architectures are separately designed.

There is a huge performance gap between intra and interchip electrical interconnects. First, the delay of on-chip wires is much smaller than the off-chip ones because of the substantially smaller physical length, resistance, and capacitance. For optical interconnects, unlike electrical wires, inter and intrachip channels can be interconnected seamlessly. Both on-chip and off-chip channels can be implemented with optical waveguides and they can be interconnected with passive couplers. The allowed operating bandwidths of both waveguides are broad enough for real applications. Given the high propagation speed of light, the delay difference for on-chip and off-chip links is minor. In addition, if the small transmission loss is neglected, the transmission power is independent of transmission length. All these make the optical interchip and intrachip interconnects well matched, and a unified design becomes natural. There are different methods are available for inter/intra chip communication. Apart from the electrical connection optical interconnections are the better method. The following sections deals with literature background of different algorithms and their comparative analysis.

With CMOS technology scaling down, many core processors are becoming an attractive platform delivering high performance with limited power budget. It is projected that hundreds or even thousands of cores will be integrated on the chip. In a many core processor system with so many cores, the communication demand will be so large that conventional electrical interconnects may not be able to fulfill it due to the bandwidth density and energy consumption constraints. The limitation of the communication subsystem will confine the many core processor performance severely. Another limitation to the future many core processors is the power density. It is estimated that more than 50% cores on the chip at 8 nm will not be utilized due to the power constraint [1]. The process yield will also confine the chip area and hence the scalability of future many core processor. Breaking a large many core processor into many smaller processors may decrease the power density as well as increase the yield. However, it requires enormous inter-chip bandwidth, laying the burdens on the off-chip interconnects, which is already the bottleneck of the system performance. The 3-D technology can be used to stack the chips and support low-latency inter-chip communication. However, the power density becomes even higher.

With the recent progress in silicon photonics, optical interconnects may be adopted to address these issues effectively. Optical interconnects promise ultrahigh bandwidth, low latency, and low energy consumption. They can address both the intra-chip and inter-chip communication requirements with limited power budget. For example, a silicon waveguide on the chip can

support a data rate of 10 Gb/s for each light wavelength, and multiple wavelengths can be multiplexed into the single waveguide to achieve extremely high bandwidth. The waveguide can also be connected with off-chip waveguide passively to support ultrahigh off-chip bandwidth.

Optical network-on-chip (ONoC) using optical interconnects has been put forward to replace electronic NoC by many studies [2]-[7]. These works mainly focus on the intra-chip communication, while the work in [8] only deals with the inter-chip network. In this paper, we propose a new inter/intra-chip optical network (I2CON), which supports both intra-chip and inter-chip communication. It includes multiple intra-chip sub networks and an off-chip one, where the intra-chip and inter-chip sub networks are code signed to balance the bandwidths and the resources as well.

LITERATURE SURVEY

Based on the silicon photonic technologies, different on-chip network architectures have been proposed. Kirman *et al.* [13] presented an opto-electrical hierarchical bus for future manycore processors with cache-coherence supported. Xu *et al.* [14] proposed a hierarchical optical network and a composite cache coherence protocol, trying to acquire both advantages in snoopy and directory-based protocols. Pasricha and Dutt [15] proposed an optical ring waveguide to replace global pipelined electrical interconnects while preserving the interface with bus protocol standards. O'Connor [3] presented a full connected ONoC based on the special λ-I2CON with WDM technology. Shacham et al. [5] proposed a hybrid ONoC combining an optical circuit-switched network with an electrical packet switched network. Joshi *et al.* [16] presented a photonic close network in which long electrical links between I2CONs are replaced by optical ones.

The proposed network provides more uniform latency and higher throughput compared with mesh network. Cianchetti *et al.* [4] proposed a packet-switched optical network. The packet may pass through multiple I2CONs without being buffered as long as no collision happens. Li *et al.* [17] proposed a hybrid network in which optical network is used to broadcast latency-critical messages and electrical network is used to transfer high bandwidth traffic. Ouyang *et al.* [18] proposed an ONoC based on freespace optical interconnects to reduce power consumption. Psota *et al.* [19] used WDM technology to build contentionfree network, which facilitated new programming model. Koohi *et al.* [20] proposed hierarchical optical rings, where local rings are used for intranode communication and global rings are to connect the nodes. In all these designs, only one chip is considered, and the networks are proposed to address the intra-chip communication requirements. In I2CON, we also use an optical intra-chip subnetwork to support the on-chip communication; but more importantly, we use an inter-chip network, which is highly correlated with on-chip network to address the communication among chips.

The on-chip subnetwork in I2CON is an optical crossbar network with ring topology. Similar topologies have been proposed in [2], [6], and [19]-[21]. In crossbar design with large network resources, link sharing is important to reduce the resource requirements. For

example, Vantrease *et al.* [2] proposed a crossbar, in which a waveguide for data transfer is shared by multiple writers and a single reader. On the other hand, Pan *et al.* [21] proposed a design that a waveguide is shared by single writer and multiple readers. In [6], a waveguide can be further shared by Multiple Writers and Multiple Readers (MWMRs). Xu *et al.* [18] proposed a channel borrowing technology to improve the channel utilization and also reduce the power consumption. In all these designs, a waveguide is unidirectional, and at any time, there can be no more than one transaction with same wavelengths in a single waveguide. In I2CON, bidirectional transmission is supported, and we further improve the resource sharing by allowing concurrent transmissions with same wavelengths on a single waveguide.

NOC WITH INTER INTRA COMMUNICAITON TOPOLOGY

To meet the growing computation-intensive applications and the needs of low-power, high-performance systems, the number of computing resources in single-chip has enormously increased, because current VLSI technology can support such an extensive integration of transistors. By adding many computing resources such as CPU, DSP, specific IPs, etc., to build a system in System-on-Chip, its interconnection between each other becomes another challenging issue. In most System-on-Chip applications, a shared bus interconnection which needs arbitration logic to serialize several bus access requests, is adopted to communicate with each integrated processing unit because of its low-cost and simple control characteristics. However, such shared bus interconnection has some limitation in its scalability because only one master at a time can utilize the bus which means all the bus accesses should be serialized by the arbitrator. Therefore, in such an environment where the number of bus requesters is large and their required bandwidth for interconnection is more than the current bus, some other interconnection methods should be considered.

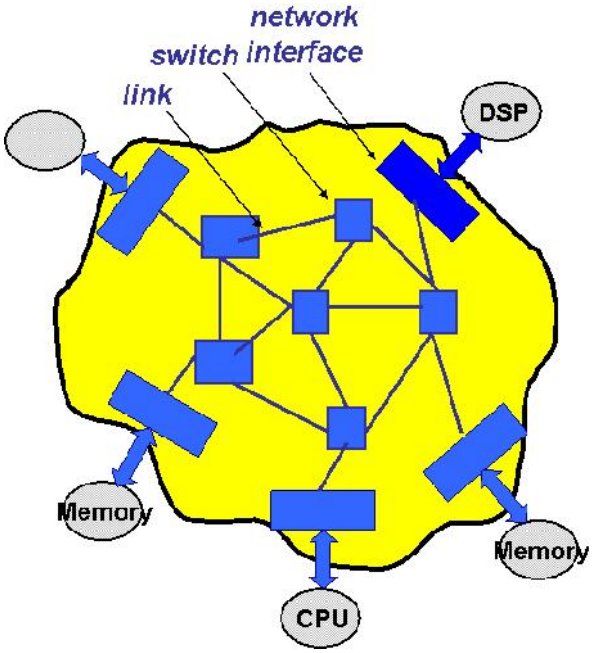
One possible solution to these problems requires a stronger adoption of hardware reuse methodologies, that lead the way to the creation of flexible platforms, while minimizing the design effort for building new systems. Tomorrow complex on-chip systems will be almost always created assembling a great number of IP modules, developed in house as well as by third party partners. Furthermore the growth of the number of elements that need to be interconnected is starting to increase the negative side effects of classical “shared bus” architectures, and pose the need for an interconnection system that allows more than one IP to use the communication resources at the same time. “For all these reasons the NoC approach appears to be the most promising solution at hand “. Network on chip or network on a chip (NoC or NOC) is a communication subsystem on an integrated circuit (commonly called a “chip”), typically between Intellectual Property (IP) cores in a System on a Chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC technology applies networking theory and methods to on-chip communication and brings notable

improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs.

System Overview

Network on chip topology is composed by an arbitrary number of instances of three basic kind of functional blocks are Network Interfaces, Switches, Links.As shown in the fig1 Network Interfaces connect all the IP cores to the network, mapping the bus type transitions coming from the IPs into packets that can be propagated inside the Network on chip and, on the opposite side, building the bus transactions that correspond to packets that need to exit the NoC. Switches carry out the task of dispatching packets inside the network, depending on the particular routing scheme choosen. The number of ports depends on the topology of the network. Usually they have buffers inside for storing information tokens, in order to minimize the risk of losing data due to congestion problems. Links connect switches with network interfaces or with other switches. Links can be latency insensitives and can also contain buffering resources if needed by a particular application.

Figure 1: NOC Topology



As the semiconductor processing technology is advanced to sub-nano one, there are several side effects awaited. One of critical issues is a wiring delay. While the speed of basic elements such as gate delay becomes much faster, the wiring delay is growing exponentially as shown in Figure 2 because of the increased capacitance caused by narrow channel width and increased crosstalk. Therefore, if this trend be sustained, the wiring is one of the critical issues to be concerned.

There are quite a few topologies proposed for NoCs including fat tree, honeycomb, 2D mesh, etc.; we will discuss the most common and agreed upon topology – 2D mesh – in our tutorial because of its simplicity. Consider Figure 3 which shows a simple mesh topology

Figure 2: Technical Roadmap in Semiconductor Industry [1]

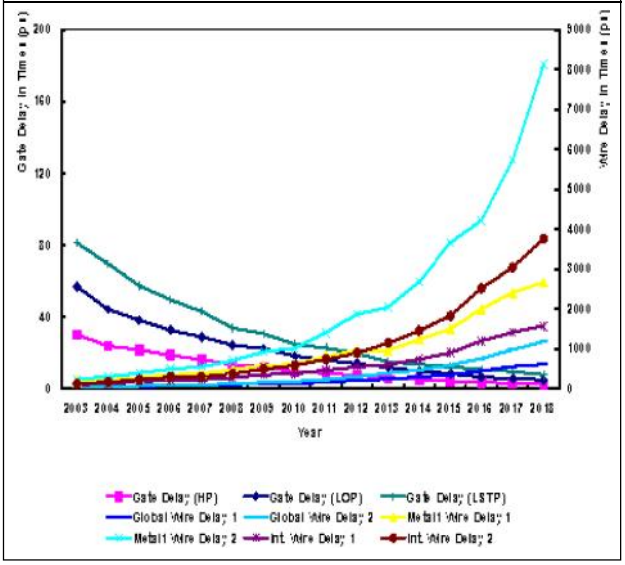
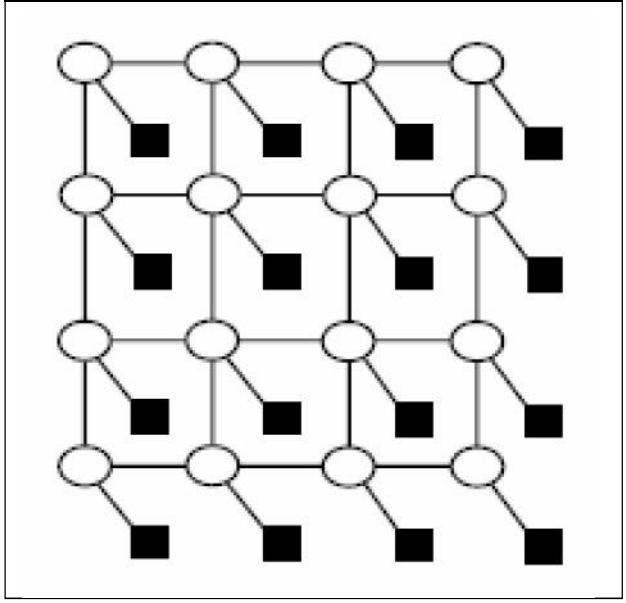


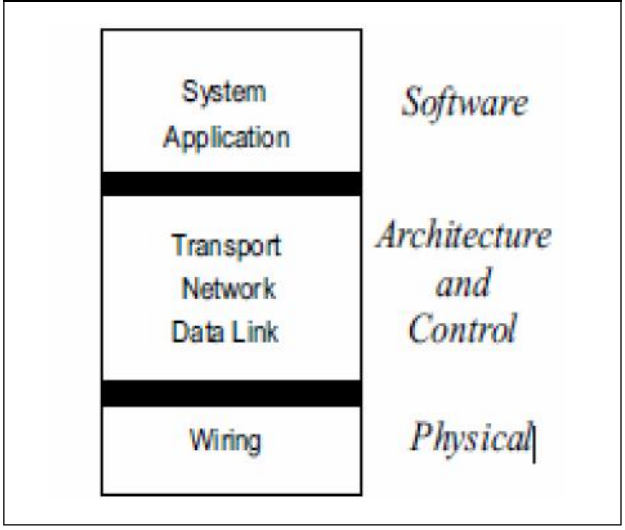
Figure 3: 2D Mesh Based NoC



where circles represent switches while squares are resources. A resource is a computational unit; it can be a processor, memory, DSP core, etc., whereas switches route and buffer messages between resources. It can be seen from the Figure 3 that almost each switch is directly connected to neighboring four switches (except for the ones at the edges). The communication channel consists of two one-directional point-topoint buses between two neighboring switches or a switch and a resource. It is expected that, as the technology grows with time, the number and size of resources will also grow, resulting in growth of bandwidth of switch-to-switch or switch-to resource links, but network wide communication will remain unaffected.

Routing is the process of moving information from a source to a designated target. This term is very common in the Internet. Routing can be static or dynamic. Static routing is managed by an administrator manually, and is suitable for networks where

Figure 4: Protocol Stack for NoC's



network traffic is predictable and relatively simple, which is a rare case in the Internet. Dynamic routing, as the name suggests, is used to dynamically discover routes in case of path changes. Due to the regular structure and on-chip memory constraints static routing is more feasible for NoCs. However, in case of path failures, adaptive routing can be introduced but special care must be taken as to avoid excessive use of buffers or logic on-chip.

Optical Network-on-Chip (ONoC) is a new type of Network on Chip (NoC) for multiprocessor system-on-chip. While traditional NoC relies on electrical signals to transfer information, hence called Electrical Network-on-Chip (ENoC), its performance and energy efficiency are bound by the significantly unbalanced scaling of on-chip global metal wires comparing to transistors. Optical telecommunications have been successful in many networking domains to replace electrical telecommunications. Riding on the achievements of photonic technologies, a wide range of studies have been done on ONoC.

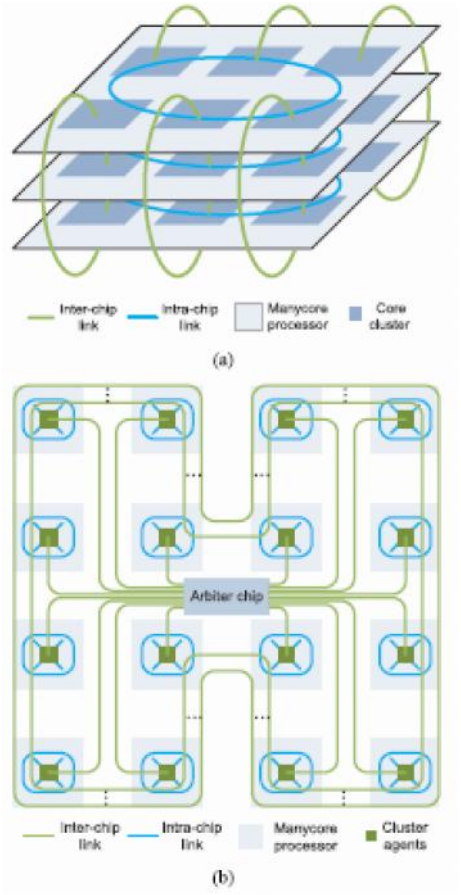
ARCHITECTURE OVERVIEW

I2CON targets an optically connected manycore processor system with multiple chips. On each chip, there are two layers: 1) optical layer and 2) electrical layer. They are stacked together with 3-D stacking technology. There are processor cores in the electrical layer. In optical layer, siliconphotonic devices, including waveguides, optical switches, and photodetectors, will be fabricated to support optical signal transmission. On-chip lasers, VCSELs, are bonded on the chip as light sources. The cores on the electrical layer can access these optical components with through-silicon-vias. The chips are bonded on the board and connected with boardlevel optical interconnects. The on-chip optical fabrics work together with the on-board waveguides to facilitate not only the intra-chip communication among the cores on the same chip, but also the inter-chip communication among the cores on different chips.

The logical view of I2CON is shown in Figure 5a. It is composed of an inter-chip network and multiple intra-chip networks. Each intra-chip network is to interconnect all cores on the same chip plane. And the inter-chip network is to thread the cores in a third dimension, which is perpendicular to the chip plane. In this way, the chips are virtually stacked like a 3-D chip. Optical signals can tolerate much longer distance than electrical signals, given that a longer distance will not introduce much power, throughput, and latency overheads. Therefore, physically, the chips are placed far away from each other as shown in Figure 5b. The large distance between chips can essentially reduce the power density. These features can help build a logical dense but physical-large system.

Figure 5: Conceptual Topology and Physical Floorplan Overviews of I2CON

(a) Logical View of I2CON



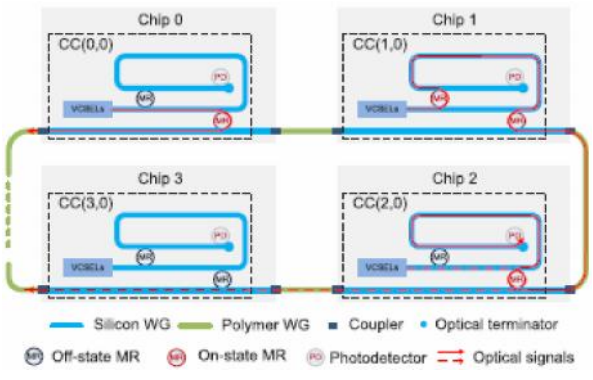
(b) Physical Floorplan of I2CON

Inter-chip network addresses the communication requirements among the chips. The requirements, such as large bandwidth density, low latency, and low power consumption, are difficult to be fulfilled by the conventional electrical wires. By exploiting the inherent properties of optical links, we place the chips far from each other to reduce the power density but still provide high performance and high energy efficiency communication structure. The inter-chip network is composed of data channels and the accompanying control fabrics. There are N

data channels, which are parallel to each other with the same design. They connect the core-clusters in different chips. Payload data are transmitted between clusters on different chips. The control fabric is composed of the control channels and an arbiter chip, as shown in Figure 5b. Before accessing the data channel, the clusters are required to send requests to the arbiter chip through the control channels. The arbiter chip will make the arbitration and also configure the data channels by sending out control information to the data channels. The detailed design of data channels will be discussed first, followed by the discussion of the control structure.

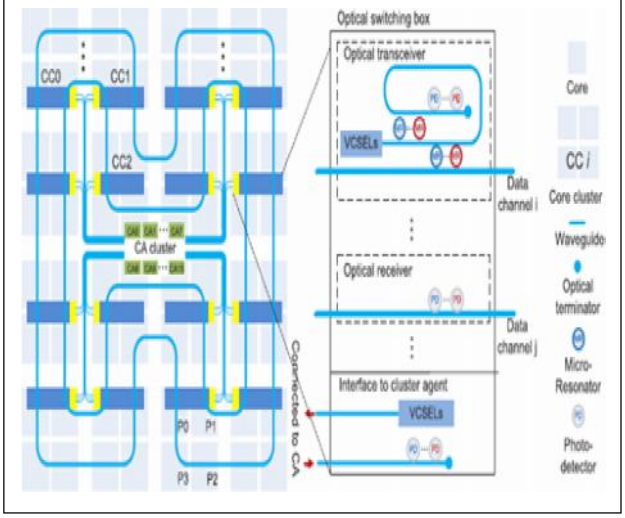
The MR is a switching element. It can divert the light with resonance wavelength from one waveguide to the opposing one. The resonance wavelength of the MR can be controlled by electrical voltage. The functionality of the MR in the data channel can be shown in Figure 6. In the transceiver of cluster CC(0, 0), the upper left MR is turned OFF, and the light passes by this MR safely. On the other hand, in the transceiver of cluster CC(1, 0), the upper left MR is turned ON and it diverts the light from one waveguide to another parallel one. Therefore, by turning ON/OFF the MR, the light will take different paths.

Figure 6: Illustration of Inter-Chip Data Channel 0. One Wavelength is Illustrated, Both Solid and Dashed Lines are Used to Distinguish the Different Transactions at the Same Wavelength



In I2CON, multiple homogenous chips are used. The architecture of the chip with intra-chip network is shown in Figure 7. All the core-clusters are interconnected with each other by the parallel closed-loop channels. The cluster accesses the channels with optical switching box shown in the right side of Figure 7. The communication among the cores are coordinated by the control subsystem. In the control subsystem, each cluster is assigned with a Cluster Agent (CA). All agents are located at the chip center, forming cluster agent cluster as shown in Figure 7. They are interconnected with short local electrical wires, while each cluster agent is connected to the corresponding cluster with dedicated optical waveguides. This approach utilizes the advantages of optical interconnects in long distance communication and electrical interconnects in short distance.

Figure 7: Overview of Intra-Chip Architecture and its Floor Plan



FUNCTIONALITY AND PRINCIPLES OF I2CON DESIGN

A I2CON is a device that forwards data packets between computer networks. This creates an overlay internetwork, as a I2CON is connected to two or more data lines from different networks. When a data packet comes in one of the lines, the I2CON reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table or routing policy, it directs the packet to the next network on its journey. I2CONs perform the "traffic directing" functions on the Internet. A data packet is typically forwarded from one I2CON to another through the networks that constitute the internetwork until it reaches its destination node.

Routing is the process of selecting best paths in a network. In the past, the term routing was also used to mean forwarding network traffic among networks. However this latter function is much better described as simply forwarding. Routing is performed for many kinds of networks, including the telephone network (circuit switching), electronic data networks (such as the Internet), and transportation networks. This article is concerned primarily with routing in electronic data networks using packet switching technology. In packet switching networks, routing directs packet forwarding (the transit of logically addressed network packets from their source toward their ultimate destination) through intermediate nodes. Intermediate nodes are typically network hardware devices such as I2CONs, bridges, gateways, firewalls, or switches. In many instances, an ISP will allow you to use a I2CON and connect multiple computers to a single Internet connection and pay a nominal fee for each additional computer sharing the connection. This is when home users will want to look at smaller I2CONs, often called broadband I2CONs that enable two or more computers to share an Internet connection. Within a business or organization, you may need to connect multiple computers to the Internet, but also want to connect multiple private networks Not all I2CONs are created equal since their job will differ slightly from network to network. General-purpose computers can also forward packets and perform routing, though they are not specialized hardware and may suffer from limited performance. The routing process usually directs forwarding on the basis of routing tables which maintain a record of the routes to various network destinations. Thus, constructing routing tables, which are held in the I2CON's memory, is very important for efficient routing. Most routing algorithms use only one network path at a time.

RESULTS

Waveform for the I2CON

In the waveform which is shown above, clk signal represents clock which we are applying to the design. Similarly channel outputs are the output signal for the design. Here clock signal is generated for the positive edge. Initially the resetn signal should be force to logic 1 and after one clock cycle made it to logic 0 for performing the corresponding functional operation. To obtain the required outputs force the inputs logic with the required values. Here the I2CON operation is performed perfectly with both inter and intra communication topology and information is routed to the

Figure 8: Waveform for the I2CON

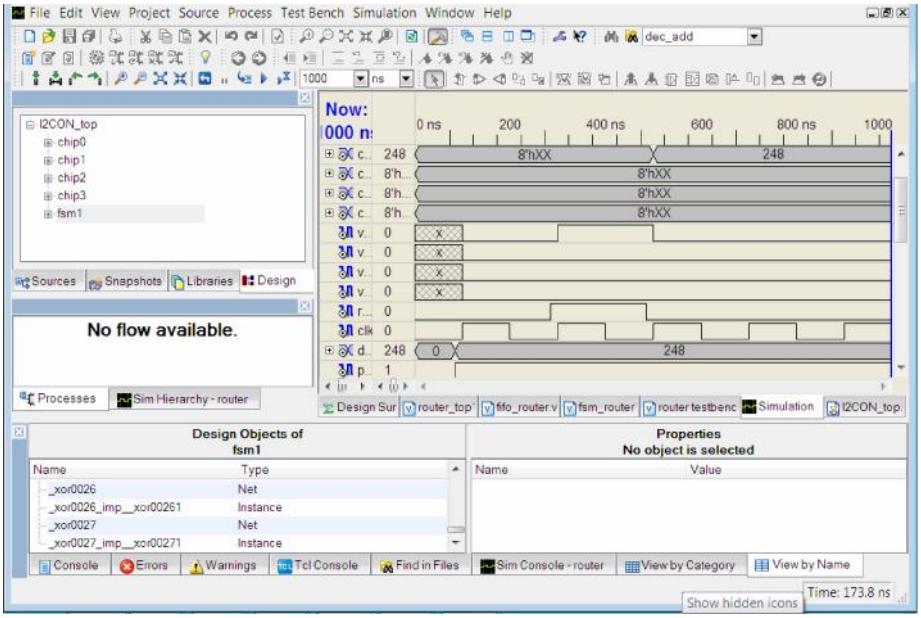


Figure 9: RTL Schematic

corresponding channel based on the address which is provided.

RTL Schematic

The RTL SCHEMATIC gives the information about the user view of the design.The internal blocks contains the basic gate representaion of the logic.These basic gate realization is purely depend upon the corresponding FPGA selection and the internal database information.

CONCLUSION

The advances in nano photonics have motivated us to exploit the benefits of optical interconnects for future many core processor with a large number of cores. In this paper, we propose an inter/intra-chip optical network called I2CON, which supports high-throughput with reduced power consumption for the multichip system. The proposed network effectively explores the distinctive properties to boost performance as well as reduce power consumption which is 22.1 uw when compare with the literature report power 100 uw. The simulation and synthesis is carried out using XILINX ISE EDA and the RTL is developed based on the VERILOG language.

REFERENCES

1. Bartolini S and Grani P (2012), "A Simple on-Chip Optical Interconnection for Improving Performance of Coherency Traffic in CMPs", in Proc. 2012 15th Euromicro Conf. DSD, September, pp. 312-318.
2. Beux S L, Trajkovic J, O'Connor I, Nicolescu G, Bois G and Paulin P (2011), "Optical Ring Network-on-Chip (ORNoC): Architecture and Design Methodology", in Proc. DATE Conf. Exhibition, March, pp. 1-6.
3. Cianchetti M J, Kerekes J C and Albonesi D H (2009), "Phastlane: A Rapid Transit Optical Routing Network", in *Proc. 36th Annu. ISCA*, pp. 441-450, New York, USA.
4. Dong P *et al.* (2010), "Low Loss Silicon Waveguides for Application of Optical Interconnects", in Proc. 2010 IEEE Photonics Society Summer Topical Meeting Series, July, pp. 191-192.
5. Esmaeilzadeh H, Blem E, Amant R S, Sankaralingam K and Burger D (2012), "Dark Silicon and the End of Multicore Scaling", *IEEE Micro*, Vol. 32, No. 3, pp. 122-134.
6. Joshi A *et al.* (2009), "Silicon-Photonic Clos Networks for Global on-Chip Communication", in Proc. 3rd ACM/IEEE Int. Symp. Networks-on-Chip, May, pp. 124-133.
7. Kirman N *et al.* (2006), "Leveraging Optical Technology in Future Bus-Based Chip Multiprocessors", in Proc. 39th Annu. IEEE/ACM Int. Symp. Microarchitecture, pp. 492-503, Washington, DC, USA.
8. Koka P, McCracken M O, Schwetman H, Zheng X, Ho R and Krishnamoorthy A V (2010), "Silicon-Photonic Network Architectures for Scalable, Power-Efficient Multi-Chip Systems", in Proc. 37th Annu. ISCA, pp. 117-128, New York, USA.
9. Koohi S, Abdollahi M and Hessabi S (2011), "All-Optical Wavelength Routed NoC Based on a Novel Hierarchical Topology", in Proc. 5th 2011 IEEE/ACM Int. Symp. Networks Chip, May, pp. 97-104.
10. Li Z *et al.* (2009), "Spectrum: A Hybrid Nanophotonic—Electric On-Chip Network", in Proc. 46th ACM/IEEE DAC, July, pp. 575-580, New York, USA.
11. Masini G, Capellini G, Witzens J and Gunn C (2007), "A 1550 nm, 10 Gbps Monolithic Optical Receiver in 130 nm CMOS with Integrated Ge Waveguide

Photodetector", in Proc. 4th IEEE Int. Conf. Group IV Photonics, September, pp. 1-3.

12. O'Connor I (2009), "Optical Solutions for System-Level Interconnect", in Proc. 2004 Int. Workshop SLIP, pp. 79-88, New York, USA.
13. Ouyang J, Yang C, Niu D, Xie Y and Liu Z (2011), "F2BFLY: An On-Chip Free-Space Optical Network with Wavelength-Switching", in Proc. ICS, pp. 348-358, New York, USA.
14. Pan Y, Kim J and Memik G (2010), "Flexi Share: Channel Sharing for an Energy-Efficient Nanophotonic Crossbar", in *Proc. IEEE 16th Int. Symp. HPCA*, January, pp. 1-12.
15. Pan Y, Kumar P, Kim J, Memik G, Zhang Y and Choudhary A (2009), "Firefly: Illuminating Future Network-on-Chip with Nanophotonics", in *Proc. 36th ISCA*, Vol. 37, No. 3, pp. 429-440.
16. Pasricha S and Dutt N (2008), "ORB: An On-Chip Optical Ring Bus Communication Architecture for Multi-Processor Systems-on-Chip", in Proc. ASPDAC, March, pp. 789-794.
17. Psota J *et al.* (2010), "ATAC: Improving Performance and Programmability with On-Chip Optical Networks", in Proc. 2010 IEEE ISCAS, May/June, pp. 3325-3328.
18. Rao Y (2012), "In P-Based Long Wavelength VCSEL Using High Contrast Grating", December, Ph.D. Dissertation, Dept. Elect. Eng. Comput. Sci., Univ. California, Berkeley, CA, USA.
19. Shacham A, Bergman K and Carloni L P (2008), "Photonic Networks-on-Chip for Future Generations of Chip Multiprocessors", *IEEE Trans. Comput.*, Vol. 57, No. 9, pp. 1246-1260.
20. Vantrease D *et al.* (2008), "Corona: System Implications of Emerging Nanophotonic Technology", in *Proc. 35th ISCA*, June, pp. 153-164.
21. Xu S P Q, Schmidt B and Lipson M (2005), "Micrometre-Scale Silicon Electro-Optic Modulator", *Nature*, Vol. 435, May, pp. 325-327.
22. Xu Y, Du Y, Zhang Y and Yang J (2011), "A Composite and Scalable Cache Coherence Protocol for Large Scale CMPs", in Proc. ICS, pp. 285-294, New York, USA.